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Non-isolated stacked bidirectional soft-switching DC-DC converter with PWM plus phase-shift control scheme

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Abstract In this paper, a non-isolated stacked bidirectional DC-DC converter with zero-voltage-switching (ZVS) is introduced for the high step-up/step-down conversion systems. The extremely narrow turn-on and/or turn-off duty cycle existing in the conventional bidirectional buck-boost converters can be extended due to the stacked module configuration for large voltage conversion ratio applications. Furthermore, the switch voltage stress is halved because of the series connection of half bridge modules. The PWM plus phase-shift control strategy is employed, where the duty cycle is adopted to regulate the voltages between the input and output sides and the phase-shift angle is applied to achieve the power flow regulation. This decoupled control scheme can not only realize seamless bidirectional transition operation, but also achieve adaptive voltage balance for the power switches. In addition, ZVS soft-switching operation for all active switches is realized to minimize the switching losses. Finally, a prototype of 1 kW operating at 100 kHz is built and tested to demonstrate the effectiveness of the proposed converter and the control strategy.

Keywords Bidirectional DC-DC converter, PWM plus phase-shift control (PPS), Zero voltage switching (ZVS), Large voltage conversion ratio, Flexible power flow regulation

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1 Introduction

Energy storage systems (ESS) with bidirectional DC-DC converters are essential in renewable energy based micro-grids, electric vehicles (EVs), transportations, et al [1–5]. Bidirectional DC-DC converters play the role of converting and transferring the electrical energy of the storage elements, which conduct both charge and discharge operation. As a result, the bidirectional DC-DC converters are the key interfaces for efficient energy management. Generally, the voltage of the storage elements is relatively low due to safety issues. Meanwhile, the bus voltage of the DC-based micro-grid, electric EVs and plug-in hybrid EVs (PHEVs) is relatively high in order to improve the system power level. Consequently, a step-up and step-down bidirectional converter is required to link the low voltage storage elements and high voltage bus. How to derive high efficiency DC-DC converters with large conversion ratio is still challengeable in the power electronics community.

Isolated bidirectional DC-DC converters with high-frequency transformer, such as the Flyback-based [6, 7], Forward-Flyback based [8], boost integrated Flyback rectifier/energy (BIFRED) based [9], dual half-bridge based [10, 11], dual active bridge (DAB) based converters [12–15] and their counterparts [16–22], can easily achieve high step-up/step-down conversion because the turns ratio of the transformer provides another control freedom for the voltage regulation. However, the conduction losses and transformer losses are a little high because the whole delivered energy will flow through the power switches and windings of primary and secondary sides.

If the passive diodes in buck or boost converters are replaced by active switches, the conventional bidirectional Buck-Boost converters are formed. They suffer from large switching losses due to the hard switching operation. In order to solve this problem, some active and/or passive components are inserted to achieve zero-voltage-switching (ZVS) or zero-current-switching (ZCS) performance [12, 23–26]. However, the additional active switches may increase the control complexity and the passive components may bring extra voltage or current stress on the power switches. More importantly, extreme duty cycle and high voltage stress for the power switches are inevitable in large conversion ratio and high voltage applications, which would limit the converter efficiency and dynamic response.

In order to avoid the extreme duty cycle operation, multi-level converters are attractive candidates [27, 28]. Three level bi-directional converters are proposed by introducing the three-level tank into the conventional bidirectional converters. The switch voltage stress is only half of the high-side voltage [29]. And the inductor is reduced to improve the dynamic response due to the reduced voltage step.

An advanced non-isolated stack bidirectional DC-DC converter is proposed in [30], which has a high step-up/step-down conversion ratios. This converter is controlled by an optimized PWM method, which is divided into forward and reverse modes according to the power flow. Seamless mode change is realized by introducing an intermediate switching pattern. However, the PWM plus phase-shift control (PPS) control scheme, which is widely adopted in the isolated converters [31–33], can be employed in this non-isolated stack converter to improve the circuit performance. The duty cycle and phase shift angle of the PPS control strategy can not only balance the voltage of the high and low voltage side sources, but also regulate the power flow independently and smoothly, which eliminates the requirement of switching pattern change. Furthermore, due to the stack structure and PPS control method, the voltage stress of power switches is reduced to half of the high-side voltage and the extreme duty cycle operation is avoided in high step-up/step-down conversion systems. Moreover, ZVS soft switching operation is achieved for all the power switches without any additional active or passive components.

The outline of this paper is highlighted as follows. The brief introduction of the non-isolated stack converter with PPS control and the steady-state operation analysis are illustrated in Section 2. The performance characteristics of the converter are specified in Section 3. Besides, the phase-shift angle selection analysis is implied in Section 4. The performance of the introduced converter is verified by a 1 kW prototype in Section 5. The main contributions of this paper are summarized in the last section.

2 Bidirectional converter with PPS control and its steady-state operation analysis

The stacked bidirectional converter in [30] is redrawn in Fig. 1. In Fig. 1, V_{H} and V_{L} are the high and low side voltage sources; C_{H1} and C_{H2} are the series capacitors to perform as a voltage divider in the high voltage side; $\mathrm{S}_1 \sim \mathrm{S}_4$ are the active switches with their parasitic capacitors $C_{\mathrm{s1}} \sim C_{\mathrm{s4}}$; L_{r} is the resonant inductor; C_{r} is the resonant capacitor; L_{f} and C_{L} are the filter inductor and capacitor in the low voltage side; $i_{L_{\mathrm{r}}}$ and $i_{L_{\mathrm{f}}}$ are the currents of L_{r} and L_{f}; i_{x} is the neutral current of the series capacitors; $V_{C_{\mathrm{H1}}}$, $V_{C_{\mathrm{H2}}}$, $V_{C_{\mathrm{r}}}$ are the voltages of C_{H1}, C_{H2} and C_{r} with the defined polarities; f_{s} is the switching frequency.

PPS control strategy is applied to the stacked converter to balance the voltage and regulate the power flow between the high and low voltage terminals. S_2 is driven complementarily with S_1, while S_4 works complementarily with S_3. S_1 and S_3 act with the same duty cycle D, and D is regulated to balance the high-side and low-side voltages. The phase-shift angle between S_1 *and* S_3 *is* indicated as φ. The range of φ is limited from $-DT_{\mathrm{s}}$ to DT_{s}. The key waveforms of the stacked converter at the steady-state operation are plotted in Fig. 2. There are two operation

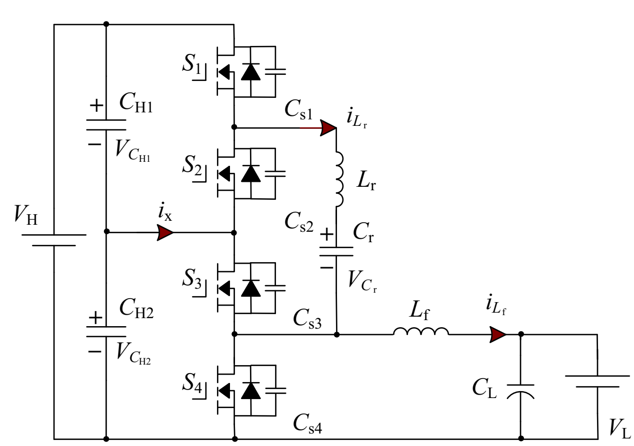

Fig. 1 Stacked bidirectional converter

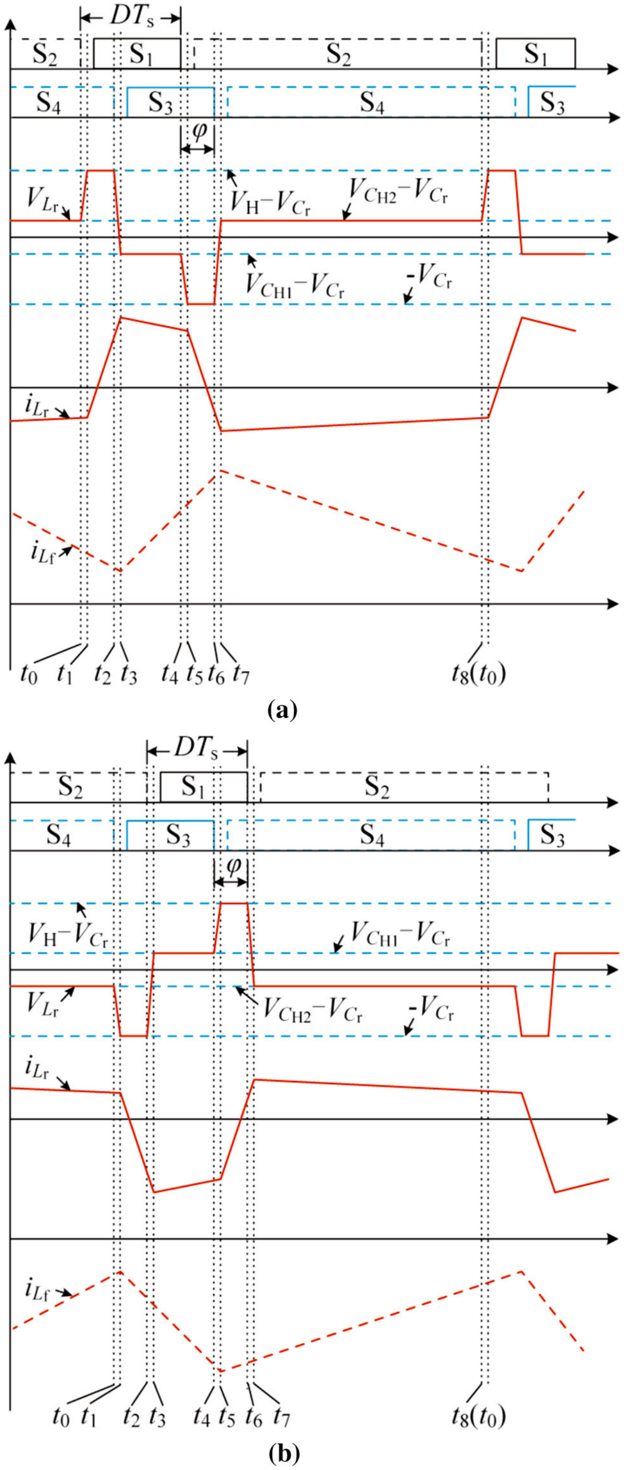

Fig. 2 Steady-state waveforms of stacked converter

modes corresponding to the power flow directions. One is the buck mode, where the energy is delivered from the high side to low side, and the other is the boost mode, where the energy flows reversely. Due to the symmetrical operation of the introduced converter, the buck mode is taken as an example to analyze its steady-state operation.

In order to simplify the analysis, the following assumptions are made: ① the voltage ripples on the capacitors C_{H1}, C_{H2} and C_r are small and ignored; ② the voltages $V_{C_{H1}}$, $V_{C_{H2}}$ are balanced. There are 8 operation stages in one switching period analyzed as follows and the equivalent operation circuits are illustrated in Fig. 3.

1) Stage 1: $[t_0 \sim t_1]$

Before t_0, S_2 and S_4 are both in the turn-on state and the current i_{L_r} i_{Lr} flows through L_r negatively. At t_0, S_2 is turned off. Due to the capacitor C_{s2}, ZVS turn-off for S_2 is ensured. The current i_{L_r} keeps unchanged as the operation interval is short. Consequently, C_{s2} is charged while C_{s1} is discharged linearly.

2) Stage 2: $[t_1 \sim t_2]$

At t_1, the voltage of C_{s1} is reduced to zero. As a result, the resonant current i_{L_r} flows through the anti-parallel diode of S_1 before its turn-on gate signal comes. S_1 is turned on with ZVS during this stage. i_{L_r} increases and i_{L_f} decreases linearly, and the neutral current i_x is zero. The currents are derived by

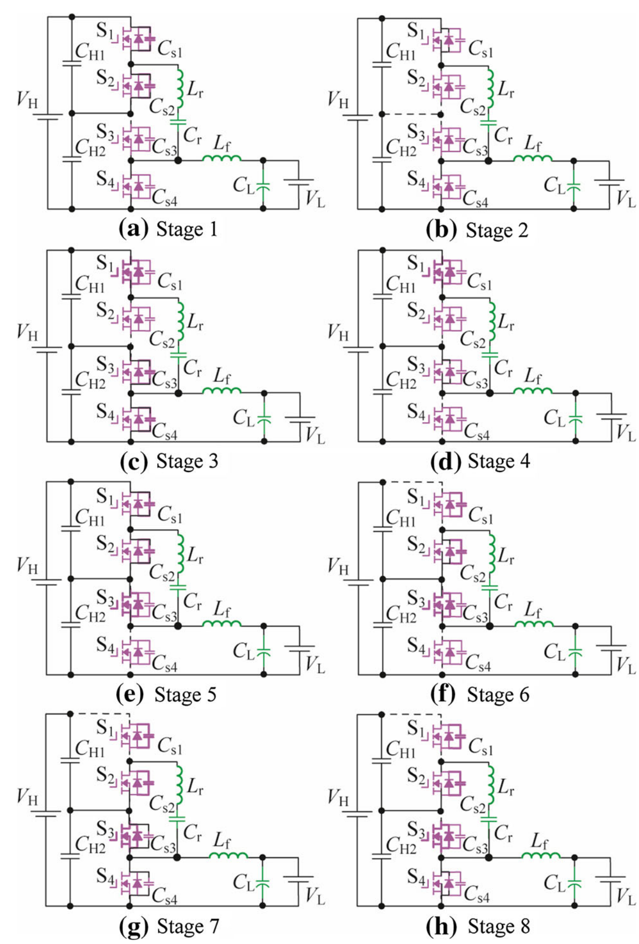

Fig. 3 Equivalent operation circuits of introduced converter

$$i_{L_r}(t) = I_{L_r}(t_1) + \frac{V_H - V_{C_r}}{L_r}(t - t_1) \tag{1}$$

$$i_{L_f}(t) = I_{L_f}(t_1) - \frac{V_L}{L_f}(t - t_1) \tag{2}$$

$$i_x(t) = 0 \tag{3}$$

3) Stage 3: $[t_2 \sim t_3]$

At t_2, S_4 is turned off. The resonant current i_{L_r} remains unchanged due to the short interval and the capacitor C_{s4} is charged while C_{s3} is discharged in a linear way, and the ZVS turn-off of S_4 is achieved.

4) Stage 4: $[t_3 \sim t_4]$

At t_3, the voltage of S_3 reduces to zero and the difference of the currents i_{L_r} and i_{L_f} flows through the anti-parallel diode of S_3. S_3 is turned on with ZVS during this stage. Resonant capacitor C_r is in parallel with C_{H1} through inductor L_r, and i_{L_r} changes with a small slope. i_{L_f} increases linearly. The neutral current i_x equals to the difference of i_{L_r} and i_{L_f}.

$$i_{L_r}(t) = I_{L_r}(t_3) + \frac{V_{C_{H1}} - V_{C_r}}{L_r}(t - t_3) \tag{4}$$

$$i_{L_f}(t) = I_{L_f}(t_3) + \frac{V_{C_{H2}} - V_L}{L_f}(t - t_3) \tag{5}$$

$$i_x(t) = i_{L_f}(t) - i_{L_r}(t) \tag{6}$$

5) Stage 5: $[t_4 \sim t_5]$

At t_4, S_1 is turned off with ZVS. The resonant current i_{L_r} remains unchanged due to the short interval and C_{s1} is charged while C_{s2} is discharged in a linear way.

6) Stage 6: $[t_5 \sim t_6]$

At t_5, the switching voltage of S_2 reduces to zero and i_{L_r} flows through the anti-parallel diode of S_2, to guarantee the ZVS turn-on for S_2 during this stage. L_r is in parallel with C_r. As a result, i_{L_r} decreases linearly. i_{L_f} increases with the same slope as that in stage4. i_x is equal to i_{L_f}, and the currents are given by

$$i_{L_r}(t) = I_{L_r}(t_5) - \frac{V_{C_r}}{L_r}(t - t_5) \tag{7}$$

$$i_{L_f}(t) = I_{L_f}(t_5) + \frac{V_{C_{H2}} - V_L}{L_f}(t - t_5) \tag{8}$$

$$i_x(t) = i_{L_f}(t) \tag{9}$$

7) Stage 7: $[t_6 \sim t_7]$

At t_6, S_3 is turned off with ZVS and C_{s3} is charged while C_{s4} is discharged in a linear way.

8) Stage 8: $[t_7 \sim t_8]$

At t_7, the voltage of C_{s4} reduces to zero and i_{L_f} flows through the anti-parallel diode of S_4. ZVS turn-on for S_4 is ensured in this stage. Resonant capacitor C_r is parallel connected with C_{H2} through inductor L_r, and i_{L_r} changes with a small slope. i_{L_f} decreases with the same slope as that in stage1 and i_x equals to i_{L_r}.

$$i_{L_r}(t) = I_{L_r}(t_7) + \frac{V_{C_{H2}} - V_{C_r}}{L_r}(t - t_7) \tag{10}$$

$$i_{L_r}(t) = I_{L_f}(t_7) - \frac{V_L}{L_f}(t - t_7) \tag{11}$$

$$i_x(t) = i_{L_r}(t) \tag{12}$$

3 Converter performance analysis

3.1 Voltage conversion ratio

By applying the voltage-second balance principle to the filter inductor L_f, it can be derived that

$$V_L = DV_{C_{H2}} \tag{13}$$

Which is to say, the voltage of C_{H2} is proportional to the output voltage V_L. Then with phase-shift (PS) control of a fixed 50% duty cycle, the proposed converter will operate under an unbalanced condition for $V_{C_{H1}}$ and $V_{C_{H2}}$ for most input and output combinations. But with the PWM PPS control method, the duty cycle D can be set by control loop to be

$$D = \frac{2V_L}{V_H} \tag{14}$$

So that

$$V_{C_{H1}} = V_{C_{H2}} = \frac{1}{2}V_H \tag{15}$$

Equation (15) indicates that it is possible for the stacked converter to work in balanced condition for $V_{C_{H1}}$ and $V_{C_{H2}}$ when PPS control is employed. Thus the voltage stress of the power switches $S_1 \sim S_4$ is half of the high-side voltage due to the stack structure and voltage balance mechanism. As a result, low-voltage rated power devices can be used to reduce the conduction losses compared with conventional buck-boost bidirectional converters.

The voltage conversion ratio can be derived by

$$M = \frac{V_L}{V_H} = \frac{D}{2} \tag{16}$$

From (16), it can be concluded that a high step-down or step-up voltage conversion ratio is achieved due to the stack configuration.

3.2 Power transfer characteristics

The phase-shift angle between S_1 and S_3 is defined as φ, which can be employed to control the delivered power and direction. As plotted in Fig. 2a, when S_1 is leading to S_3, φ is defined as positive, which means the power is delivered from the high side to the low side as the buck mode. When φ is negative, the power flow reversely and the converter works at the boost mode.

When the proposed converter works under the balanced condition with PPS control, by applying the voltage-second balance to the resonant inductor L_r, the voltage on the resonant capacitor can be obtained by

$$V_{C_r} = \frac{1}{2} V_H \tag{17}$$

As the range of φ is limited from $-DT_s$ to DT_s, in order to simplify the expression, α is defined as

$$\alpha = \frac{\varphi}{DT_s} \tag{18}$$

According to the charging and discharging balance of the series capacitors in one switching cycle, the expression of i_x is obtained by

$$\frac{1}{T_s}\int_0^{T_s} i_x(t)\mathrm{d}t = 0 \tag{19}$$

From (19) and the analysis in Section 2, the equation of φ is calculated as follows.

$$\varphi^2 - 2D(1-D)T_s\varphi + \frac{2L_r I_o D T_s}{V_H} = 0 \tag{20}$$

where I_o is the average current of the low side.

The delivered power is defined as

$$P = V_L I_o \tag{21}$$

From (18)$\sim$(21), the delivered power in the buck mode can be expressed as

$$P = -\frac{V_L^2\alpha^2}{L_r f_s} + \frac{2(V_H - 2V_L)V_L^2\alpha}{V_H L_r f_s} \tag{22}$$

The expression of the delivered power in the boost mode can be calculated in a similar way. Therefore, in terms of different ranges of the phase-shift angel φ, the delivered power can be calculated by

$$P = \begin{cases} -\dfrac{V_L^2\alpha^2}{L_r f_s} + \dfrac{2(V_H - 2V_L)V_L^2\alpha}{V_H L_r f_s} & 0 \le \alpha \le 1 \\ \dfrac{V_L^2\alpha^2}{L_r f_s} + \dfrac{2(V_H - 2V_L)V_L^2\alpha}{V_H L_r f_s} & -1 \le \alpha \le 0 \end{cases} \tag{23}$$

The relationship of the delivered power and the coefficient α is illustrated in Fig. 4, according to (23) where $V_L = 40\sim56$ V, $V_H = 400$ V, $f_S = 100$ kHz, $L_r = 12.8$ μH.

From Fig. 4, the delivered power curves are totally symmetrical to $\varphi = 0$. The higher the low-side voltage is, the larger the maximum delivered power is. Therefore, the phase-shift angle can be a control freedom to regulate the power flow accurately.

3.3 ZVS soft-switching condition

From the operation analysis in Section 2, during the dead time interval between the turn-off of S_1 and turn-on of S_2, the parasitic capacitors of S_1 and S_2 are charged and discharged by the resonant current as shown in Fig. 3 (Stage 5). C_{s1} is charged by the current of L_r. Due to the very short interval of the stage, it is reasonable to take the current of L_r as a constant value to simplify the analysis. $I_{L_r}(t_4)$ is the current of L_r at t_4, which is derived by

$$I_{L_r}(t_4) \approx \frac{\varphi(1-D)V_H}{2L_r} \tag{24}$$

The drain-source voltage increasing rate of S_1 is limited by its parallel capacitor, and the ZVS turn-off operation for S_1 can be achieved once the following is satisfied

$$C_{s1} \le \frac{I_{L_r}(t_4)t_r}{V_H} = \frac{\varphi(1-D)t_r}{2L_r} \tag{25}$$

where t_r is the rise time of S_1, which can be found in the datasheet.

In order to realize ZVS turn-on for S_1, the voltage of C_{s1} should be discharged totally before the turn-on signal of S_1 comes during Stage 1. As given in Fig. 3 (Stage 1), C_{s1} is charged by $I_{L_r}(t_0)$, which is the current of L_r at t_0. $I_{L_r}(t_0)$ is calculated as follows.

$$I_{L_r}(t_0) \approx -\frac{\varphi D V_H}{2L_r} \tag{26}$$

Once the falling time t_f of S_1 is smaller than the dead time t_d, ZVS turn-on of S_1 can be achieved by satisfying the following

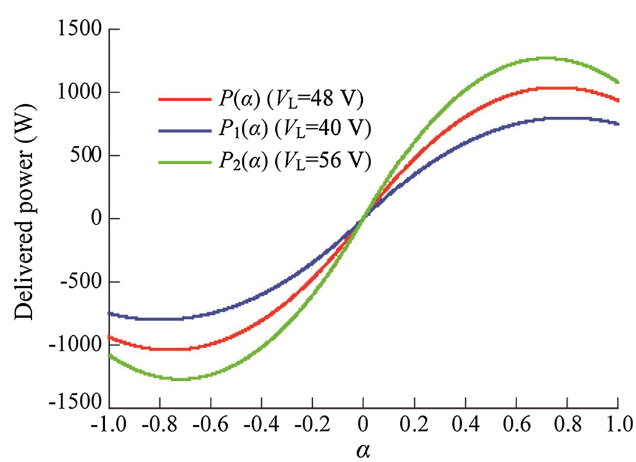

Fig. 4 Relationship between delivered power and coefficient α

$$C_{s1} \leq \frac{|I_{L_r}(t_0)|t_f}{V_H} = \frac{\varphi D t_f}{2L_r} \tag{27}$$

Similar to S_1, ZVS turn-off for S_2, S_3 and S_4 can be achieved by their parallel capacitors when the following are satisfied

$$C_{s2} \leq \frac{I_{L_r}(t_0)t_r}{V_H} = \frac{\varphi D t_r}{2L_r} \tag{28}$$

$$C_{s3} \leq \frac{(I_{L_f}(t_6) - I_{L_r}(t_6))t_r}{V_H} = \left[\frac{I_o}{V_H} + \frac{D(1-D)}{4L_f f_s} + \frac{\varphi D}{2L_r}\right] t_r \tag{29}$$

$$C_{s4} \leq \frac{(I_{L_f}(t_2) - I_{L_r}(t_2))t_r}{V_H} = \left[\frac{I_o}{V_H} - \frac{D(1-D)}{4L_f f_s} - \frac{\varphi(1-D)}{2L_r}\right] t_r \tag{30}$$

C_{s2}, C_{s3} and C_{s4} are charged by $I_{L_r}(t_0)$, $I_{L_f}(t_6) - I_{L_r}(t_6)$, and $I_{L_f}(t_2) - I_{L_r}(t_2)$ respectively.

For the ZVS turn-on, C_{s2}, C_{s3} and C_{s4} are discharged by $I_{L_r}(t_4)$, $I_{L_f}(t_2) - I_{L_r}(t_2)$, and $I_{L_f}(t_6) - I_{L_r}(t_6)$ respectively. The following expressions should be satisfied

$$C_{s2} \leq \frac{I_{L_r}(t_4)t_f}{V_H} = \frac{\varphi(1-D)t_f}{2L_r} \tag{31}$$

$$C_{s3} \leq \frac{(I_{L_f}(t_2) - I_{L_r}(t_2))t_f}{V_H} = \left[\frac{I_o}{V_H} - \frac{D(1-D)}{4L_f f_s} - \frac{\varphi(1-D)}{2L_r}\right] t_f \tag{32}$$

$$C_{s4} \leq \frac{(I_{L_f}(t_6) - I_{L_r}(t_6))t_f}{V_H} = \left[\frac{I_o}{V_H} + \frac{D(1-D)}{4L_f f_s} + \frac{\varphi D}{2L_r}\right] t_f \tag{33}$$

In summary, with the PPS control strategy, ZVS soft switching performance can be achieved without adding extra power switches, which simplifies the circuit configuration.

4 Phase shift angle selection analysis

According to the charging and discharging balance of the series capacitors in one switching cycle, the equation of φ has been obtained in (20). The value of φ can be calculated by

$$\begin{aligned} \varphi_1 &= D(1-D)T_s + \sqrt{D^2(1-D)^2 T_s^2 - \frac{2I_o L_r D T_s}{V_H}} \\ \varphi_2 &= D(1-D)T_s - \sqrt{D^2(1-D)^2 T_s^2 - \frac{2I_o L_r D T_s}{V_H}} \end{aligned} \tag{34}$$

Both φ_1 and φ_2 can be employed to achieve the required delivered power, but with different current performance of the circuit. According the analysis in Sections 2 and 3, the RMS currents of the resonant inductor can be calculated by

$$I_{RMS\_L_r} = \sqrt{\frac{-V_H^2 f_s \varphi^3 + 3D(1-D)V_H^2 \varphi^2}{12L_r^2}} \tag{35}$$

The curves of $I_{RMS\_L_r}$ under φ_1 and φ_2 are illustrated in Fig. 5, where $I_{RMS\_L_r}$ is larger with φ_1 compared with that with φ_2. Furthermore, with the decreasing of L_r, the current difference is significant. A large $I_{RMS\_L_r}$ means high conduction losses, and the size of the inductor would be larger. Therefore, it is preferred to select φ_2 as the phase-shift angle to regulate the power flow.

5 Experimental verifications

A 1 kW prototype is built and tested to verify the effectiveness of the introduced bidirectional converter. The circuit parameters are listed in Table 1.

Due to the stacked construction and voltage balance mechanism, 300 V rated MOSFETs can be used to realize 400 V input voltage operation. The filter parameters of L_f and C_L can be calculated exactly the same as that in a buck/boost converter. The resonant inductor is determined by the maximum delivered power illustrated in (23). Generally, the resonant capacitor C_r should be relatively large to suppress its ripple voltage, 5% is a practical value for the voltage ripple and C_r is selected to be 4.7 μF for this design.

The control block diagram of the proposed converter is introduced in Fig. 6. The PWM control loop is employed to balance $V_{C_{H1}}$ and $V_{C_{H2}}$ voltage. Moreover, the output filter inductor current i_L is adopted for the phase shift control loop to achieve the charge/discharge current management. The digital voltage controlled oscillator (DVCO) is used to generate the phase-shift angle φ_2. With this solution, the duty cycle regulation and the phase shift control are decoupled and easy for implementation by digital signal processors (DSP).

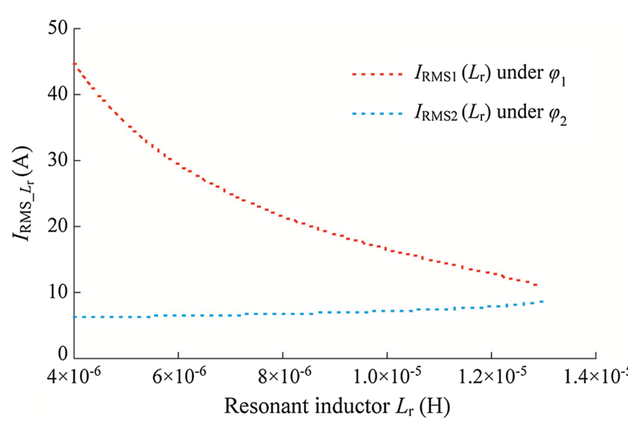

Fig. 5 RMS currents of resonant inductor L_r under φ_1 and φ_2 (P = 1 kW)

Table 1 Parameters of tested prototype

Parameters	Value
Power level P_{out}	1 kW
High-side voltage V_H	400 V
Low-side voltage V_L	40 ~ 56 V
Switching frequency f_s	100 kHz
Main switches $S_1 \sim S_4$	IRFP4242PBF
Divider capacitors $C_{H1} \sim C_{H2}$	470 μF
Resonant inductor L_r	12.8 μH
Resonant capacitor C_r	4.7 μF
Filter inductor L_f	20 μH
Output capacitor C_L	220 μF

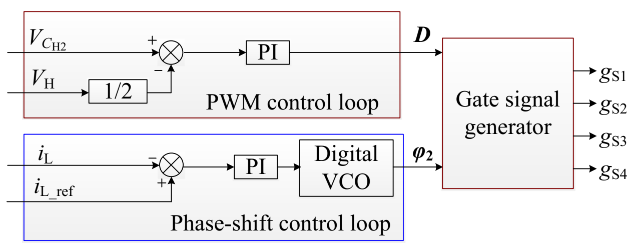

Fig. 6 Control loop for proposed converter

The experimental results of the proposed converter in the buck mode at 1 kW load are shown in Fig. 7. The driving signals of the power switches are illustrated in Fig. 7a, where S_1, S_2 and S_3, S_4 operate complementarily respectively. The signal of S_1 is leading of that of S_3, which shows the circuit works at buck mode as analyzed in Section 2. The voltage and current waveforms of L_r are implied in Fig. 7b. When S_1 and S_3 turn on/off synchronously, the slope of i_{L_r} is small because V_{L_r} equals to the difference between V_{C_r} and the voltage of the series capacitors, while the value of V_{C_r} is almost the same as $V_{C_{H1}}$ or $V_{C_{H2}}$. Meanwhile, i_{L_r} increases linearly when S_1 and S_4 are turned on and L_r is charged by the voltage difference between the high voltage source and C_r. L_r is discharged by C_r when S_2 and S_3 are turned on, leading to the decreasing of i_{L_r} with the same slope. In addition, the waveforms of V_{L_f} and i_{L_f} are shown in Fig. 7c. L_f is discharged when S_4 is in the turn-off state, and charged by the low voltage source when S_4 is ON. The voltage balance of the series capacitors are proved in Fig. 7d, where both of $V_{C_{H1}}$ and $V_{C_{H2}}$ are half of the high-side voltage. V_{L_r} also equals to half of the high-side voltage, which is consistent with the previous analysis.

ZVS soft switching performance of the power switches in buck mode at full load are given in Fig. 8. From Fig. 8, ZVS turn-on and turn-off for all of the switches are implemented. Moreover, the voltage stress is only half of the high-side voltage, promoting the utilization of switches with low conduction losses.

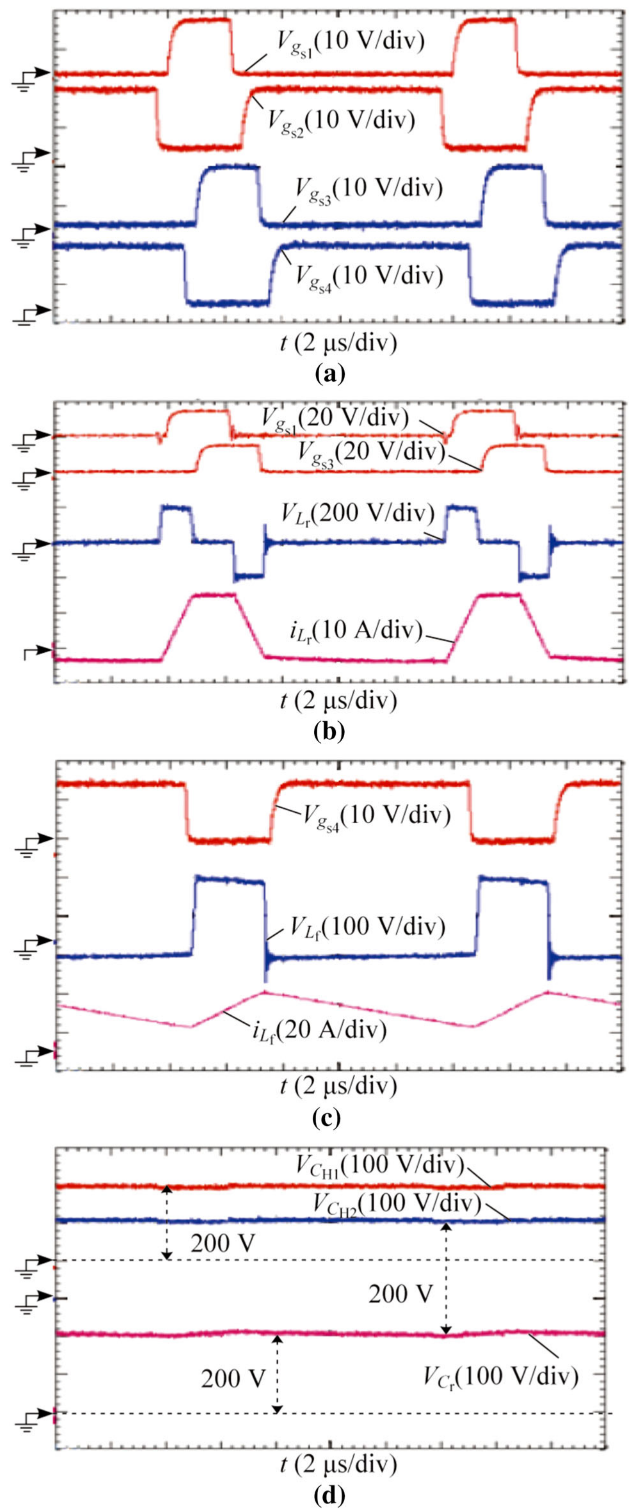

Fig. 7 Experimental results in buck mode

Figures 9 and 10 demonstrate the circuit performance in the boost mode at full load. The driving signals of the power switches in the boost mode is almost the same as those in the buck mode, expect for that S_3 has the leading phase. Consequently, the phase-shift angle is verified to be a control freedom for the power regulation. The voltage and current waveforms of L_r and L_f are illustrated in Figs. 8b, c, where the current waveforms are reversed

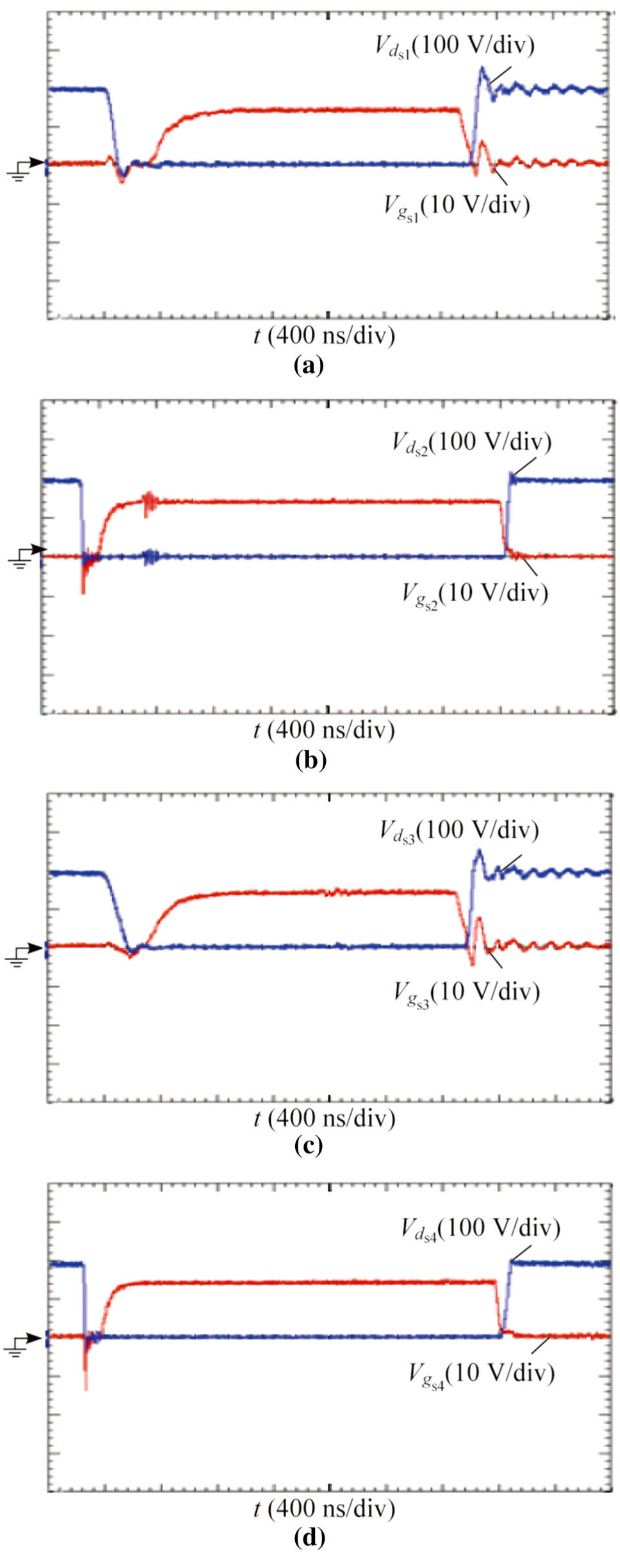

Fig. 8 ZVS soft switching performance in buck mode

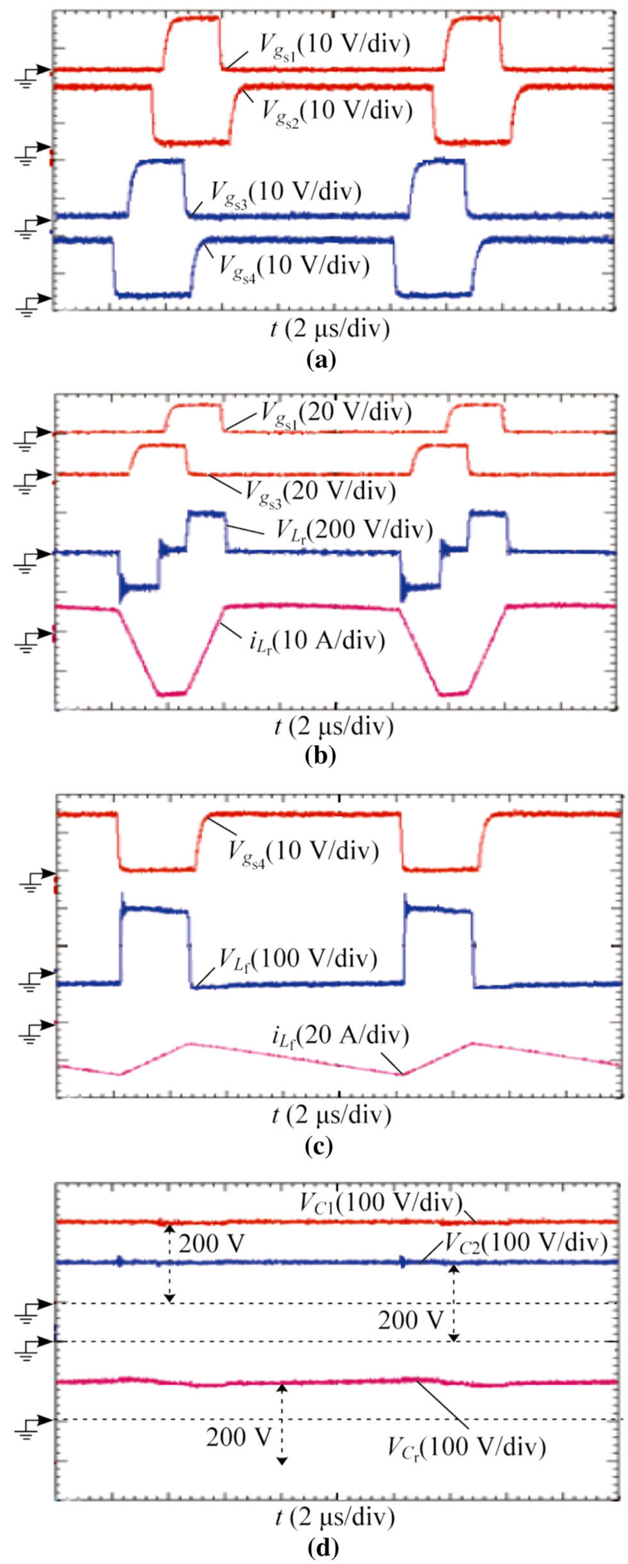

Fig. 9 Experimental results in boost mode

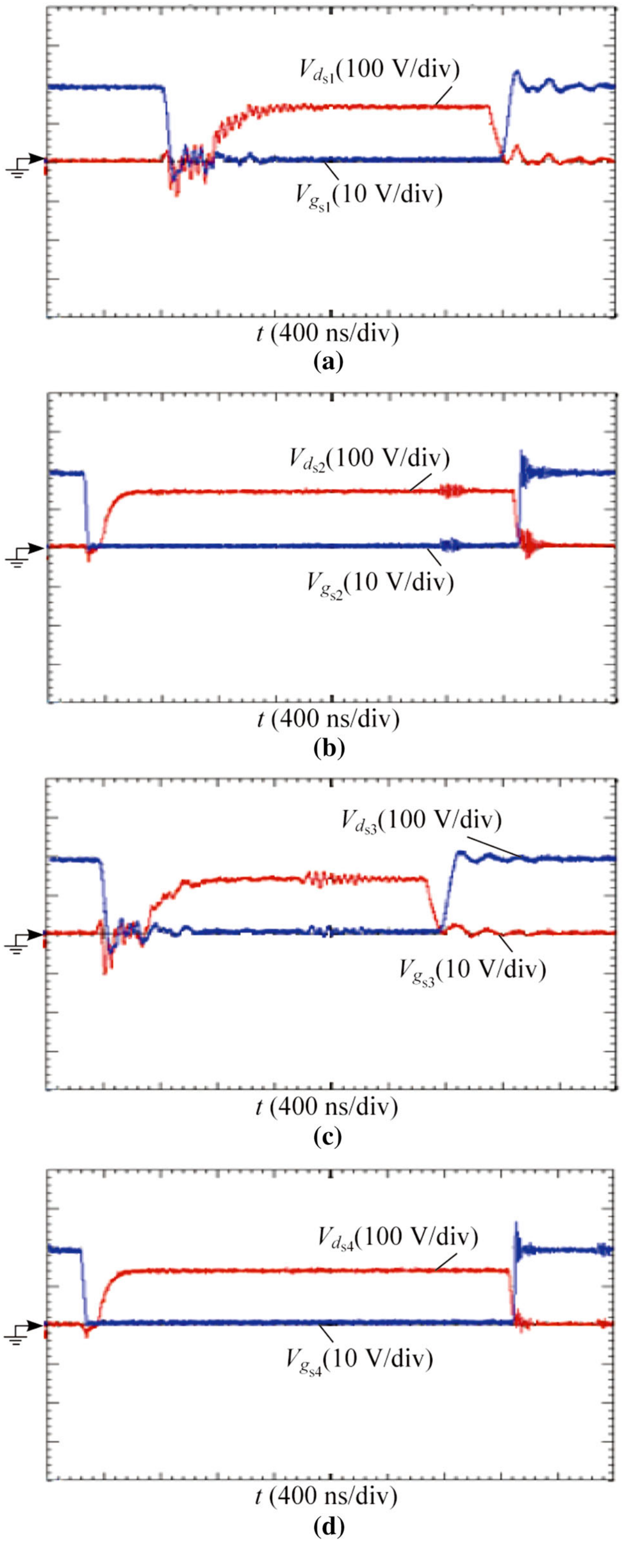

Fig. 10 ZVS soft switching performance in boost mode

compared with that in the buck mode. Figure 9d implies that the high-side voltage is halved equally by the voltage balance mechanism. Moreover, ZVS soft switching operations are achieved in the boost mode as shown in Fig. 10.

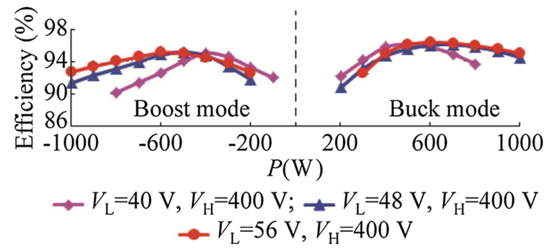

Fig. 11 Measured efficiency of proposed converter

The measured efficiency of the proposed converter at different load conditions is plotted in Fig. 11. In the buck mode, the maximum efficiency is about 96%, and the full load efficiency is about 94.5% when $V_H = 400$ V and $V_L = 48$ V. When the low-side voltage increases to 56 V, the maximum efficiency is about 96.3%. In the boost mode, when $V_L = 48$ V and $V_H = 400$ V, the efficiency is 91.3% at full load, and the maximum efficiency is 94.7%. The efficiency reaches 95% when $V_L = 56$ V in the boost mode. The efficiency in the buck or boost modes decreased a little when $V_L = 40$ V due to the relatively larger conduction losses.

6 Conclusion

A stacked bidirectional DC-DC converter with PPS control has been introduced to provide an advanced solution for the large voltage conversion ratio applications. By employing PPS control scheme, high and low sides voltages are matched, the divider capacitors voltages are balanced, and flexible power flow regulation is achieved. Furthermore, ZVS soft switching is ensured to reduce the switching losses, and the stacked structure suppresses the switch voltage stress to only half of the high-side voltage. In addition, the extremely narrow duty cycle is extended compared with the conventional buck-boost converters. At last, a 1 kW prototype converter has been built to verify the effectiveness of the stacked converter, where the experimental results have illustrated that the proposed converter is a competitive candidate for the non-isolated high step-up/step-down bidirectional DC-DC conversion systems.

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