

# Digital and Analog Electronics for an autonomous, deep-sea, Gamma Ray Burst Neutrino prototype detector

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**Abstract.** GRBNeT is a Gamma Ray Burst Neutrino Telescope made of autonomously operated arrays of deep-sea light detectors, anchored to the sea-bed without any cabled connection to the shore. This paper presents the digital and analog electronics that we have designed and developed for the GRBNeT prototype. We describe the requirements for these electronics and present their design and functionality. We present low-power analog electronics for the PMTs utilized in the GRBNeT prototype and the FPGA based digital system for data selection and storage. We conclude with preliminary performance measurements of the electronics systems for the GRBNeT prototype.

## 1. Introduction

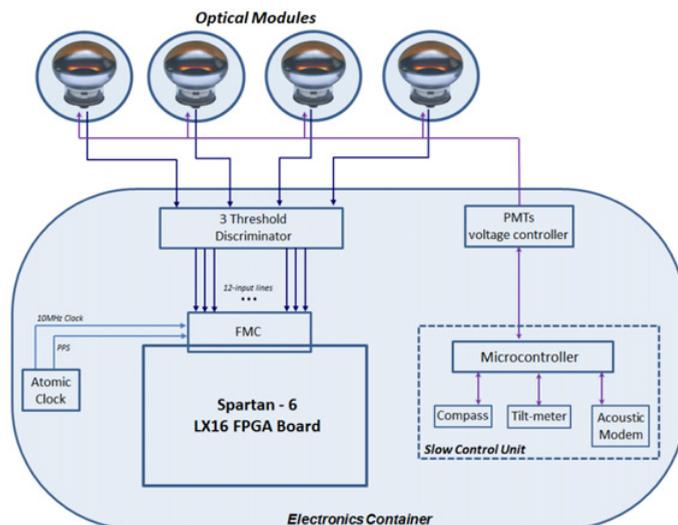
*GRBNeT* is a Gamma Ray Burst Neutrino Telescope that involves the development, construction and testing of a prototype for an autonomous array of deep-sea detectors, capable to operate continuously for a prolonged period of time, anchored at the sea bed without any cabled connection to the shore. A few tens of such arrays, separated by 300–400 meters from each other, will be able to cover a volume of  $\sim 10 \text{ km}^3$  in the deep-sea, down to 5 km depth, thus providing a sufficiently large observational volume, capable of detecting high-energy neutrinos originating from Gamma Ray Bursts (GRBs).

In this paper we present the digital and analog electronics of the Data Acquisition (DAQ) and readout system for the *GRBNeT* prototype. This prototype consists of four Cherenkov light detectors, based on photomultiplier tubes (PMTs) inside a pressure resistant glass sphere. Immersed in the deep-sea these light detectors will be operated, and their analog signals will be transmitted to a fifth glass sphere, which houses the data acquisition and the readout system of the detector. One of the key features of *GRBNeT* is its ability to operate autonomously, without the need of a submarine cable to supply the necessary power from the shore. This autonomy is achieved by utilizing locally a cluster of batteries, also housed in glass spheres that provide the entire system with power. The main advantage of this feature is the cost reduction by omitting the submarine power cables to shore, while on the other hand, it creates a restriction to the detector's power consumption.

The design of the DAQ architecture demands low power analog electronics and it is well suited for a low power FPGA implementation. The Xilinx Spartan-6 FPGA LX16 evaluation board is targeted to implement and to validate the functionalities of the DAQ design. Moreover, a PIC microcontroller

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**Figure 1.** Block diagram of the detector unit. The prototype consists of two such units, operating independently of each other.

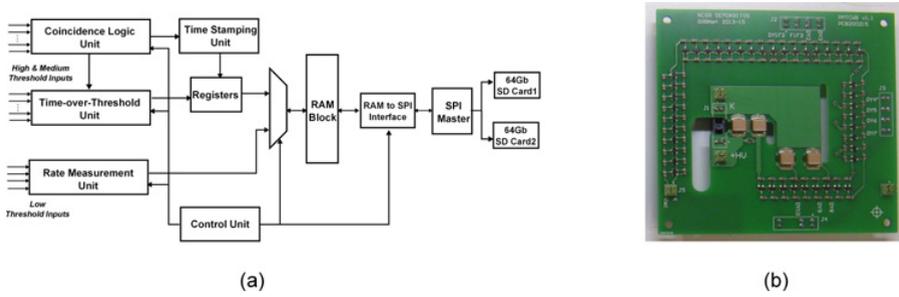
is used to handle the slow-control tasks, thus partitioning the system's tasks to achieve low power dissipation.

## 2. Design description

The main functions of the DAQ system and the readout electronics are the following: i) detect events of interest, based on a digital analysis of the light detectors' digitized signals, ii) measure the temporal and spatial characteristics of selected events (i.e. duration, intensity etc.), iii) use an atomic clock as an autonomous, free running, reference clock for synchronicity and time-stamping of each event, iv) store these results locally to permanent data storage, in order to be analyzed after retrieval, and v) collect and store operational data, as well as data from auxiliary devices such as orientation sensitive devices (i.e. compass, tiltmeter etc.). Figure 1 depicts the detector unit with the block diagram of the electronics container, which consists of both analog and digital electronics. The detection unit utilizes a set of 4 Optical Modules (OMs). Each OM consists of a 17-inch diameter Benthos glass-sphere and contains a single R8055 Hamamatsu PMT of 13-inch diameter.

### 2.1 Analog electronics

In order to maintain the power consumption for the PMT bases at a minimum, instead of a resistive divider design, we have developed a Cockroft-Walton (CW) voltage multiplier (Fig. 2b) and a High Voltage (HV) control unit, that utilizes ultra-low power microcontrollers. In each OM the HV-controller drives the Cockroft Walton (CW) voltage multiplier to produce the desired voltage for the specific PMT. When a PMT detects Cherenkov light it produces an analog pulse, whose characteristics (i.e. duration, height) depend on the intensity of the light detected. Each OM transmits the analog signal from its PMT to a 3 threshold-level discriminator. A single discriminator unit implements 4 independent input channels, one for each OM, where the analog signals are compared to three distinct threshold levels (low, medium and high). When a threshold level is crossed the discriminator outputs a leading edge, followed by a trailing edge that lasts for as long as the analog signal remains above that specific threshold. The



**Figure 2.** (a) Block diagram of the FPGA design, (b) Cockcroft-Walton board.

discriminator's digitized outputs enter as input to the digital circuit implemented on the FPGA board. Since each PMT uses a dedicated 3 threshold-level discriminator, with 4 PMTs operated in a cluster, a total of 12 input lines are produced for the FPGA design.

## 2.2 FPGA architecture

The Data Acquisition (DAQ) hardware system, in this prototype version, of the *GRBN<sub>e</sub>T* module consists of the Spartan-6 LX16 Evaluation board [2] and the Microsemi SA.45 s Chip Scale Atomic Clock [3]. The atomic clock provides the system with a stable, low-jitter reference clock of 10 MHz and a Pulse-Per-Second (PPS) signal. This clock is free-running for the duration of the deployment and is used by the FPGA to derive the other clock domains that will be used by the design.

Figure 2a shows the block diagram of the FPGA architecture. The main task of the design implemented on the Spartan-6 FPGA is to detect and record events that could be related to high-energy neutrinos. The selection of such events is based on the inputs received by the 4 PMTs of the cluster and it is performed by the *Coincidence Logic Unit (CLU)*. The *CLU* searches for PMT signals that, after passing a threshold, coincide within a fixed time frame. These coincidences are considered as events of interest and therefore, when detected by the *CLU* a trigger is generated in order to save all the corresponding PMT data to permanent local storage.

In this prototype, any PMT signal passing at least the programmable threshold level will be considered in the search for coincidences. Whenever this occurs a 200 ns time-window is generated. When a second PMT signal, that has passed the same threshold, is detected within the time-window a 2-fold coincidence occurs. When a 3-fold coincidence occurs it triggers the expansion of the time window for a subsequent period, a post-trigger window, of an extra 100 ns. At the end of the expanded 300 ns time-window, the data of all 4 PMTs are stored to the RAM block.

The data of interest for each detected event are the length of each PMT pulse and the timing information regarding when the event has been detected. To determine the length of a PMT pulse we measure the Time-over-Threshold (ToT), the time duration for which the pulse remains above the specific threshold. This is performed by the *ToT Unit* that is implemented in the Spartan-6 according to [4].

As we mentioned previously, there are 3 input lines per PMT that correspond to the three threshold levels. The medium and the high threshold are taken into account by the *CLU* in order to detect events of interest, while the low threshold level is used by the Rate Measurements Unit. The purpose of this unit is to measure the rate of the pulses generated by each PMT. The result of these measurements will also be recorded, regardless of coincidences, providing additional information during the off-line data analysis to determine the operational functionality of each PMT and to monitor the pulse rates of each PMT.

The data gathered from the previous units are temporarily stored to a RAM block, in order to be permanently stored to a flash memory. Two high speed 64 Gb SD memory cards are used for this purpose, communicating with the FPGA via the SPI protocol.

The *Control Unit* handles the synchronization and the control signals of the FPGA design. It provides all the parameters to the design's components, it is responsible for all data and command handling, and it periodically initiates the data storage from the RAM block to the SD cards.

### 2.3 Slow Control Unit

Throughout the deployment a number of different parameters are monitored, such as the PMTs voltage levels, the detector's orientation and the temperature inside the glass sphere that houses all the electronic components. These tasks are performed by the *Slow Control Unit* (SCU) by utilizing a PIC microcontroller that communicates via the I2C protocol with a compass and a tiltmeter in order to record changes in the detector's orientation. Moreover, the SCU is directly connected to the PMTs voltage controller in order to control and monitor the voltages. The slow control data gathered by the microcontroller are stored periodically and independently of the events detected by the FPGA design.

## 3. Implementation analysis and tests

The presented design was tested at a hardware level targeting the Spartan-6 LX16 evaluation board, utilizing initially a function generator to produce the incoming pulses and subsequently performing test with the actual PMTs. The maximum operating frequency of the FPGA is 200 MHz, but in order to reduce the power consumption slower clock domains are also used, depending on the operation of the various design components. To further minimize the power consumption the design has incorporated low power techniques, such as avoiding free rolling counters and implementing clock gating techniques to keep several components of the design inactive for the time period where there is no PMT activity. As a result, the total power consumption of the design was reduced to 375 mW for a typical operational scenario, of which 93 mW is the quiescent power, and the dynamic power equals to 282 mW.

## 4. Conclusions

This paper has presented the digital and analog electronics of the DAQ system for an autonomous deep-sea Gamma Ray Burst Neutrino Telescope prototype. The design features programmable functionality based on a scalable design, while maintaining a low power consumption with the ability to operate autonomously utilizing a local cluster of batteries. The FPGA implementation shows the benefits of the presented architecture and field experiments are expected to provide measurements for the design's parameter tuning to optimize its performance.

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