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RESEARCH ARTICLE - ELECTRICAL ENGINEERING

Minimization of CNTFET Ternary Combinational Circuits Using Negation of Literals Technique

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Abstract A multi-threshold design can be achieved by employing carbon nanotubes (CNTs) with different diameters, as the threshold voltage of the carbon nanotube field effect transistor (CNTFET) depends on the diameter of the CNT. In this paper, this feature is exploited to design ternary logic circuits for achieving improved performance. We presented new design for CNTFET-based ternary combinational circuits such as half adder, full adder, half subtractor, full subtractor and comparator using negation of literals technique. Extensive simulation results using Synopsis HSPICE simulator demonstrate that using new technique 5–145 times improvement in power delay product can be achieved with reduced gate count compared to the existing ternary–binary combinational gate design.

Keywords Adder · Chiralities · CNTFET · Comparator · Decoder · Hspice · Multi-valued logic · Power delay product · Subtractor · Ternary

الخلاصة

يمكن تحقيق التصميم متعدد العتبة من خلال توظيف أنابيب الكربون النانونية ذات الأقطار المختلفة، حيث إن جهد العتبة لترانزستور تأثير مجال أنابيب الكربون النانونية CNTFET يعتمد على قطر أنابيب الكربون النانونية. وفي هذه الورقة العلمية، تم استغلال هذه الميزة لتصميم دوائر المنطق الثلاثية لتحقيق الأداء المحسن. فقدمنا تصميما جديدا لترانزستور تأثير مجال أنابيب الكربون النانونية (CNTFET) مستنداً إلى الدوائر التوافقية الثلاثية مثل نصف المضيف، والمضيف الكامل، ونصف التراكتور الفرعي، والتراكتور الفرعي الكامل والمقارن باستخدام إبطال تقنية الحرفية. وتوضح نتائج المحاكاة واسعة النطاق باستخدام محاكي خلاصة HSPICE أنه باستخدام التقنية الجديدة يمكن تحقيق تحسن من 5 إلى 145 مرة في منتج تأخير القوة مع انخفاض عد بوابة مقارنة بتصميم البوابة التوافقية الثلاثي - الثنائي القائم.

Abbreviations

MVL	Multi-valued logic
CNT	Carbon nanotube
CNTFET	Carbon nanotube field effect transistor
STI	Simple ternary inverter
PTI	Positive ternary inverter
NTI	Negative ternary inverter
FA	Full adder
HA	Half adder
PDP	Power delay product

1 Introduction

Multi-valued logic replaces the classical Boolean characterization of variables with either finitely or infinitely many values such as ternary logic [1] or fuzzy logic, since it reduces the number of signals involved in the communication increasing their information content, thereby reducing complexity of interconnects and chip area [2–4]. Ultimate goal of using multi-valued logic over binary logic is that (i) Chip area can

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be reduced by transmitting more MVL information through each wire than binary (ii) Complexity of the circuit may be decreased since each MVL element can process more information than binary element and (iii) speed of serial information transmission can be faster since the transmitted information p.u time is increased. Ternary circuits may be of more theoretical significance than other MVL logics as (i) 3 is the smaller radix greater than binary and ternary functions and circuits have the simpler form and construction, (ii) the product of radix and the number of signals have impact on the cost or complexity of MVL circuits, ternary circuits will be more economical, (iii) the same hardware of balanced ternary logic (1, 0, −1) is used for addition and subtraction, and (iv) 3 is not an integral power of 2, research on ternary logic may reveal design techniques that are overlooked in the study of binary or other MVL logic.

By employing ternary logic, serial and serial parallel arithmetic operations can be carried out faster. In many cases, MVL logic has been combined with binary logic to enhance the performance of CMOS technologies [5]. Three kinds of MVL circuits are current-mode, voltage-mode and mixed-mode or hybrid mode. Several current-mode MVL circuits have been fabricated which show better performances compared to binary circuits [6–8]. But the power consumption of current mode circuits is high due to their inherent nature of constant current flow during the operation. Voltage mode circuits consume a large current only during the logic level switching, thus offering less power consumption.

The multi-valued logic design by itself is not enough in nanotechnology for speed of power improvements needed in digital systems, as a result new devices and circuits have been explored to replace silicon in nanoscale transistors. Among all, CNTFET is a promising alternative to replace conventional devices for low power and high performance design, due to its ballistic transport and low off current properties [9–13]. The multi-threshold design depends on the transistor body effects that apply different bias voltages to the bulk terminal of the transistors. As the threshold voltage of a CNTFET is determined by the CNT diameter, a multi-threshold design can be achieved by employing CNTs with different diameters in the CNTFET model.

The scope of this paper is to implement novel multi-valued logic design based on multi-threshold CNTFETs to explore the possibilities and advantages in realizing CNTFET circuits with reduced T-gates by employing negation of literals technique. In this paper, new design for CNTFET combinational circuits is proposed, described and assessed. Extensive simulation results using Synopsys HSPICE simulator demonstrate significant advantages of proposed design in terms of speed and power consumption compared with existing multi-valued logic design.

2 Ternary Logic Operation

To maintain the Moore's exponential growth, the IC industry must solve many problems, importantly interconnection problem, both on-chip and between chips. The reason being that the silicon area used for interconnections may be greater than that used for the active logic elements [3]. One of the best solutions for these interconnection problems is the use of circuits with more than two levels. If a third value is introduced to the binary logic function, the resultant is the ternary logic function. Using ternary logic, simplicity and energy efficiency in digital design can be achieved as it reduces the complexity of interconnects and chip area and in turn the power delay. Better utilization of transmission channels can be achieved because of the higher information content carried by each line. By employing ternary logic, serial and serial-parallel arithmetic operations can be carried out faster. Let 0, 1 and 2 be the ternary values to represent false, undefined and true conditions, respectively. Any ternary function $f(x)$ of n variable $(X_1, X_2 \ldots X_n)$ is defined as a logic function mapping $\{0, 1, 2\}^n$ to $\{0, 1, 2\}$. The basic operations of ternary logic can be defined as:

$$X_i + X_j = \max\{X_i, X_j\} \tag{1}$$

$$X_i \bullet X_j = \min\{X_i, X_j\} \tag{2}$$

$$\overline{X_i} = 2 - X_i \tag{3}$$

The basic ternary logic gates are designed according to the convention defined by Eqs. (1–3). In ternary logic, there exist 3^{3^n} modal functions and 3^n combinations, where n is a variable. When $n = 1$, we have one-variable functions $f(x)$, and there are $3^{3^1} = 27$ modal functions called Literals. If $n = 2$, there are $3^{3^2} = 19{,}683$ two variable functions and if $n = 3$ there are $3^{3^3} = 7{,}625{,}597{,}484{,}987$ three variable functions. Literal is denoted by $X_i^{a_i}$ where $a_i = 0, 1, 2, 01, 02$ and 12 defined as given below,

$$X_i = \begin{cases} 0 & \text{if } X \neq i \\ 2 & \text{if } X = i \end{cases} \quad \text{where} \quad i = 0, 1 \,\&\, 2 \tag{4}$$

$$X_{01} = X_0 + X_1 \tag{5}$$

$$X_{12} = X_1 + X_2 \tag{6}$$

$$X_{02} = X_0 + X_2 \tag{7}$$

$$X_{01} \bullet X_{12} = X_1 \tag{8}$$

$$X_{01} \bullet X_{02} = X_0 \tag{9}$$

$$X_{02} \bullet X_{12} = X_2 \tag{10}$$

$$X_0 + X_1 + X_2 = 2 \tag{11}$$

In any VLSI circuit, 70 % of the area is devoted to interconnection, 20 % to insulation and 10 % to devices [14]. This paper mainly focused on minimization of representations of combinational logic functions with reduced number of devices using the negation of literals approach. The comple-

ment or negation of literals (X_i) gives the following observed Eqs. (14–18) which are helpful in reduction of ternary gates during implementation, thereby the power delay product can be substantially reduced and is defined as below

$$\text{COM}(X_i) \text{ or } \text{NEG}(X_i) = X_i = \begin{cases} 0 & \text{if } X = i \\ 2 & \text{if } X \neq i \end{cases} \tag{12}$$

$$X_2 = \overline{X_{01}} \ \ \& \ \ X_{01} = \overline{X_2} \tag{13}$$

$$X_1 = \overline{X_{02}} \ \ \& \ \ X_{02} = \overline{X_1} \tag{14}$$

$$X_2 = \overline{X_{01}} \ \ \& \ \ X_{01} = \overline{X_0} \tag{15}$$

$$\overline{0} = 2 \ \ \& \ \ \overline{2} = 0 \tag{16}$$

For supply voltage of 0.9 V, three levels of ternary system are defined as: logic 0—ground potential, logic 1—0.45 V and logic 2—0.9 V.

3 Carbon Nanotube Field Effect Transistor

Carbon nanotubes (CNTs) were discovered in 1991 by S. Iijima, having a cylindrical structure formed by one or more concentric crystalline layers of carbon atoms in a honey comb lattice arrangement [15,16]. Based on the number of concentric layers of carbon atoms, CNTs are classified into single walled CNT (SWCNT) if one layer is present and Multi-walled CNT (MWCNT) if two or more layers are present [17]. In MWCNT, the concentric shell can differ in their chirality and may consist of both metallic and semiconducting tubes, where the metallic shells may negate some of the semiconducting properties. As a consequence, the number of layers and physical features are difficult to control [18] leading to limited use in electronics. In SWCNT, though the researchers face a number of problems in generating it with required characteristics, it draws much academic interest due to its unique feature [19]. In terms of the electrical conductivity, SWCNT can be either metallic with zero band gap or semiconducting with finite band gap due to its chiral number (n_1, n_2) that defines the form of position of the carbon atoms along a CNT. Electronic circuit designers utilize semiconducting SWCNT as the channel of the carbon nanotube field effect transistor (CNTFET) which was first fabricated by Tans et al. in 1998 [20].

The current–voltage (I–V) characteristics of the CNTFET are similar to the MOSFET's [21]. Like MOSFETs, CNTFETs also have N-type and P-type devices. The advantage of CNTFETs over MOSFETs is that the P-type and N-type CNTFETs with the same device size have the same mobility, thereby simplifies the process of transistor scaling, especially in complex circuits using large number of transistors. Furthermore, circuits designed using CNTFETs are faster and have lower average power consumption as compared to MOSFET-based designs [22,23]. Another great advantage of CNTFET over MOSFET is that the threshold voltage of CNTFET is decided by the appropriate diameter of the CNTs used. This makes CNTFET more flexible than the MOSFET for digital circuit design. As the threshold voltage (the voltage required to turn on the transistor) of the CNTFET is determined by the diameter of the CNT, a multi-threshold design can be achieved by employing CNTs with different diameters. The diameter of the CNT can be calculated as:

$$D_{\text{CNT}} = \frac{\sqrt{3}a_o}{\pi}\sqrt{n_1^2 + n_1 n_2 + n_2^2} \tag{17}$$

where $a_o = 0.144$ nm is the inter-atomic distance and the threshold voltage of the intrinsic CNT is given by

$$V_{\text{th}} = \frac{\sqrt{3}}{3}\frac{aV_\pi}{eD_{\text{CNT}}} \tag{18}$$

where $a = 2.49$ A is the carbon to carbon atomic distance, $V_\pi = 3.033$ eV is the carbon π–π bond energy in the tight binding model and e is the unit electron charge. Thus, the threshold voltage of the CNT is inversely proportional to the diameter of the CNT and in turn the chiral vector. The chiralities of the CNTs used for modeling of CNTFETs for ternary logic circuits are (19, 0), (13, 0) and (10, 0) with diameters 1.487, 0.783 and 1.018 nm whose threshold voltages are 0.293, 0.428 and 0.557 V, respectively. In this paper, we use a multi-diameter CNTFET-based design for the implementation of ternary combinational circuits.

4 Circuit Level Implementation of Ternary Logic

A compact SPICE model including non-idealities is used for simulations which has been designed for unipolar, MOSFET-like CNTFET based circuits, also considers Schottky Barrier Effects, Parasitics, including CNT, Source/Drain, and Gate resistances and capacitances, and CNT Charge Screening Effects. Table 1 shows the parameters of the CNTFET model used for designing ternary circuits and their values with brief description.

HSPICE simulator has been used to simulate the proposed ternary-logic-based combinational circuits, such as half adder, full adder, half subtractor, full subtractor and comparator. The threshold voltages of CNTFETs used in the circuits are shown in Table 2.

4.1 Ternary Gates or T-Gates

A complementary CNTFET network can be used for ternary logic circuits design for achieving good performance and lower power consumption, and also to avoid the use of large resistors in the circuits which may lead to high-power dissipation. Ultimately, size and area can be reduced by avoiding

Table 1 CNTFET model parameters

Parameter	Description	Value
L_{ch}	Physical channel length	32 nm
L_{geff}	The mean free path in the intrinsic CNT channel	100 nm
L_{ss}	The length of doped CNT source side extension region	32 nm
L_{dd}	The length of doped CNT drain side extension region	32 nm
K_{gate}	The dielectric constant of high-k top gate dielectric material	16
n_1, n_2	The chirality of the tube	19, 0
T_{ox}	The thickness of high-k top gate dielectric material	4 nm
C_{sub}	The coupling capacitance between the channel region and the substrate	20 pF/m
K_{ox}	Gate dielectric constant (HfO_2)	16
V_{DD}	Supply voltage	1 V
E_f	The Fermi level of the doped S/D tube	0.6 eV
H_{ox}	The gate dielectric thickness between the SWCNT center and gate	4 nm

Table 2 Threshold voltages of CNT with different chiralities

Chirality (n_1, n_2)	Diameter (nm)	Threshold voltage (V)
(19, 0)	1.487	0.293
(10, 0)	0.783	0.557
(13, 0)	1.018	0.428

the large resistors. The fundamental gates in the digital systems design are the inverter, the NOR gate, and the NAND gate. Figure 1 shows the symbols of ternary gates. The basic function of ternary NAND and NOR gates is defined by [24] as follows:

$$Y_{NAND} = \overline{\text{Min}\{X_1, X_2\}} \tag{19}$$

$$Y_{NOR} = \overline{\text{Max}\{X_1, X_2\}} \tag{20}$$

There are three inverters in the ternary inverter systems which are STI (Standard Ternary Inverter), PTI (Positive Ternary Inverter) and NTI (Negative Ternary Inverter) [4]. Firstly, CNTFET-based ternary inverter logic design has been proposed by Raychowdhury et al. [25] which consists of two CNTFETs with resistive pull-ups. The values of two resistors (usually 100 MΩ or greater) used are too large to be integrated into CNTFET technology.

The schematic of CNTFET-based STI (Simple Ternary Inverter) is shown in Fig. 2. It consists of 3 NCNTFETs and 3 PCNTFETs. The chiralities of the CNTs used in T_3, T_4, and T_6 are (13, 0), (19, 0) and (10, 0), respectively. From Eq. (1),

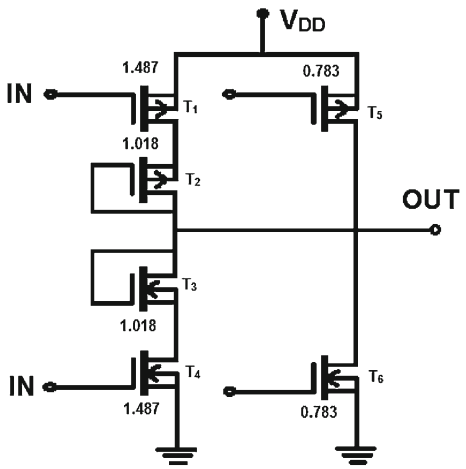
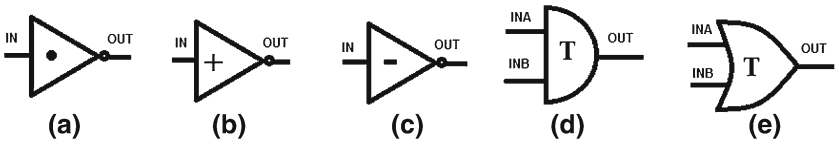


Fig. 2 Structure of STI

the diameters of T_3, T_4, and T_6 are 1.018, 1.487 and 0.783 nm, respectively. Therefore from Eq. (2), the threshold voltages of T_3, T_4, and T_6 are 0.428, 0.293 and 0.559 V, respectively. Similarly, the threshold voltages of T_1, T_2 and T_5 are - 0.293, −0.428 and −0.559 V, respectively. When the input voltage changes from low to high at 0.9 V supply, initially the input voltage is less than 300 mV that turns both T_1, T_5 ON and T_4, T_6 OFF and thereby the output voltage is 0.9 V (logic 2). When the input voltage increases beyond 300 mV, T_5 is OFF, T_1 is still ON, T_4 is ON and T_6 is OFF. The diode-connected CNTFETs T_2 and T_3 produce a voltage drop of 0.45 V (logic 1) from node1 (T_1–T_2 junction) to the output,

Fig. 1 Symbol of **a** STI **b** PTI **c** NTI **d** TNAND **e** TNOR



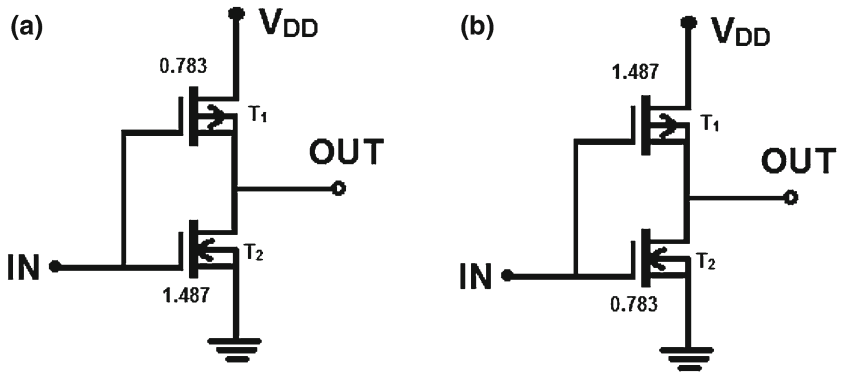


Fig. 3 Structure of **a** NTI **b** PTI

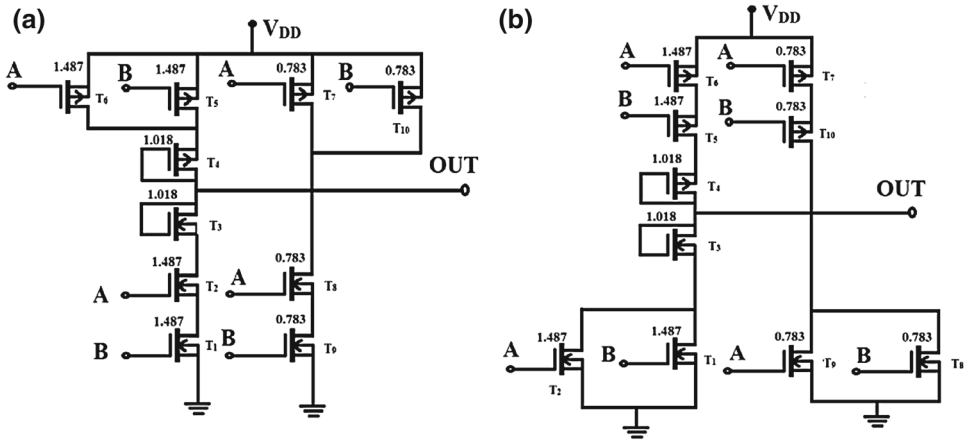


Fig. 4 Structure of 2-input. **a** TNAND gate, **b** TNOR gate

and from the output to node2 (T_3–T_4 junction) due to the threshold voltages of T_2 and T_3, thereby the output voltage becomes 0.45 V. When the input voltage exceeds 0.6 V, both T_1 and T_5 are OFF and T_6 is ON to pull down the output voltage to zero.

Figure 3a shows the schematic of CNTFET NTI. The threshold voltage of T_1 is 0.293 V and T_2 is −0.557 V. When the input voltage is less than 0.3 V (logic 0), the output is 0.9 V. When the input increases above 0.3 V, T_1 is ON and T_2 is OFF and the output voltage will be zero. Figure 3b shows the schematic of CNTFET PTI. The threshold voltage of T_1 is 0.557 V and T_2 is −0.293 V. Only when the input voltage is greater than 0.6 V, the output is zero.

The circuit realization of ternary NAND and NOR gates requires 5 n-CNTFETs and 5 p-CNTFETs as shown in Fig. 4a, b. The chirality of the CNT used for transistors T_1, T_2, T_5, T_6 is (19, 0), for T_3, T_4 is (13, 0) and for T_7, T_8, T_9, T_{10} is (10, 0). The diameter of CNT used for T_1, T_2, T_5, T_6 is 1.487, for T_3, T_4 is 1.018 and for T_7, T_8, T_9, T_{10} is 0.783. The threshold voltage for T_1, T_2, T_5, T_6 is 0.293 V, for T_3, T_4 is 0.428 V and for T_7, T_8, T_9, T_{10} is 0.557 V.

The ternary gates presented in this section can be used for designing CNTFET-based arithmetic and combinational circuits.

4.2 Ternary Decoder

A ternary decoder is a one-input three-output combinational circuit that generates unary functions (X_0, X_1, X_2) for an input X as given by

$$X_0 = \begin{cases} 2 & \text{if } X = 0 \\ 0 & \text{if } X \neq 0 \end{cases} \tag{21}$$

$$X_1 = 2 - X \tag{22}$$

$$X_2 = \begin{cases} 2 & \text{if } X \neq 2 \\ 0 & \text{if } X = 2 \end{cases} \tag{23}$$

Equations (21)–(23) can be realized using NTI, STI and PTI, respectively. In this paper, ternary decoder circuit is constructed using a PTI gate, two NTI gates and one NOR gate as shown in Fig. 5.

4.3 Ternary Half Adder

In ternary logic, as each signal can have three distinct values, the number of digits required is $\log_3 2$ times less than the digits required in binary logic leading to reduced number of computation steps. For example, if we consider an N-bit

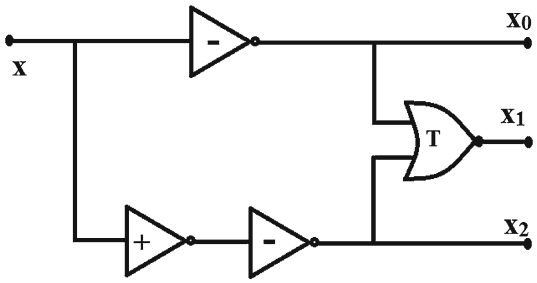


Fig. 5 Ternary decoder circuit

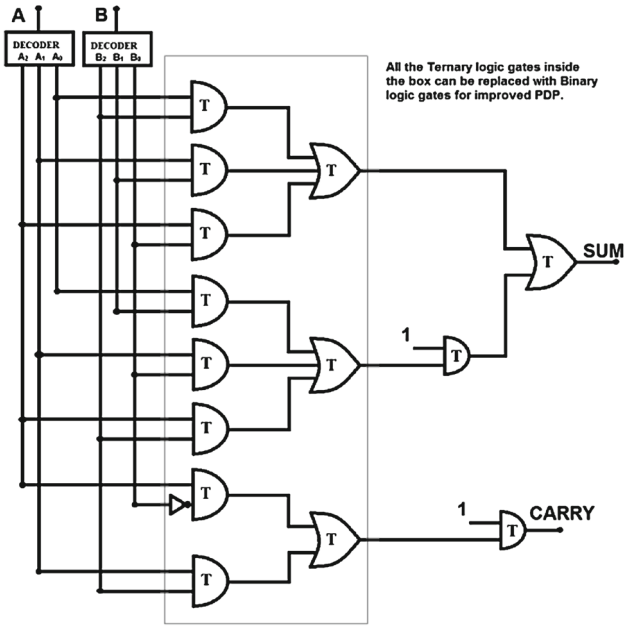


Fig. 6 Structure of ternary half adder

binary adder, then the equivalent ternary adder has $\log_3 2N$ digits.

A ternary half adder is a combinational circuit that adds two bits and generates sum and carry, whose output equations are given by

$$\text{SUM} = A_0B_2 + A_1B_1 + A_2B_0 + 1.(A_0B_1 + A_1B_0 + A_2B_2) \tag{24}$$

$$\text{CARRY} = 1 \cdot (A_2B_1 + A_1B_2 + A_2B_2) \tag{25}$$

$$\text{CARRY} = 1 \cdot (A_2[B_1 + B_2] + A_1B_2) \tag{26}$$

By applying negation of literals technique and equations discussed in Sect. 2, the equation for carry is reduced to

$$\text{CARRY} = 1 \cdot (A_2B_{12} + A_1B_2) = 1 \cdot (A_2\overline{B_0} + A_1B_2) \tag{27}$$

The half adder functions are realized using ternary decoders and ternary logic gates as shown in Fig. 6. Here, A and B are the inputs, and SUM and CARRY are the outputs. The two decoders generate the required unary output signals for the inputs A and B, while the AND and OR logic gates compute the functions given by Eqs. (24) and (27). Number of gates required for conventional ternary half adder circuit is 14 whereas for the proposed using negation is 12.

4.4 Ternary Full Adder

A ternary full adder is a combinational circuit that adds three bits and generates sum and carry, whose output equations are given by

$$\begin{aligned}\text{SUM} = {} & C_0[A_2B_0 + A_1B_1 + A_0B_2] + C_1[A_1B_0 + A_0B_1 \\ & + A_2B_2] + C_2[A_0B_0 + A_2B_1 + A_1B_2] + 1 \cdot \{C_0 \\ & [A_1B_0 + A_0B_1 + A_2B_2] + C_1[A_0B_0 + A_2B_1 \\ & + A_1B_2] + C_2[A_2B_0 + A_1B_1 + A_0B_2]\}\end{aligned} \tag{28}$$

$$\begin{aligned}\text{CARRY} = {} & A_2B_2C_2 + 1 \cdot \{C_0[A_1B_2 + A_2B_1 + A_2B_2] \\ & + C_1[A_1B_1 + A_2 + B_2] + C_2[A_1 + A_2 + B_1 \\ & + B_2]\}\end{aligned} \tag{29}$$

By applying negation of literals technique, the equation for carry is reduced to

$$\begin{aligned}\text{CARRY} = {} & A_2B_2C_2 + 1 \cdot \{A_{12}B_2C_0 + A_2B_1C_0 \\ & + A_1B_1C_1 + A_2C_{12} + B_2C_{12} + A_1C_2 + B_1C_2\} \\ = {} & A_2B_2C_2 + 1 \cdot \{\overline{A_0}B_2C_0 + A_2B_1C_0 \\ & + A_1B_1C_1 + A_2\overline{C_0} + B_2\overline{C_0} + A_1C_2 + B_1C_2\}\end{aligned} \tag{30}$$

The full adder functions are realized using ternary decoders and ternary logic gates as shown in Fig. 7. Here, A, B and C are the inputs, and SUM and CARRY are the outputs. Number of gates required for conventional ternary full adder circuit is 41 whereas for the proposed using negation is 37.

4.5 Ternary Half Subtractor

A ternary half subtractor shown in Fig. 8 is a combinational circuit that subtracts one bit from the other and generates difference and borrow, whose output equations are given by

$$\text{DIFF} = A_0B_1 + A_1B_2 + A_2B_0 + 1 \cdot \{A_1B_0 + A_2B_1 + A_0B_2\} \tag{31}$$

$$\text{BORROW} = 1 \cdot \{A_0B_1 + A_0B_2 + A_1B_2\} \tag{32}$$

Using negation of literals technique, the equation for borrow is reduced to

$$\text{BORROW} = 1 \cdot \{A_0\overline{B_0} + A_1B_2\} \tag{33}$$

Number of gates required for conventional ternary half subtractor circuit is 14 whereas for the proposed using negation is 12.

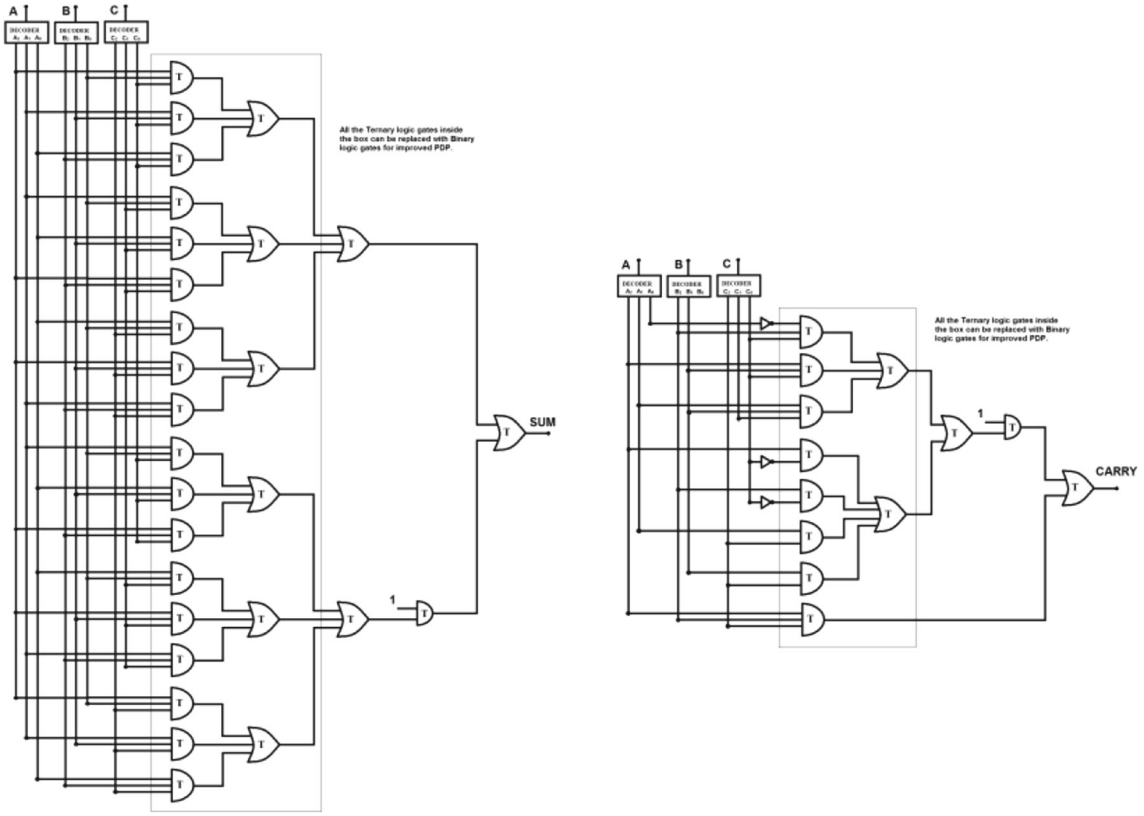


Fig. 7 Structure of ternary full adder for sum & carry

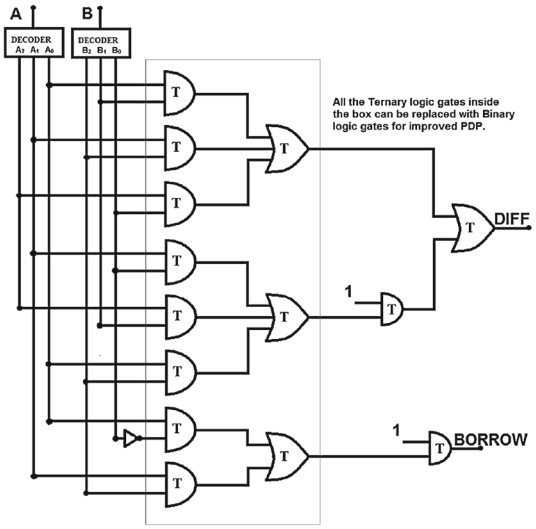


Fig. 8 Structure of ternary half subtractor

$$
\begin{aligned}
\text{DIFF} = {} & A_0B_0C_1 + A_0B_1C_0 + A_2B_2C_0 \\
& + A_1B_0C_2 + A_1B_1C_1 + A_1B_2C_0 \\
& + A_2B_0C_0 + A_2B_1C_2 + A_2B_2C_1 \\
& + 1 \cdot \{A_0B_0C_2 + A_0B_1C_1 + A_2B_2C_1 \\
& + A_1B_0C_0 + A_1B_1C_2 \\
& + A_1B_2C_1 + A_2B_0C_1 + A_2B_1C_0 + A_2B_2C_2\} \quad (34)
\end{aligned}
$$

$$
\begin{aligned}
\text{BORROW} = {} & A_0B_2C_2 + 1 \cdot \{A_0C_2 + A_1C_2 + A_0C_1 \\
& + A_0B_2 + A_1B_2 + B_2C_1 + B_2C_2 + B_1C_2 \\
& + A_0B_1C_0 + A_1B_1C_1\} \quad (35)
\end{aligned}
$$

By applying negation technique, the equation for borrow is reduced to

$$
\begin{aligned}
\text{BORROW} = {} & A_0B_2C_2 + 1 \cdot \{A_{01}C_2 + A_0C_1 + A_{01}B_2 \\
& + B_2C_{12} + B_1C_2 + A_0B_1C_0 + A_1B_1C_1\} \\
= {} & A_0B_2C_2 + 1 \cdot \{\overline{A_2}C_2 + A_0C_1 + \overline{A_2}B_2 \\
& + B_2\overline{C_0} + B_1C_2 + A_0B_1C_0 + A_1B_1C_1\} \\
& \quad (36)
\end{aligned}
$$

4.6 Ternary Full Subtractor

A ternary full subtractor shown in Fig. 9 is a combinational circuit that subtracts one bit from the other and generates difference and borrow, whose output equations are given by

Number of gates required for conventional ternary full subtractor circuit is 41 whereas for the proposed using negation is 37.

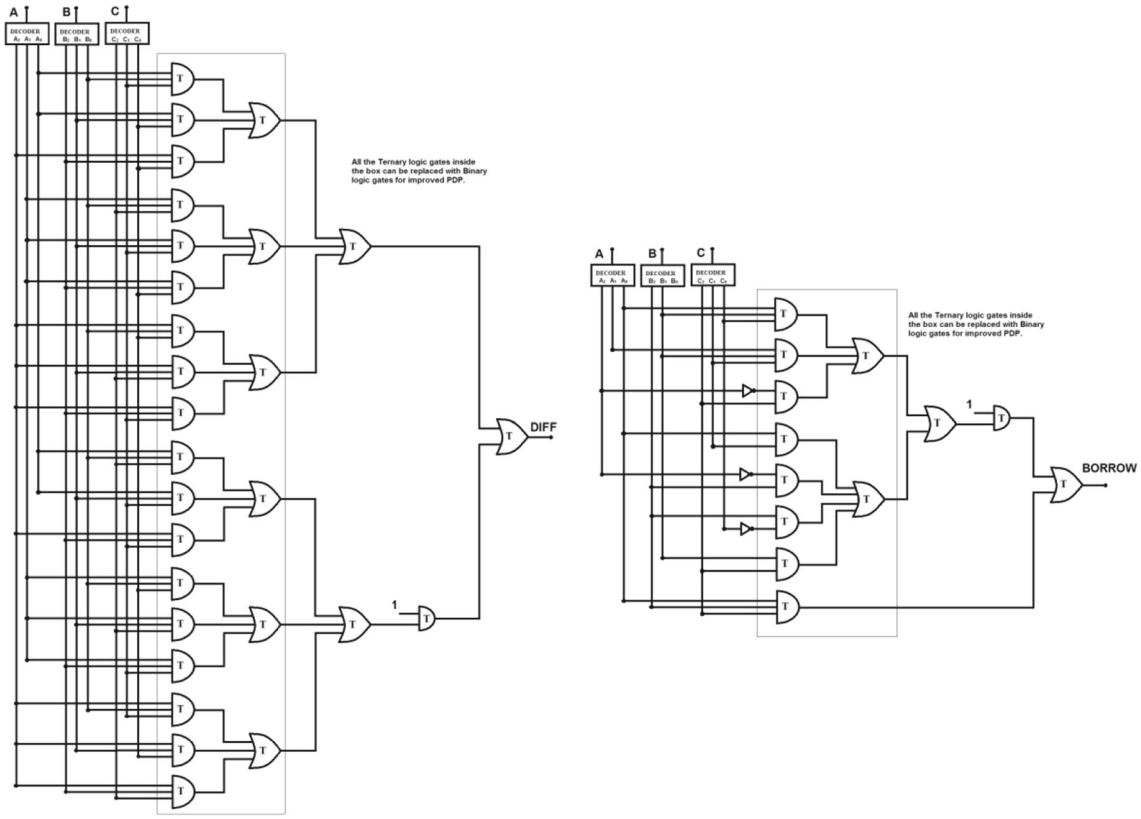


Fig. 9 Structure of ternary full subtractor for difference and borrow

4.7 2-Bit Binary Comparator

A ternary magnitude comparator is a combinational circuit that compares two bits A and B and determines their relative magnitudes. The comparison of two bits is an operation that determines if one number is greater than, less than or equal to other number. Circuit realization of ternary comparator is shown in Fig. 10a–c.

4.7.1 Ternary Equality Comparator

A ternary equality comparator shown in Fig. 10a compares two numbers A (A_1A_0) and B (B_1B_0) and sets the output $Y_{A=B}$ as '2' if and only if $A = B$; otherwise sets $Y_{A=B}$ as '0'. The output equations of the comparator for the operation $A = B$ are given by

$$\begin{aligned} Y_{A=B} &= A_0^0A_1^0B_0^0B_1^0 + A_0^1A_1^0B_0^1B_1^0 + A_0^2A_1^0B_0^2B_1^0 \\ &\quad + A_0^0A_1^1B_0^0B_1^1 + A_0^1A_1^1B_0^1B_1^1 + A_0^2A_1^1B_0^2B_1^1 \\ &\quad + A_0^0A_1^2B_0^0B_1^2 + A_0^1A_1^2B_0^1B_1^2 + A_0^2A_1^2B_0^2B_1^2 \\ &= [A_0^0B_0^0 + A_0^1B_0^1 + A_0^2B_0^2] \\ &\quad \cdot [A_1^0B_1^0 + A_1^1B_1^1 + A_1^2B_1^2] \end{aligned} \tag{37}$$

4.7.2 Ternary Less than Comparator

A ternary less than comparator shown in Fig. 10b compares two numbers A (A_1A_0) and B (B_1B_0) and sets the output Y as '2' if and only if $Y_{A<B}$, otherwise sets $Y_{A<B}$ as '0'. The output equations of the comparator for the operation $A < B$ are given by

$$\begin{aligned} Y_{A<B} &= A_0^0A_1^1B_0^1B_1^1 + A_0^0A_1^2B_0^1B_1^2 + A_0^0A_1^1B_0^2B_1^1 \\ &\quad + A_0^1A_1^1B_0^2B_1^1 + 2A_1^0B_1^1 + 2A_1^0B_1^2 + 2A_1^1B_1^2 \\ &\quad + 2B_0^2B_1^2[A_0^0 + A_0^1] + A_0^0A_1^0B_0^1 \\ &\quad + 2A_1^0B_0^2[A_0^0 + A_0^1] \end{aligned} \tag{38}$$

By applying negation of literals technique, the output equation of the comparator for the operations $A < B$ is reduced to

$$\begin{aligned} Y_{A<B} &= A_1^0B_1^{12} + A_1^1B_1^2 + A_0^0A_1^0B_0^{12} + A_0^{01}B_0^2B_1^2 \\ &\quad + A_0^1A_1^0B_0^2 + A_0^0A_1^1B_0^{12}B_1^1 + A_0^1A_1^1B_0^2B_1^1 \\ &\quad + A_0^0A_1^2B_0^1B_1^2 \\ &= A_1^0\overline{B_1^0} + A_1^1B_1^2 + A_0^0A_1^0\overline{B_0^0} + \overline{A_0^2}B_0^2B_1^2 \\ &\quad + A_0^1A_1^0B_0^2 + A_0^0A_1^1\overline{B_0^0}B_1^1 + A_0^1A_1^1B_0^2B_1^1 \\ &\quad + A_0^0A_1^2B_0^1B_1^2 \end{aligned} \tag{39}$$

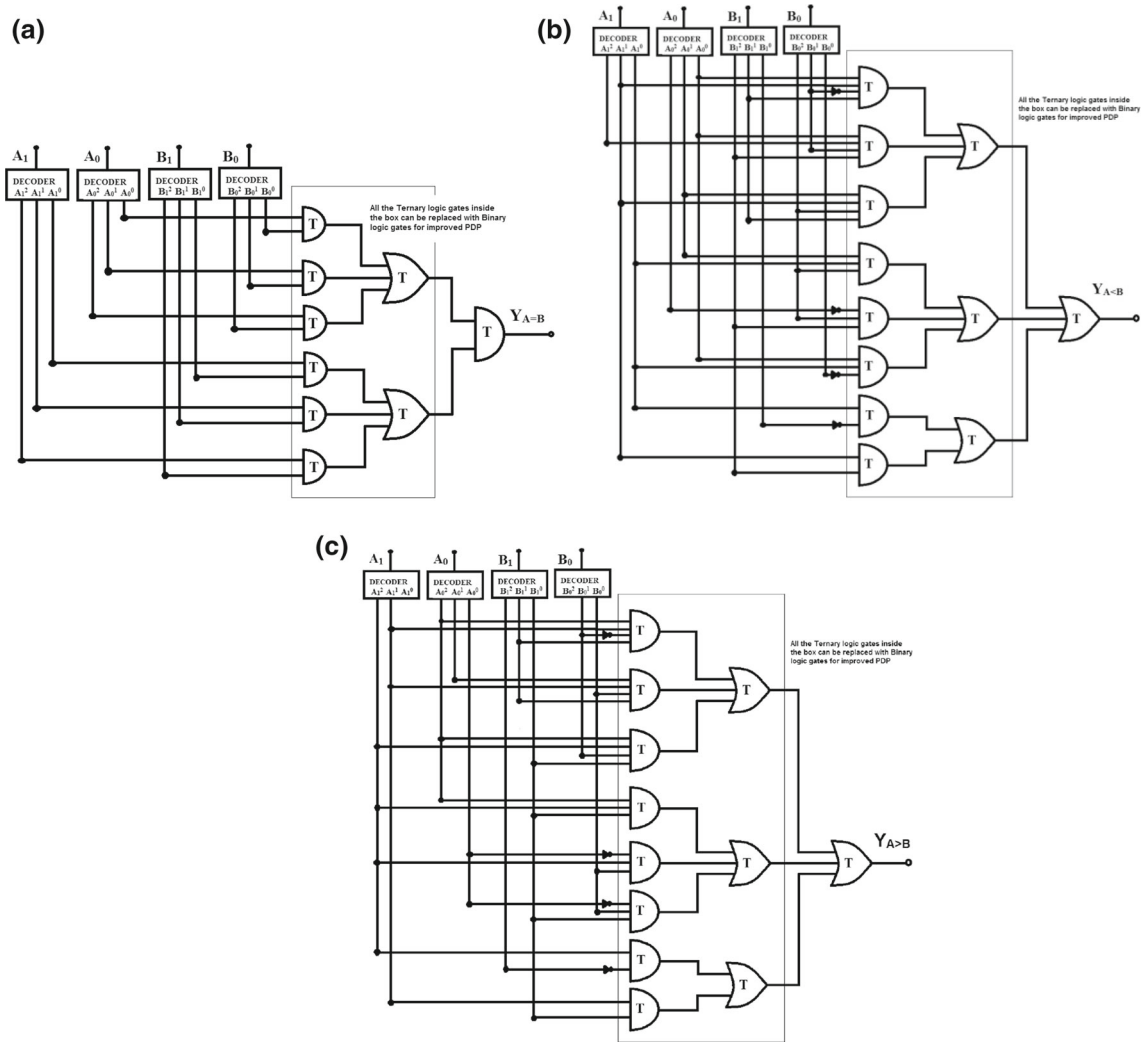


Fig. 10 **a** CNTFET-based 2-bit ternary comparator ($A = B$). **b** CNTFET-based 2-bit ternary comparator ($A < B$). **c** CNTFET-based 2-bit ternary comparator ($A > B$)

4.7.3 Ternary Greater than Comparator

A ternary greater than comparator shown in Fig. 10c compares two numbers A (A_1A_0) and B (B_1B_0) and sets the output $Y_{A>B}$ as '2' if and only if $A > B$, otherwise sets $Y_{A>B}$ as '0'. The output equations of the comparator for the operation $A > B$ are given by

$$\begin{aligned} Y_{A>B} = {} & A_0^2A_1^1B_0^0B_1^1 + A_0^1A_1^1B_0^0B_1^1 + A_0^2A_1^1B_0^1B_1^1 \\ & + A_0^2A_1^2B_0^1B_1^0 + A_0^2A_1^2B_0^1 + 2B_0^0B_1^0[A_0^1 + A_0^2] \\ & + 2A_1^2B_0^0[A_0^1 + A_0^2] + 2A_1^1B_1^0 + 2A_1^2B_1^1 + 2A_1^2B_1^0 \end{aligned} \tag{40}$$

By applying negation of literals technique, the output equation of the comparator for the operations $A > B$ is reduced to

$$\begin{aligned} Y_{A>B} = {} & A_0^2A_1^1B_0^{01}B_1^1 + A_0^1A_1^1B_0^0B_1^1 + A_0^2A_1^2B_0^1B_1^0 \\ & + A_0^2A_1^2B_0^1 + A_0^{12}A_1^2B_0^0 + A_0^{12}B_0^0B_1^0 \\ & + A_1^1B_1^0 + A_1^2B_1^{01} \\ = {} & A_0^2A_1^1\overline{B_0^2}B_1^1 + A_0^1A_1^1B_0^0B_1^1 + A_0^2A_1^2B_0^1B_1^0 \\ & + A_0^2A_1^2B_0^1 + \overline{A_0^0}A_1^2B_0^0 + \overline{A_0^0}B_0^0B_1^0 + A_1^1B_1^0 \\ & + A_1^2\overline{B_1^2} \end{aligned} \tag{41}$$

Number of gates required for conventional ternary comparator circuit is 41 whereas for the proposed using negation is 31.

5 Results and Discussion

A Synopsys HSPICE simulator has been used to simulate the proposed ternary-logic-based combinational circuits. The analysis has been done at three levels:

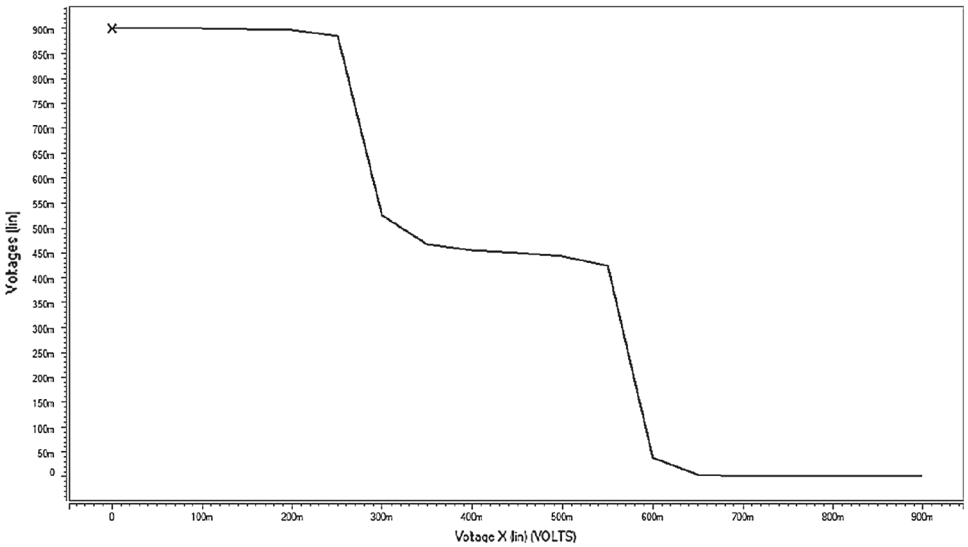


Fig. 11 Transient response of ternary inverter

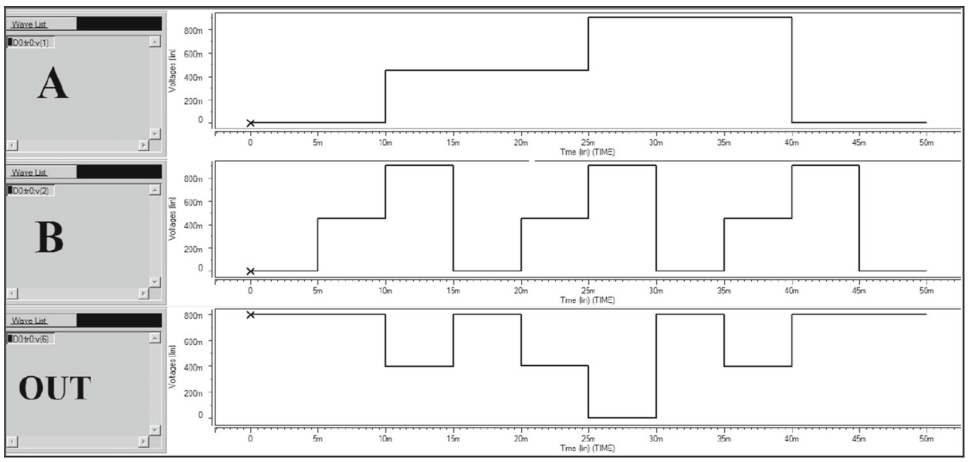


Fig. 12 Behavior of ternary NAND

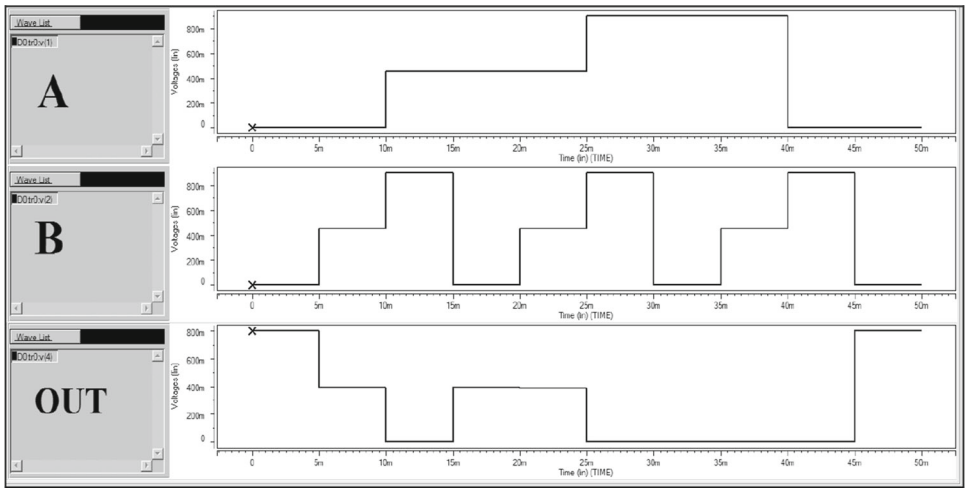


Fig. 13 Behavior of ternary NOR

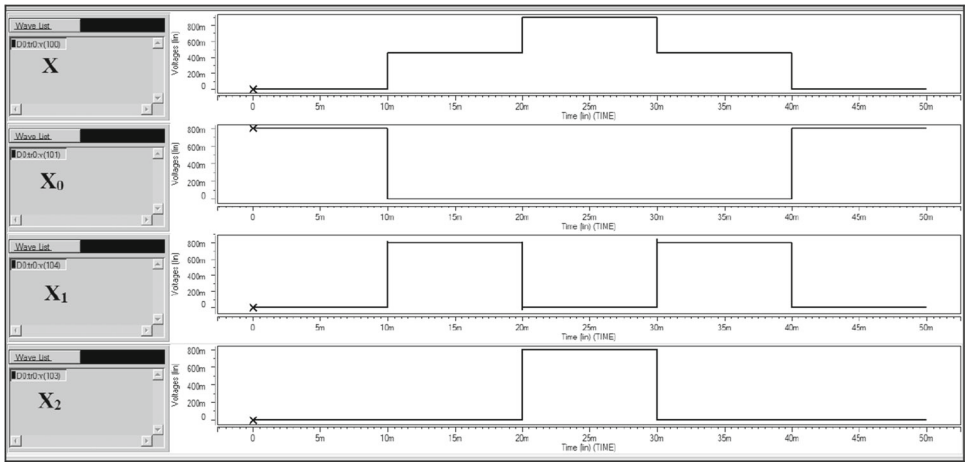


Fig. 14 Transient response of ternary decoder

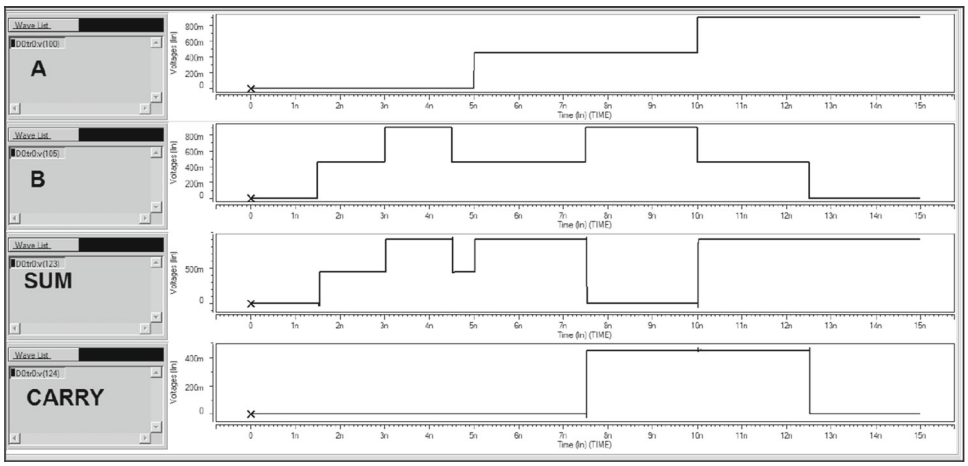


Fig. 15 Transient response of ternary half adder

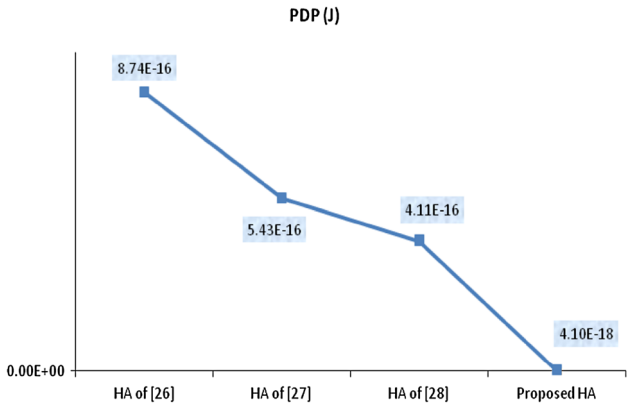


Fig. 16 Comparison of PDP of proposed and existing half adder

(i) Using ternary logic gates alone.
(ii) Using a combination of ternary and binary logic gates, thereby the performance can be significantly improved if the ternary and binary logic gates are used in a combined manner to take the advantage of their respective merits because binary logic is a good candidate for fast computing modules.
(iii) Using negation of literals technique, this proposed design achieves power and delay savings due to the reduced number of transistors and a significant saving in the area can also be achieved.

These analyses assume CNTFETs that are made of homogeneous, identical CNTs, i.e. well-aligned parallel semiconducting CNTs that have the same chirality, the same doping level, the same inter-CNT pitch and local interconnect capacitances and CNT imperfections are not included. Increase in the number of CNTs per device is the most effective way of improving the circuit speed. In this paper, the number of CNTs per device is increased from 1 to 3 to evaluate the trade-off between speed and energy.

Figure 11 shows the voltage transfer characteristics of STI. Compared to the STI design proposed by Raychowdhury et al. [25], the proposed STI design provides a larger noise margin and achieves a rail to rail output swing which is highly required for low-power supply circuits. HSPICE simulation results showed that PDP of STI is 5.22×10^{-17} J and the PDP of the STI in [25] is 2.07×10^{-16} J. The proposed design achieves more than 350 % PDP improvement over [25].

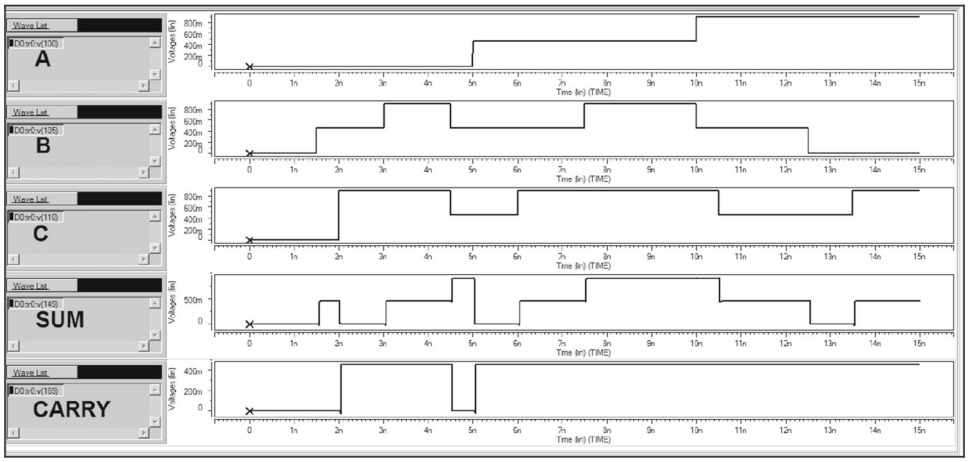


Fig. 17 Transient response of ternary full adder

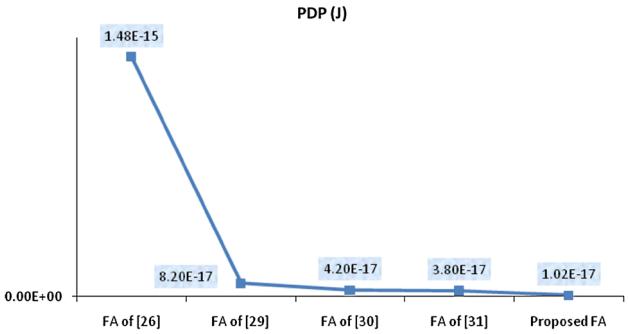


Fig. 18 Comparison of PDP of proposed and existing full adder

Figures 12 and 13 show the behavior of ternary NAND and NOR gates, respectively, from which the proper functioning of the circuits for various input variables can be observed. The average delay and average power consumed by the ternary NAND are 7.47×10^{-12} s and 1.95×10^{-7} W, respectively. Thus, the power delay product is 1.46×10^{-18} J. The average delay and average power consumed by the ternary NOR are 4.99×10^{-12} s and 2.57×10^{-7} W, respectively. Thus, the power delay product is 1.28×10^{-18} J.

Figure 14 shows the transient response of ternary decoder circuit. Using Hspice simulations, the average delay and average power consumed by the designed ternary decoder are calculated to be 4.24×10^{-11} s and 1.2×10^{-7} W, respectively. Thus, the power delay product is 5.10×10^{-17} J.

Figure 15 shows the transient response of ternary half adder circuit. Using Hspice simulations, the average delay and average power consumed by the designed ternary half adder are calculated to be 0.52×10^{-11} s and 0.77×10^{-6} W, respectively. Thus, the power delay product is 0.041×10^{-16} J (Neg) which is about 29 times lower than ternary logic(Ter), 17 times lower than ternary–binary logic (Ter–Bin), 145 times lower than the circuit of Subhajit Das et al. [26], 134 times lower than the circuit of Dhande et al. [27], 100 times lower than the circuit of Sheng Lin et al. [28] (shown in Fig. 16).

Figure 17 shows the transient response of ternary full adder circuit. Using Hspice simulations, the average delay and average power consumed by the designed ternary full adder are calculated to be 0.96×10^{-11} s and 1.06×10^{-6} W, respectively. Thus, the power delay product is 0.102×10^{-16} J which is about 21 times lower than ternary logic,

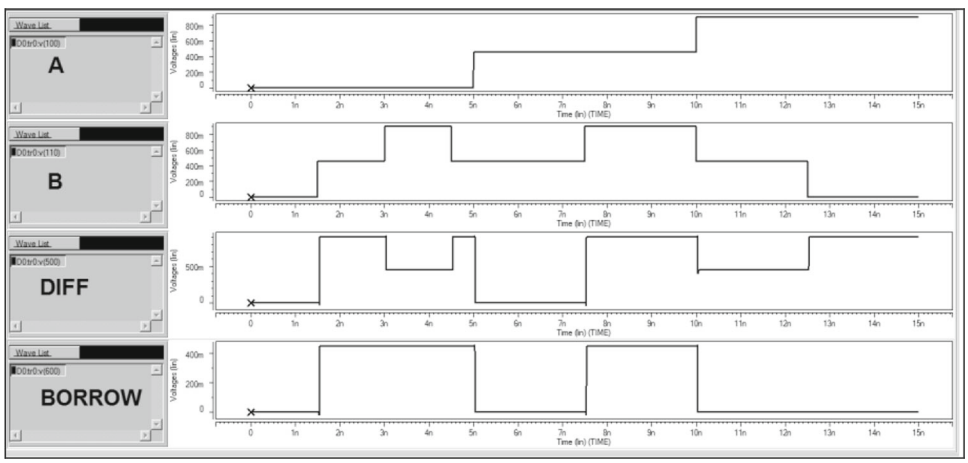


Fig. 19 Transient response of ternary half subtractor

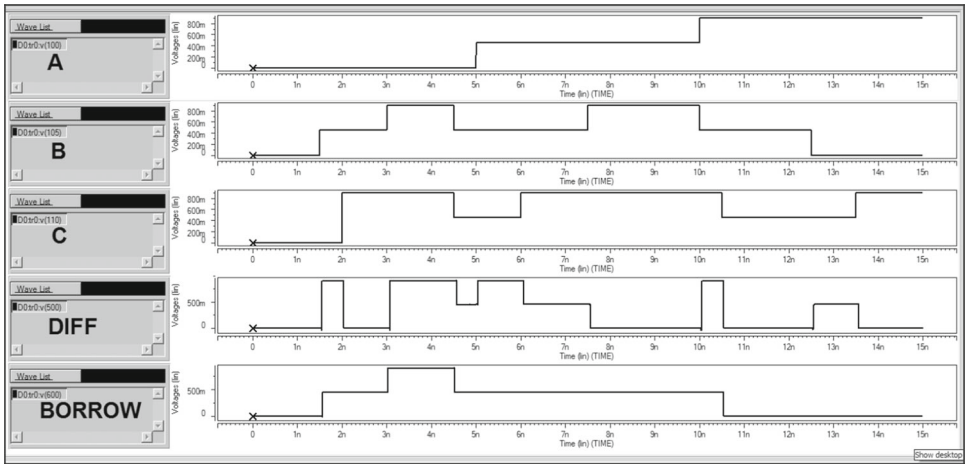


Fig. 20 Transient response of ternary full subtractor

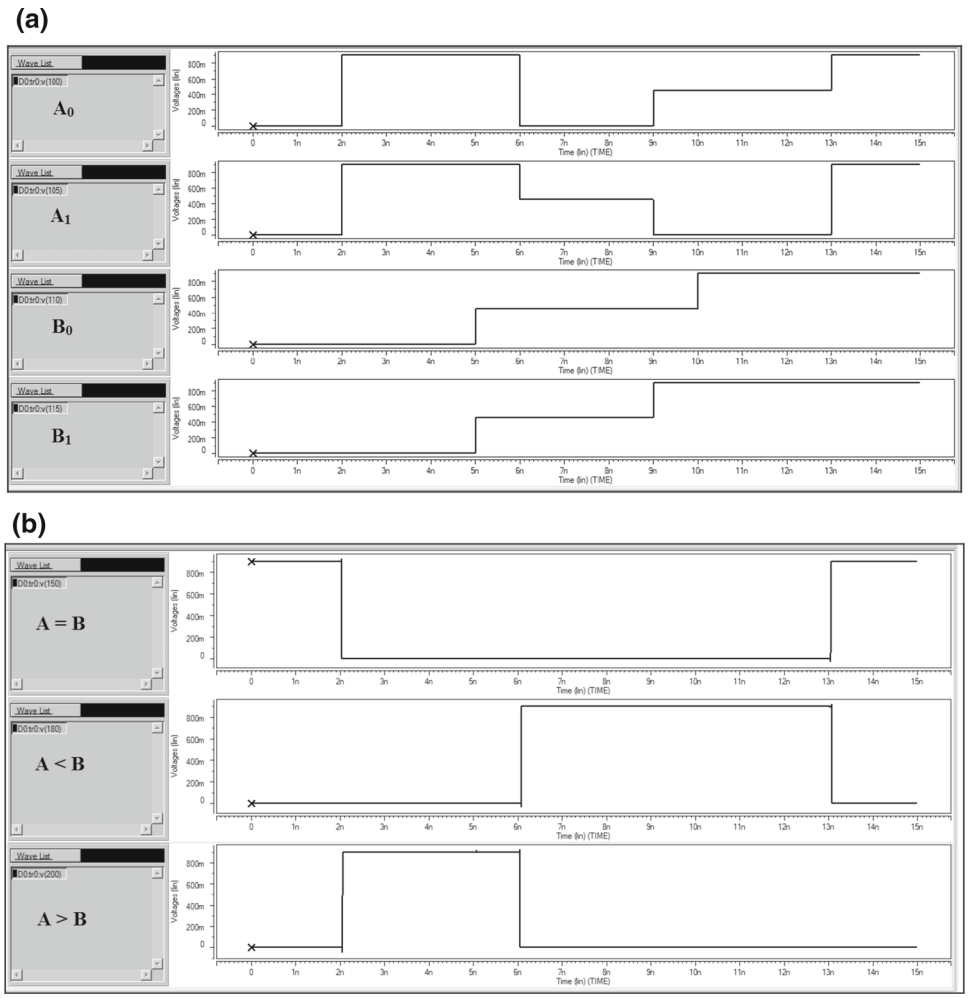


Fig. 21 **a** Behavior of 2-bit comparator inputs—A_0, A_1, B_0 & B_1. **b** Behavior of 2-bit comparator outputs—$A = B$, $A < B$ & $A > B$

13 times lower than ternary–binary logic, 145 times lower than the full adder designed by Subhajit Das et al. [26] and 4 to 5 times lower than the full adder designed by Navi et al. [29–31] (shown in Fig. 18).

Figure 19 shows the transient response of ternary half subtractor circuit. Using Hspice simulations, the average delay and average power consumed by the designed ternary half subtractor are calculated to be 0.71 $\times$ 10^{-11} s and 0.99 $\times$

Table 3 Comparison between CNTFET combinational circuits

Combinational circuit	Average delay ($\times 10^{-11}$ s)			Average power ($\times 10^{-6}$ W)			PDP ($\times 10^{-16}$ J)		
	Ter	Ter–Bin	Neg	Ter	Ter–Bin	Neg	Ter	Ter–Bin	Neg
Full adder	5.32	3.41	.96	4.04	3.87	1.06	2.15	1.32	.102
Half adder	4.13	2.48	.52	2.87	2.77	.77	1.19	.686	.041
Full subtractor	6.55	3.72	.88	3.87	3.66	1.77	2.53	1.36	.155
Half subtractor	5.47	3.97	.71	2.20	2.16	.99	1.20	.857	.069
Comparator	20.00	17.6	9.11	10.3	6.35	2.56	20.6	11.2	2.33

Table 4 Comparison of proposed design with existing design

Circuit	Average power (W)	Average delay (s)	PDP (J)
FA of [26]	2.4×10^{-7}	6.2×10^{-9}	14.8×10^{-16}
FA of [29]	1.05×10^{-6}	7.83×10^{-11}	8.2×10^{-17}
FA of [30]	7.83×10^{-7}	5.36×10^{-11}	4.2×10^{-17}
FA of [31]	3.32×10^{-7}	1.14×10^{-10}	3.8×10^{-17}
Proposed FA	1.06×10^{-6}	0.96×10^{-11}	1.02×10^{-17}
HA of [26]	1.9×10^{-7}	4.6×10^{-9}	8.74×10^{-16}
HA of [27]	–	–	5.43×10^{-16}
HA of [28]	–	–	4.11×10^{-16}
Proposed HA	7.7×10^{-7}	0.52×10^{-11}	$.041 \times 10^{-16}$

10^{-6} W, respectively. Thus, the power delay product is 0.069 $\times 10^{-16}$ J which is about 17 times lower than ternary logic and 12 times lower than ternary–binary logic.

Figure 20 shows the transient response of ternary full subtractor circuit. Using Hspice simulations, the average delay and average power consumed by the designed ternary full subtractor are calculated to be 0.88 $\times 10^{-11}$ s and 1.77 $\times 10^{-6}$ W, respectively. Thus, the power delay product is 0.155 $\times 10^{-16}$ J which is about 16 times lower than ternary logic and 9 times lower than ternary–binary logic.

Figure 21a, b shows the transient response of the proposed ternary comparator. Using Hspice simulations, the average delay and average power consumed by the ternary comparator are calculated to be 9.11 $\times 10^{-11}$ s and 2.56 $\times 10^{-6}$ W, respectively. Thus, the power delay product is 2.33 $\times 10^{-16}$ J which is about 9 times less than ternary logic and 5 times less than ternary–binary logic.

The values of average power consumed, average delay and PDP of the proposed and existing circuits are tabulated in Tables 3 and 4.

Figure 22a–c shows the comparison of average delay, average power and power delay product of the proposed circuits with three different approaches such as by using ternary logic gates, combination of ternary–binary logic gates and the proposed negation of literals technique.

The proposed negation of literals approach reduces the number of products in the SOP (sum of products) expressions of the output equations (Eqs. (27), (30), (33), (36), (39), (41)) of the combinational circuits. This allows achieving a number of advantages: reduction in number of devices ranging from 10 to 35 % corresponds to lowering in switching activities, reduction in computational complexity, reduction in computational time ranging from 75 to 95 % with reduced number of iterations (ranges from 27 to 43 %) and reduction in output error from 29 % (Ternary–Binary) to 6 % compared to Ternary logic. Thus, the proposed approach on combinational circuits is shown to have some significant advantages relative to other ternary circuits like low-power dissipation, reduced propagation delay and also reduced device count. From Fig. 22c, it can be shown that the proposed design offers 5 to 29 times improvement in PDP as compared to the other two existing designs.

Comparison based on number of gates used for the design of various circuits is shown in Fig. 23 which shows that a significant reduction in the gate count can be achieved using the proposed technique leading to reduction in chip area.

6 Conclusion

The prospects of applying ternary logic in computation have been discussed in this paper. As the diameter of the CNT used in CNTFET decides the threshold voltage of the transistor, a multi-threshold design was achieved using CNTs with different diameters in the CNTFETs which is used for realizing ternary-logic circuits. All simulations have been performed in HSPICE and the simulated results validated the correct operation of the realized circuits. Comparison made between binary and ternary logic showed that the circuits designed using ternary logic and combination of ternary and binary logic are predicted to be faster than classical binary circuits and work at even lower power. Also the proposed ternary logic design using negation of literals technique achieves significant power and delay savings due to the reduced number of transistors and a significant saving in the area could be the fast and low-power solution to digital computation compared

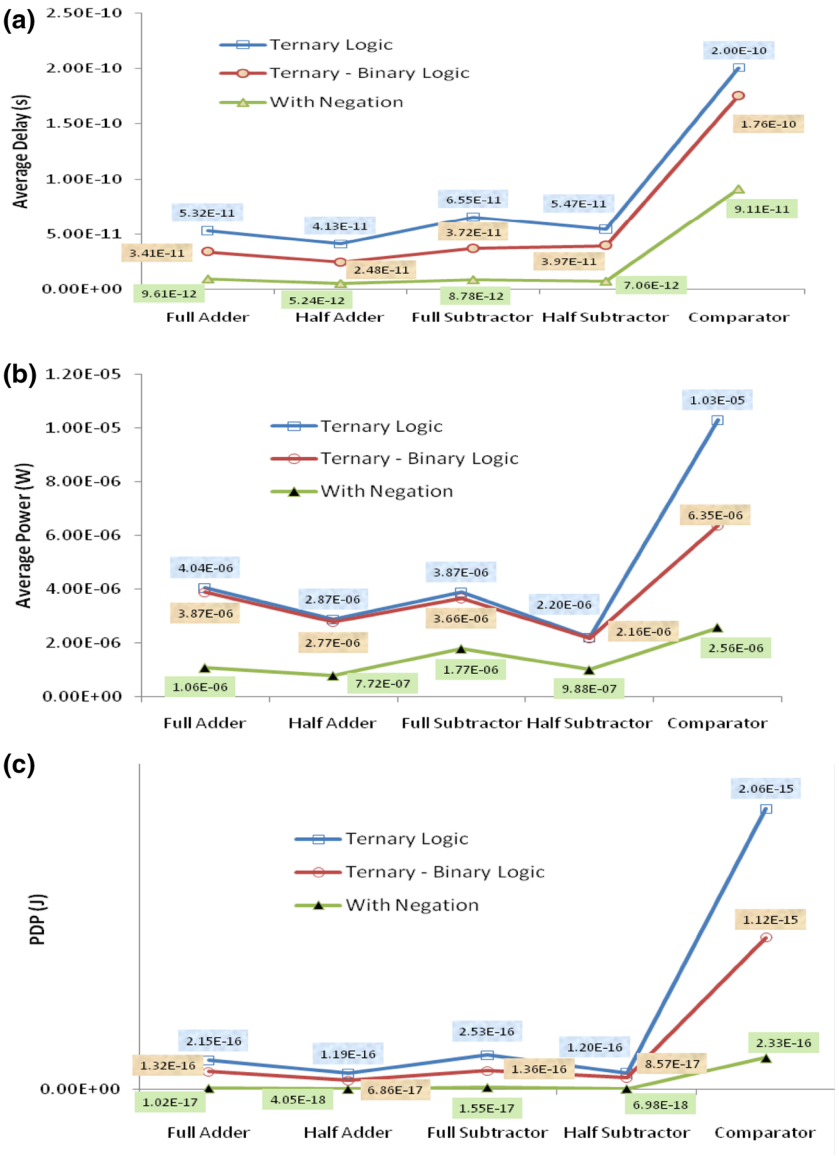


Fig. 22 **a** Comparison of average power of CNTFET combinational circuits. **b** Comparison of average delay of CNTFET combinational circuits. **c** Comparison of PDP of CNTFET combinational circuits

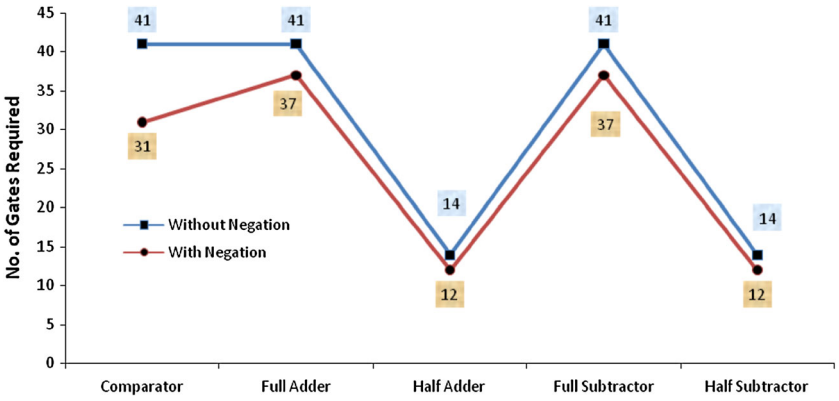


Fig. 23 Comparison based on number of gates used

with existing ternary logic families for arithmetic circuits. A higher processing rate can be achieved by expanding the existing logic levels to the higher logic levels by applying the proposed technique.

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