

Role of Doping in Carbon Nanotube Transistors With Source/Drain Underlaps

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Abstract—The effects of doping on the performance of coaxially gated carbon nanotube (CNT) field-effect transistors for both zero Schottky-barrier (SB) and doped carbon nanotube contacts are theoretically investigated. For ultrascaled CNTFETs in which the source/drain metal contacts lie 50 nm apart, there is no MOSFET-like contact CNTFET (C-CNTFET) with an acceptable on/off current ratio using a CNT of diameter ≥ 1.5 nm and a source/drain voltage ≥ 0.4 V. For CNTFETs with source/drain metal contacts either 50 nm or 100 nm apart, there is an optimal doping concentration of 10^{-3} dopants per atom. The maximum on/off current ratios for the 50 nm CNT/5 nm gate and the 100 nm CNT/10 nm gate SB-CNTFETs are 5×10^4 and 6×10^5 , respectively. Performance metrics of delay time, cutoff frequency, and LC frequency are presented and compared.

Index Terms—Doped carbon nanotube, doped source/drain contact, field effect transistor, source/drain underlap, zero Schottky barrier contact.

I. INTRODUCTION

UNDERSTANDING of electrostatics [1]–[4], transport mechanisms [5]–[8], scaling behavior [9]–[14], and performance [15]–[22] of carbon nanotube field-effect transistors (CNTFETs) has been rapid. Notable breakthroughs are the discovery of zero-Schottky-barrier contacts [23]–[28], integration of logic gates, a static RAM, a ring oscillator [29], [30], and the large scale integration of CNTs with Si [31].

Performance improvement especially in the on state of CNTFETs by chemically doping the nanotube to n-type has been demonstrated experimentally [32], [33]. Doping of both single-wall and multiwall nanotubes by either electron donors or electron acceptors has been reviewed [34]. As-grown p-type nanotube devices have been converted to n-type devices by controlled doping [35], [36]. The application of doped nanotubes as single-electron transistors has been discussed [37]. Theoretical studies on CNTFETs with doped nanotube contacts (C-CNTFETs) have been performed using single band [38] and

full band calculations [39], [40]. Recently different issues in modeling C-CNTFETs have been discussed [41].

Originally motivated by bioassembly of CNTFETs, we studied CNTFETs with ultrashort metal gates and source/drain underlaps to understand the transport physics and performance [5], [6], [42]. The effects of dielectric constant and thickness and geometry were investigated [14], [22]. It soon became apparent that these designs had excellent performance metrics and that their applicability went beyond the concerns of bioassembly. We have found, as a rule of thumb, that the device with the least capacitance ‘wins’ in terms of speed performance [14], [22]. As with any rule of thumb, there are exceptions such as the asymmetric device with its figures of merit shown in Table III of [6], but the rule generally points one in the right direction. For the case of CNTFETs, we have found the capacitance to be dominated by the fringing fields directly from metal gate to metal source/drain, the equivalent of the overlap capacitance in traditional Si FETs. The underlaps reduce this capacitance. The underlaps reduce the electric field in the drain and thus reduce the interband tunneling in the drain which is the cause of the ambipolar leakage current and reduced on/off current ratios. The underlaps reduce the gate to drain capacitance and thus the effect of the drain potential on the potential under the gate. Therefore, the underlaps improve both dc and ac device performance. We are not the first to discover the advantages of underlaps. Similar device geometries with doped source/drain and undoped underlaps have been previously considered for silicon FinFETs [43], [44]. An underlap value of >10 nm has been reported to reduce short-channel effects and to obtain optimal performance [45], [46]. Recently Stanford and IBM groups have studied CNTFETs with source/drain underlap geometry to minimize parasitic capacitance [25], [47].

In our previous studies, the CNTs were undoped. In this work, we investigate the effects of doping on the same model device geometry. The n-type doped carbon nanotube transistors have been studied experimentally by Javey *et al.* [33] and Radosavljevic *et al.* [32] for CNTs with diameters 1.4 to 1.6 nm that we study here. Both the groups reported high on current and larger transconductance values with doped carbon nanotubes. Javey *et al.* observe an optimal doping level in terms of on/off current ratio. The off current increases significantly at doping levels higher than the optimal value and the on/off current ratio degrades.

To understand the physics of doping effects on the performance of CNTFETs, especially on the off-state, and to design an optimal device in terms of high on/off current ratio we consider two types of contacts in this study. (i) Zero Schottky-barrier contacts with lightly doped source/drain underlaps which we will

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designate as SB-CNTFETs and (ii) heavily doped CNT contacts which we will designate as C-CNTFETs following Knoch *et al.* [38]. With a 50 nm CNT and a 5 nm gate, the SB-CNTFETs have optimal on/off current ratios for a doping level of 10^{-3} dopants per atom. To obtain MOSFET-like contacts in a 50 nm CNT, we need a doping concentration value of 5×10^{-3} or higher dopants per atom. At these doping concentrations the direct source to drain tunneling dominates the leakage current. This reduces the on/off current ratio in C-CNTFETs by orders of magnitude. We propose a 100 nm SB-CNTFET with a gate length of 10 nm and an optimal doping level of 10^{-3} dopants per atom as the optimal device. This device has an on/off current ratio of 6×10^5 , an inverse subthreshold slope of 62 mV/dec, a switching delay time of 32 fs, and has almost unipolar characteristics over the entire range of gate bias used in this study.

II. MODEL

The simulations perform a self-consistent solution between Poisson's equation and the nonequilibrium Green's function (NEGF) equations. The NEGF/Poisson solver is discussed in detail in [6]. A two-dimensional Poisson equation is solved in the cylindrical coordinates for coaxially gated CNTFETs. The permittivity varies only in the radial direction. For the Schottky-barrier CNTFETs, Dirichlet boundary conditions are used at the source, drain, and gate. Von Neumann boundary conditions are used along the exposed surface of the dielectric. There, the radial component of the electric field is set to zero. A zero field boundary condition is applied at the source and drain ends for the CNTFETs with doped reservoirs. There, the axial component of the electric field is set to zero.

The CNT is modeled using a tight binding π -bond model with one p_z orbital per carbon atom. The Hamiltonian matrix elements are taken from [48]. The recursive Green function algorithm is used to solve the NEGF equations for the mean field charge density and current. The surface Green's function is calculated using decimation method [42], [49], [50].

III. NUMERICAL RESULTS AND DISCUSSIONS

The device channel consists of a (19,0), zigzag CNT with a bandgap E_g of 0.53 eV and a diameter of 1.5 nm. The device cross-sections are shown in Fig. 1. Fig. 1(a) is the cross section of a SB-CNTFET and 1(b) is the cross section of a C-CNTFET. The gate dielectric is a 2 nm thick SiO_2 and the device has a gate length L_g of 5 nm. Our simulation device is coaxial in structure with a partial gate. We use an extended domain scheme for the Poisson solver with extension $t_{\text{ox-ex}} = 6$ nm in the radial direction. For SB-CNTFETs, a 20 nm extension on either side of the source and drain contacts is included in the simulation domain of Poisson equation so that the fringing electric field between the gate and source and the gate and drain metals is treated correctly. We use four different doping profiles; a step doping profile and three different Gaussian distributions shown in Fig. 2. A Gaussian dopant distribution has been used before to study source/drain underlap FinFETs [44].

To see the effect of doping level on the source and drain underlaps of SB-CNTFETs, we plot, in Fig. 3(a), the simulated $\log I_D$ versus V_{GS} characteristics for five different uniform doping concentrations of 0, 5×10^{-4} , 1×10^{-3} , 5×10^{-3} ,

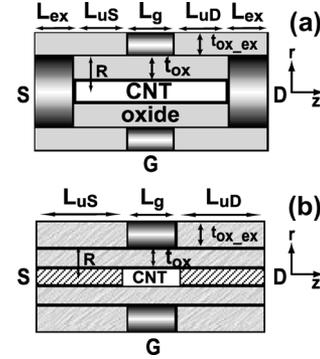


Fig. 1. Device cross-sections for the Schottky-barrier CNTFET (SB-CNTFET) and the CNTFET with semi-infinite doped CNT contacts (C-CNTFET).

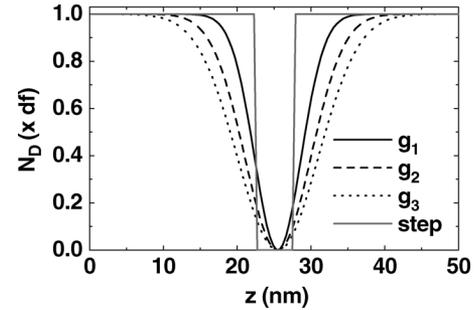


Fig. 2. Three different Gaussian and a step profiles for dopant distribution in the channel. The df is the dopant per carbon atom. Its values for step profile are mentioned in the text, and it is 10^{-3} dopant per carbon atom for SB-CNTFETs and 5×10^{-3} for the C-CNTFETs for all the Gaussian distributions.

and 1×10^{-2} dopants per carbon atom. The off-state performance (leakage current) improves with doped source/drain underlaps when the doping fraction increases from 5×10^{-4} to 10^{-3} . Further increasing the doping fraction increases the on current, however, the off current also increases significantly and on/off current ratio degrades.

To explain why the device performance, especially the subthreshold behavior, degrades with relatively high doping concentrations, we plot the conduction band profiles in Fig. 3(b). At high doping, 5×10^{-3} to 1×10^{-2} , there is a significant reduction in the conduction band tunnel barrier length as well as the barrier height. The leakage current is dominated by direct source-to-drain (intraband) tunneling. This reduces the on/off current ratio by orders of magnitude. For high doping concentrations, the electron current is the dominant component of the leakage current over the entire range of gate bias considered in these simulations.

In the lower doping range, when the CNT doping of 5×10^{-4} is increased to 10^{-3} , there is small modulation of the tunnel barrier width that increases the intraband tunneling component of the leakage current. However, the interband tunneling component of current is simultaneously reduced. The overall effect is a reduction of the the minimum current and an increase in the maximum on/off current ratio. This optimal doping level of 10^{-3} dopants per carbon atom, equivalent to 0.18 nm^{-1} , is in the range observed by the IBM experimental group [32], and Bockrath *et al.* [36].

To describe why the interband tunneling component of the leakage current is reduced when the doping is increased from 5×10^{-4} to 10^{-3} , we plot the conduction and valence bands and

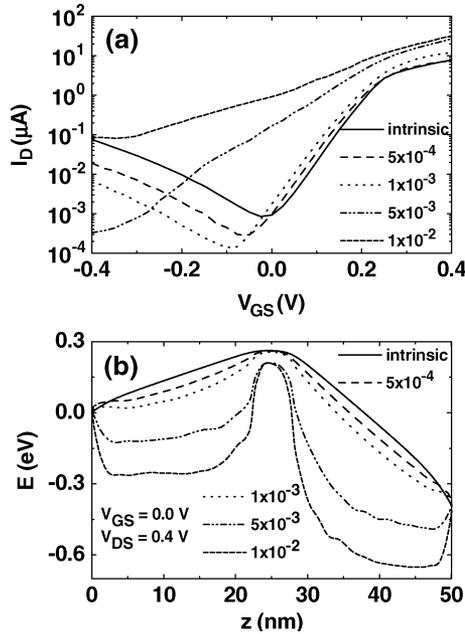


Fig. 3. (a) Simulated $\log I_D$ versus V_{GS} plots for different doping concentrations as shown. (b) Corresponding conduction band profiles in the off-state of the SB-CNTFETs for the four different uniform doping concentrations in the overlap region as well as the intrinsic CNT. The source-to-drain bias is 0.4 V.

the current distributions in Fig. 4. The gray bands in Fig. 4(a) correspond to a doping of 5×10^{-4} , and the black bands correspond to a doping of 10^{-3} . The Fermi level of the source metal is at 0 eV and the Fermi level of the drain metal is at -0.4 eV. The dashed line is at -0.45 eV in both Fig. 4(a) and (b) to serve as a reference. Near the Fermi level of the drain, the increased doping increases the electric field of the drain. One would expect this to result in increased interband tunneling and an increased ambipolar leakage current. However, in this case, with the metal drain fixed at 50 nm, the increased electric field serves to increase the tunnel barrier distance between the metal drain and the channel. At -0.45 eV, this distance is the distance along the dashed line between the 50 nm point and where it intersects the valence band. The distance to the valence band of the more heavily doped device is larger. The same also holds true on the source side. The doping increases the tunnel/thermal barrier to the ambipolar hole current. The net effect is a reduction of the minimum off-current and an increase in the on/off current ratio. We note for future reference that at 0-gate bias, for the SB-CNTFET doped at 10^{-3} , 61% of the leakage current is intraband tunneling current (electrons tunneling through the barrier in the gate region) and 34% of the leakage is interband tunneling current (holes tunneling from the drain into the valence band).

We note that there is a smooth transition from SB-CNTFET to C-CNTFET as the CNT doping is increased as shown in Fig. 3(b). For lighter doping, the devices are SB-CNTFETs. As the doping is increased, the screening increases, the bands in the source and drain become flat, the Schottky barriers become ohmic (very thin tunnel barriers), and the SB-CNTFETs become C-CNTFETs as shown in the series of band diagrams in Fig. 3(b). The appearance of the band diagram crosses over to

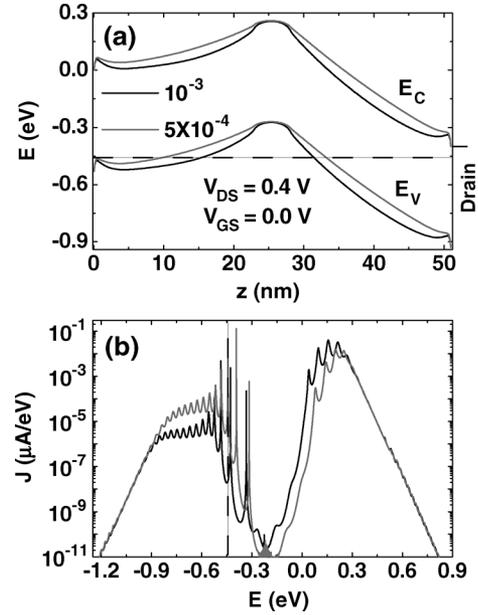


Fig. 4. (a) Conduction and valence bands of SB-CNTFET for two different dopings, 10^{-3} and 5×10^{-4} . (b) Corresponding plots of current density versus energy. The dashed line, inserted as a reference on both plots, is at an energy of -0.45 eV.

that of a C-CNTFET for the two highest doping levels, 5×10^{-3} and 1×10^{-2} .

We use these two doping levels to simulate the current and band profile of a C-CNTFET as shown in Fig. 5. Fig. 5(a) shows the simulated $\log I_D$ versus V_{GS} and 5(b) shows the band profiles at zero gate bias for C-CNTFETs with 5×10^{-3} and 1×10^{-2} dopants per carbon atom. Lesser doping concentrations can not screen the potential profile to flat band for the 50 nm CNT length between the metal source and drain. The high doping of the CNT results in a high off-current in exactly the same way as for the highly doped SB-CNTFETs. For the devices shown here with a 5 nm gate, the direct source-drain tunneling (intraband tunneling) ruins the on/off current ratio. One can reduce the interband tunneling by increasing the gate length. That, however, increases the electric field in the drain since the metal to metal source to drain length is fixed. The increased field in the drain results in a thinner interband tunnel barrier for the ambipolar current [6]. The net result is a reduction in the on/off current ratio. One can increase the intraband tunnel barrier by choosing smaller diameter, larger bandgap CNTs. However, the 1.5 nm diameter CNT is approximately the smallest diameter for which one can obtain zero Schottky barrier contacts which we consider to be an important ingredient to good CNTFET performance. Therefore, within the constraints of CNT diameters ≥ 1.5 nm and source/drain metal contacts 50 nm apart, our simulations show that a C-CNTFET structure with satisfactory on/off current ratio does not exist.

The effect of doping level was experimentally investigated by Javey *et al.* [33]. For highly doped CNTs, they found that both the on-current and the minimum leakage current increase. However, the increase in minimum leakage current is much higher and the on/off current ratio is reduced by 2 orders of magnitude

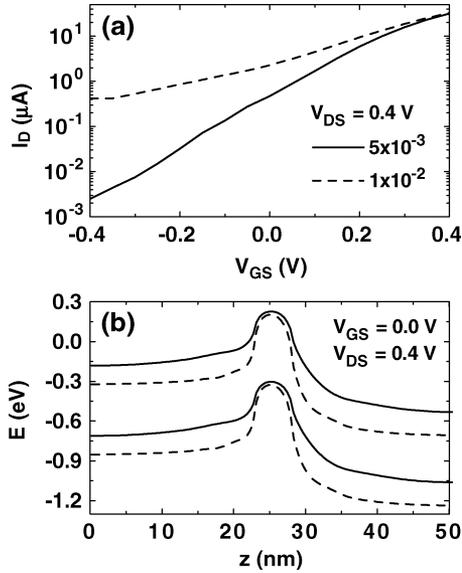


Fig. 5. The simulated (a) $\log I_D$ versus V_{GS} plots together with the (b) conduction band profiles in the off-state of the C-CNTFETs for two different values of uniform doping concentrations. The source-to-drain bias is 0.4 V.

compared to the moderately doped CNTFETs. This is consistent with our simulation study.

Next, we numerically calculate the performance metrics, namely, the gate capacitance C_g , the transconductance g_m , the kinetic inductance L_k , the intrinsic switching delay time τ_S , the intrinsic cutoff frequency f_T , and the LC frequency f_C with a doped carbon nanotube for both the SB- and C-CNTFETs. The gate capacitance is calculated from the electric flux density vector normal to the gate metal surface

$$C_g = 2\pi R \int_0^{L_g} dz \frac{\delta D_r}{\delta V_g} + 2\pi \int_{t_{ox}}^{t_{ox-ex}} r dr \frac{\delta D_z}{\delta V_g}. \quad (1)$$

The first integral is over the length of the gate along the bottom of the gate metal. The second integral is over the two sides of the gate metal. Eq. (1) gives the total gate capacitance, $C_g = C_{gs} + C_{gd}$ which includes the effect of the quantum capacitance and the fringing fields directly from the gate metal to source metal and gate metal to drain metal. The channel kinetic inductance is calculated from [51]

$$L_k = \frac{h}{4q^2} \int_0^L \frac{dz}{v(z)} \quad (2)$$

where $v(z)$ is the electron velocity in the channel and L is the CNT length. The electron velocity in the channel is calculated from

$$v(z) = \frac{I_D}{qn_e A} \quad (3)$$

where n_e is the electron concentration and A is the cross-sectional area. The magnetic inductance is ignored because the kinetic inductance is several orders of magnitude larger than the magnetic inductance [52].

Fig. 6 shows the gate capacitance, the kinetic inductance, and the transconductance for both the SB- and C-CNTFETs.

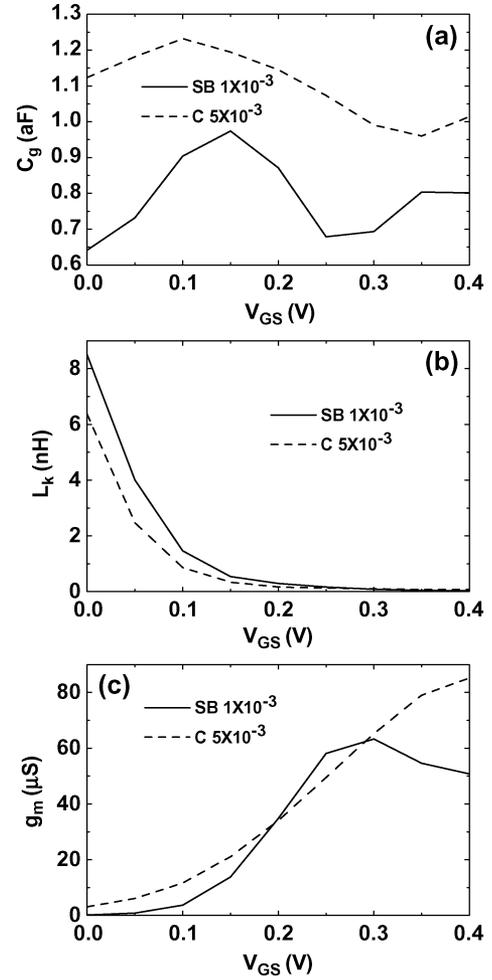


Fig. 6. (a) Gate capacitance, (b) kinetic channel inductance, and (c) transconductance versus gate bias for both the SB-CNTFET and the C-CNTFET. The uniform doping concentration for the SB-CNTFET is 10^{-3} and that for C-CNTFET is 5×10^{-3} dopant per carbon atom. The source-to-drain bias is 0.4 V.

Calculations are performed with a doping fraction of 10^{-3} dopant per carbon atom for SB-CNTFETs and 5×10^{-3} dopant per carbon atom for C-CNTFETs. The gate capacitance for SB-CNTFET in the on state ($V_{GS} = V_{DS} = 0.4$ V) is 0.8 aF, which is higher than the gate capacitance (0.5 aF) of an equivalent intrinsic SB-CNTFET. The capacitance of C-CNTFET is higher than the capacitance of SB-CNTFET due to higher doping concentration value used in C-CNTFET. The kinetic inductance is higher at relatively lower values of gate bias and higher values of doping concentrations. For comparison, if we choose the electron velocity equal to the Fermi velocity then the estimated kinetic inductance for 5 nm gate length is ≈ 0.02 nH. The transconductance of the SB-CNTFET shows a peak at a gate bias of about 0.3 V because at that gate bias there exists a flat-band condition between the source and the channel potential under the gate [22].

The intrinsic switching delay time, the intrinsic cutoff frequency, and the LC frequency are shown in Fig. 7 for both the SB-CNTFET and the C-CNTFET. The intrinsic switching delay time is calculated from $\tau_S = C_g V_{DD} / I_{ON}$, the intrinsic cutoff frequency is calculated using $f_T = g_m / (2\pi C_g)$, and the LC frequency from $f_C = 1 / (2\pi \sqrt{L_k C_g})$. The intrinsic switching

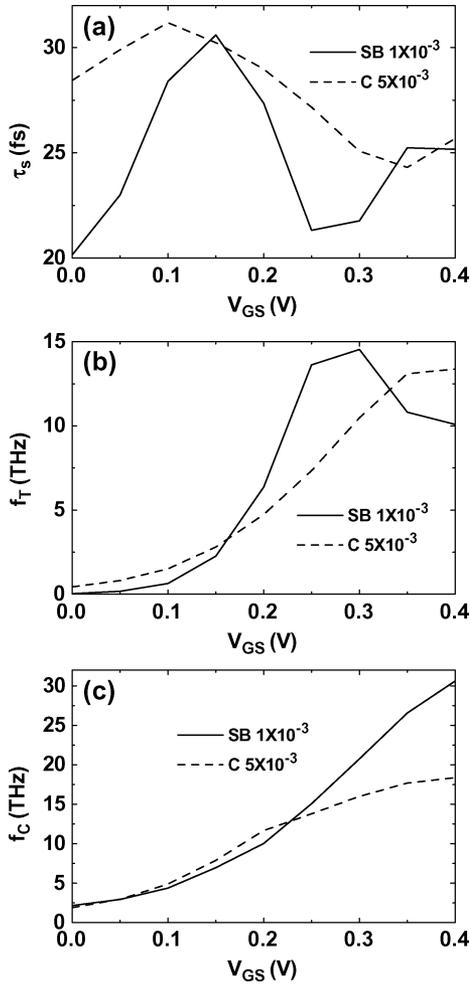


Fig. 7. (a) Intrinsic switching delay time, (b) the intrinsic cutoff frequency, and (c) the LC frequency versus gate bias for both the SB-CNTFET and the C-CNTFET. The uniform doping concentration for the SB-CNTFET is 10^{-3} and that for C-CNTFET is 5×10^{-3} dopant per carbon atom. The source-to-drain bias is 0.4 V.

delay time follows the capacitance curve and the intrinsic cutoff frequency follows the transconductance curve. The delay time is relatively small in the femtosecond range due to lower gate capacitance results from low- K gate dielectric SiO_2 [14] and the cutoff frequency is in the terahertz range. In the on-state, the intrinsic cutoff frequency of C-CNTFET is comparable to the LC frequency. Calculations (not shown here) for SB-CNTFET with a dopant concentration of 5×10^{-3} also show that the intrinsic cutoff frequency is also comparable with the LC frequency.

We next observe the effects of doping profile. For this, we consider three different Gaussian profiles shown in Fig. 2. The profiles are normalized to their maximum values of 10^{-3} for SB-CNTFET and 5×10^{-3} for C-CNTFET. Fig. 8(a) shows the simulated $\log I_D$ versus V_{GS} characteristics of the SB-CNTFETs for the three different Gaussian doping profiles shown in Fig. 2 together with the uniform doping concentration of 10^{-3} . The current-voltage response does not change with Gaussian doping in the on-state, however, we notice a slight change in the subthreshold regime. This is due to a slight modulation of the tunnel barrier length with different Gaussian doping as shown in the band profiles in Fig. 8(b) at a gate bias of 0 V. The different

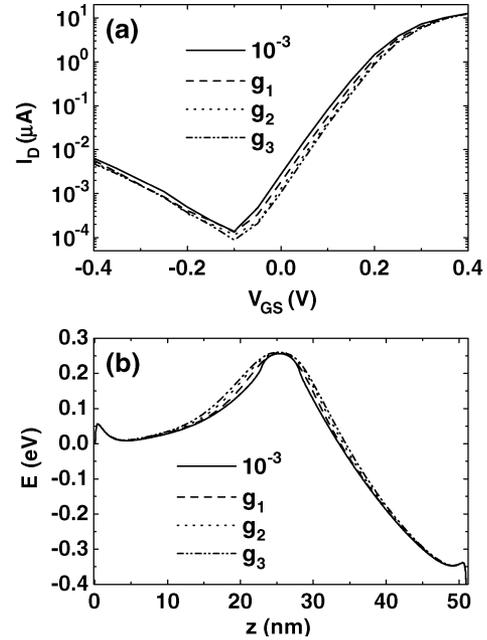


Fig. 8. The simulated (a) $\log I_D$ versus V_{GS} plots together with the (b) conduction band profiles in the off-state for the SB-CNTFETs for three Gaussian doping profiles and a step profile with the doping concentration of 10^{-3} dopant per carbon atom. Here $V_{DS} = 0.4$ V.

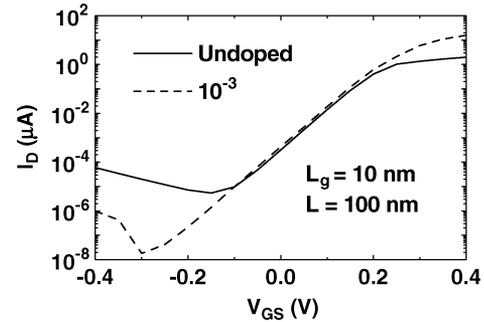


Fig. 9. The simulated $\log I_D$ versus V_{GS} plots for a 100 nm CNTFET with a 10 nm gate. The source-to-drain bias is 0.4 V and the SB-CNTFET has a step doping profile with concentration value of 10^{-3} dopant per atom.

Gaussian doping profiles leave the on-state values of τ_s and f_T unchanged for both the SB-CNTFET and the C-CNTFET.

Finally, we consider a design to increase the on-off current ratio. For the 50 nm SB-CNTFET doped at 10^{-3} dopants per carbon atom, we have a good switching delay time and cutoff frequency (see Fig. 7). However, the on/off current ratio of 5×10^4 for a 0.4 V swing from -0.1 to 0.3 V is adequate, but not great. The device shows a minimum current of $1.4 \times 10^{-4} \mu\text{A}$ and the ambipolar hole current begins to dominate at $V_{GS} = -0.1$ V. Previously we studied 50 nm devices with undoped CNTs for different asymmetric gate structures [6] and also with different gate dielectrics [14]. The best on/off current ratio (ignoring possible single electron effects) was 6×10^4 and the minimum current was $3 \times 10^{-4} \mu\text{A}$. To improve upon the 50 nm CNT, 5 nm gate, 10^{-3} doped SB-CNTFET described above, we consider the relative contribution to the leakage current from the intraband and interband tunneling processes. As noted above, direct source/drain tunneling through the gate barrier (intraband tunneling) accounts for 61% of the leakage current. One can reduce this by increasing the gate length, but this will increase the

TABLE I

FIGURES OF MERIT FOR 50 nm AND 100 nm DEVICES. THE DOPING CONCENTRATION VALUE HERE IS 10^{-3} DOPANT PER ATOM FOR BOTH THE DEVICES AND THE PARAMETER VALUES ARE LISTED AT A GATE BIAS OF 0.3 V. THE OFF CURRENT IS CORRESPONDING TO THE GATE BIAS OF -0.1 V AND THE ON CURRENT IS CORRESPONDING TO THE GATE BIAS OF 0.3 V

L(nm)	L_g (nm)	C_g (aF)	τ_s (fs)	g_m (μ S)	f_T (THz)	f_C (THz)	I_{on} (μ A)	I_{off} (μ A)	I_{min} (μ A)	on/off
50	5	0.69	21.8	63.3	14.5	20.7	6.8	1.4×10^{-4}	1.4×10^{-4}	5×10^4
100	10	1.25	31.9	88.1	11.2	16.0	5.9	9.8×10^{-6}	1.8×10^{-8}	6×10^5

interband tunneling current unless the total CNT length is increased. Therefore, to obtain a larger on/off current ratio with almost unipolar characteristics and a very low value of minimum current, we consider a 100 nm CNT with a 10 nm gate and same optimal doping concentration of 10^{-3} dopants per atom, and we compare it with an equivalent undoped device.

The current–voltage characteristics are shown in Fig. 9. With the same 0.4 V swing (-0.1 to 0.3 V), the doped SB-CNTFET has an on/off current ratio of 6×10^5 with an inverse subthreshold slope of 62 mV/dec. Furthermore, the SB-CNTFET has almost unipolar characteristics for the bias range studied here and it has higher on-current and very low value of minimum current. An undoped version of this 100 nm SB-CNTFET has an on/off current ratio of 10^5 with an inverse subthreshold slope of 63 mV/dec. We have not optimized with respect to different dielectrics, but we note that in the previous studies of these underlapped geometries, the dielectric has little effect on the potential profile and the dc device characteristics for a 2 nm thick dielectric (see [14, Figs. 2, 3]).

The increased on–off current ratio does come at a price. Doubling the CNT length increases the delay time and reduces the cutoff frequencies. The parameter values for the best 50 nm and the best 100 nm SB-CNTFETs are summarized in Table I.

IV. CONCLUSION

For ultrascaled CNTFETs in which the source/drain metal contacts lie 50 nm apart, there is no MOSFET-like contact CNTFET with an acceptable on–off current ratio using a CNT of diameter ≥ 1.5 nm and a source/drain voltage ≥ 0.4 V. For CNTFETs with source/drain metal contacts either 50 nm or 100 nm apart, there is an optimal doping concentration of 10^{-3} dopants per atom. The maximum on–off current ratios for the 50 nm CNT/5 nm gate and the 100 nm CNT/10 nm gate SB-CNTFETs are 5×10^4 and 6×10^5 , respectively. Changing the doping profile from step to Gaussian makes essentially no change in the figures of merit.

REFERENCES

- [1] J. Guo, J. Wang, E. Polizzi, S. Datta, and M. Lundstrom, "Electrostatics of nanowire transistors," *IEEE Trans. Nanotechnol.*, vol. 2, no. 4, pp. 329–334, Dec. 2003.
- [2] J. Guo, S. Goasguen, M. Lundstrom, and S. Datta, "Metal–insulator–semiconductor electrostatics of carbon nanotubes," *Appl. Phys. Lett.*, vol. 81, no. 8, pp. 1486–1488, Aug. 19, 2002.
- [3] D. L. John, L. C. Castro, J. Clifford, and D. L. Pulfrey, "Electrostatics of coaxial schottky-barrier nanotube field-effect transistors," *IEEE Trans. Nanotechnol.*, vol. 2, no. 3, pp. 175–180, Sep. 2003.
- [4] J. P. Clifford, D. L. John, L. C. Castro, and D. L. Pulfrey, "Electrostatics of partially gated carbon nanotube FETs," *IEEE Trans. Nanotechnol.*, vol. 3, no. 2, pp. 281–286, Jun 2004.

- [5] K. Alam and R. K. Lake, "Performance of 2 nm gate length carbon nanotube field-effect transistors with source/drain underlaps," *Appl. Phys. Lett.*, vol. 87, no. 7, p. 073104, 2005.
- [6] K. Alam and R. K. Lake, "Leakage and performance of zero-schottky-barrier carbon nanotube transistors," *J. Appl. Phys.*, vol. 98, no. 6, p. 064307, 2005.
- [7] J. Appenzeller *et al.*, "Comparing carbon nanotube transistors - the ideal choice: A novel tunneling device design," *IEEE Trans. Electron Devices*, vol. 52, no. 12, pp. 2568–2576, Dec. 2005.
- [8] S. O. Koswatta, M. S. Lundstrom, and D. E. Nikonov, "Band-to-band tunneling in a carbon nanotube metal-oxide-semiconductor field-effect transistor dominated by phonon-assisted tunneling," *Nano Lett.* vol. 7, no. 5, pp. 1160–1164, 2007 [Online]. Available: <http://www.dx.doi.org/10.1021/nl062843f>
- [9] J. Guo, S. Datta, and M. Lundstrom, "A numerical study of scaling issues for schottky-barrier carbon nanotube transistors," *IEEE Trans. Electron Devices*, vol. 51, no. 2, pp. 172–177, Feb. 2004.
- [10] S. Heinze, M. Radosavljevic, J. Tersoff, and P. Avouris, "Unexpected scaling of the performance of carbon nanotube schottky-barrier transistors," *Phys. Rev. B*, vol. 68, no. 2, p. 235418, 2003.
- [11] M. Radosavljevic, S. Heinze, J. Tersoff, and P. Avouris, "Drain voltage scaling in carbon nanotube transistors," *Appl. Phys. Lett.*, vol. 83, no. 12, pp. 2435–2437, 2003.
- [12] S. J. Wind, M. Radosavljevic, J. Appenzeller, and P. Avouris, "Transistor structures for the study of scaling in carbon nanotubes," *J. Vac. Sci. Technol. B*, vol. 21, pp. 2856–2859, 2003.
- [13] J. Appenzeller, J. Knoch, R. Martel, V. Derycke, S. Wind, and P. Avouris, "Short-channel like effects in schottky barrier carbon nanotube field-effect transistors," in *Tech. Dig.—Int. Electron Devices Meet.*, 2002, vol. 11, no. 2, pp. 285–288.
- [14] K. Alam and R. K. Lake, "Dielectric scaling of a zero-schottky-barrier, 5 nm gate, carbon nanotube transistor with source/drain underlaps," *J. Appl. Phys.* vol. 100, no. 2, pp. 024317-1–024317-7, Jul. 2006 [Online]. Available: <http://www.dx.doi.org/10.1063/1.2218764>
- [15] J. Guo, S. Datta, M. Lundstrom, M. Brink, P. McEuen, A. Javey, H. Dai, H. Kim, and P. McIntyre, "Assessment of silicon MOS and carbon nanotube FET performance limits using a general theory of ballistic transistors," *Dig. Int. Electron Devices Meeting (IEDM 2002)*, vol. 2, no. 2, pp. 711–714, .
- [16] A. Javey, M. Shim, and H. Dai, "Electric properties and devices of large-diameter single-walled carbon nanotubes," *Appl. Phys. Lett.*, vol. 80, no. 7, pp. 1064–1066, 2002.
- [17] J. Guo, M. Lundstrom, and S. Datta, "Performance projections for ballistic carbon nanotube field-effect transistors," *Appl. Phys. Lett.*, vol. 80, no. 17, pp. 3192–3194, Apr. 29, 2002.
- [18] D. V. Singh, K. A. Jenkins, J. Appenzeller, D. Neumayer, A. Grill, and H. S. P. Wong, "Frequency response of top-gated carbon nanotube field-effect transistors," *IEEE Trans. Nanotechnol.*, vol. 3, no. 3, pp. 383–387, Sep. 2004.
- [19] J. Appenzeller and D. J. Frank, "Frequency dependent characterization of transport properties in carbon nanotube transistors," *Appl. Phys. Lett.*, vol. 84, no. 10, pp. 1771–1773, 2004.
- [20] S. Heinze, J. Tersoff, R. Martel, V. Derycke, J. Appenzeller, and P. Avouris, "Carbon nanotubes as schottky barrier transistors," *Phys. Rev. Lett.*, vol. 89, no. 10, p. 106801, Sep. 2, 2002.
- [21] T. Nakanishi, A. Bachtold, and C. Dekker, "Transport through the interface between a semiconducting carbon nanotube and a metal electrode," *Phys. Rev. B*, vol. 66, no. 7, pp. 073307-1–073307-4, Aug. 2002.
- [22] K. Alam and R. Lake, "Performance metrics of a 5 nm, planar, top gate, carbon nanotube on insulator (COI) transistor," *IEEE Trans. Nanotechnol.*, vol. 6, no. 2, pp. 186–190, Mar. 2007.
- [23] A. Javey, J. Guo, Q. Wang, M. Lundstrom, and H. Dai, "Ballistic carbon nanotube field-effect transistors," *Nature*, vol. 424, no. 6949, pp. 654–657, Aug. 7, 2003.

- [24] A. Javey, J. Guo, M. Paulsson, Q. Wang, D. Mann, M. Lundstrom, and H. Dai, "High-field quasiballistic transport in short carbon nanotubes," *Phys. Rev. Lett.*, vol. 92, no. 10, p. 106804, Mar. 2004.
- [25] A. Javey, J. Guo, D. B. Farmer, Q. Wang, D. Wang, R. G. Gordon, M. Lundstrom, and H. Dai, "Carbon nanotube field-effect transistors with integrated ohmic contacts and high- κ gate dielectrics," *Nano Lett.*, vol. 4, no. 3, pp. 447–450, Mar. , 2004.
- [26] A. Javey, J. Guo, D. B. Farmer, Q. Wang, E. Yenilmez, R. G. Gordon, M. Lundstrom, and H. Dai, "Self-aligned ballistic molecular transistors and electrically parallel nanotube arrays," *Nano Lett.*, vol. 4, no. 7, pp. 1319–1322, Jul. 2004.
- [27] Z. Chen, J. Appenzeller, J. Knoch, Y. Lin, and P. Avouris, "The role of metal-nanotube contact in the performance of carbon nanotube field-effect transistors," *Nano Lett.*, vol. 5, no. 7, pp. 1497–1502, 2005.
- [28] W. Kim, A. Javey, R. Tu, J. Cao, Q. Wang, and H. Dai, "Electrical contacts to carbon nanotubes down to 1 nm in diameter," *Appl. Phys. Lett.*, vol. 87, no. 17, pp. 173101-1–173101-3, Oct. 2005.
- [29] A. Bachtold, P. Hadley, T. Nakanishi, and C. Dekker, "Logic circuits with carbon nanotube transistors," *Sci*, vol. 294, no. 5545, pp. 1317–1320, Nov. 9, 2001.
- [30] A. Javey, Q. Wang, A. Ural, Y. Li, and H. Dai, "Carbon nanotube transistor arrays for multistage complementary logic and ring oscillators," *Nano Lett.*, vol. 2, no. 9, pp. 929–932, Sep. 2002.
- [31] Y.-C. Tseng, P. Xuan, A. Javey, R. Malloy, Q. Wang, J. Bokor, and H. Dai, "Monolithic integration of carbon nanotube devices with silicon MOS technology," *Nano Lett.*, vol. 4, no. 1, pp. 123–127, Jan. 2004.
- [32] M. Radosavljevic, J. Appenzeller, and P. Avouris, "High performance of potassium n-doped carbon nanotube field-effect transistors," *Appl. Phys. Lett.*, vol. 84, pp. 3693–3695, 2004.
- [33] A. Javey, R. Tu, D. B. Farmer, J. Guo, R. G. Gordon, and H. Dai, "High performance n-type carbon nanotube field-effect transistors with chemically doped contacts," *Nano Lett.*, vol. 5, no. 2, pp. 345–348, 2005.
- [34] L. Duclaux, "Review of the doping of carbon nanotubes (multiwalled and single-walled)," *Carbon*, vol. 40, no. 10, pp. 1751–1764, Aug. 2002.
- [35] V. Derycke, R. Martel, J. Appenzeller, and P. Avouris, "Controlling doping and carrier injection in carbon nanotube transistors," *Appl. Phys. Lett.*, vol. 80, no. 15, pp. 2773–2775, Apr. 15, 2002.
- [36] M. Bockrath, J. Hone, A. Zettl, P. L. McEuen, A. G. Rinzler, and R. E. Smalley, "Chemical doping of individual semiconducting carbon-nanotube ropes," *Phys. Rev. B*, vol. 61, no. 16, pp. R10606–R10608, Apr. 15, 2000.
- [37] J. Kong, C. Zhou, E. Yenilmez, and H. Dai, "Alkaline metal-doped n-type semiconducting nanotubes as quantum dots," *Appl. Phys. Lett.*, vol. 77, no. 24, pp. 3977–3979, Dec. 11, 2000.
- [38] J. Knoch, S. Mantl, and J. Appenzeller, "Comparison of transport properties in carbon nanotube field-effect transistors with schottky contacts and doped source/drain contacts," *Solid-State Electron.*, vol. 49, pp. 73–76, 2005.
- [39] G. Fiori, G. Iannaccone, M. Lundstrom, and G. Klimeck, "Three-dimensional atomistic simulation of carbon nanotube FETs with realistic geometry," in *Proc. ESSDERC*, 2005, pp. 537–540.
- [40] G. Fiori, G. Iannaccone, and G. Klimeck, "Performance of carbon nanotube field effect transistors with doped source and drain extensions and arbitrary geometry," in *Tech. Dig. Int. Electron Devices Meeting (IEDM 2005)*, pp. 522–525.
- [41] D. L. John and D. L. Pulfrey, "Issues in the modeling of carbon nanotube FETs: Structure, gate thickness, and azimuthal asymmetry," *J. Comput. Electron.*, vol. 6, no. 1-3, pp. 175–178, Sep. 2007, in press.
- [42] N. A. Bruque, K. Alam, R. R. Pandey, R. K. Lake, J. P. Lewis, X. Wang, F. Liu, C. S. Ozkan, M. Ozkan, and K. L. Wang, "Self-assembled carbon nanotubes for electronic circuit and device applications," *J. Nanoelectron. Optoelectron.* vol. 1, no. 1, pp. 74–81, Apr. 1, 2006 [Online]. Available: <http://www.dx.doi.org/10.1166/jno.2006.007>
- [43] J. G. Fossum, M. M. Chowdhury, V. P. Trivedi, T. J. King, Y. K. Choi, J. An, and B. Yu, "Physical insights on design and modeling of nanoscale FinFETs," in *Tech. Dig. Int. Electron Devices Meeting (IEDM 2003)*, vol. 3, pp. 679–682.
- [44] V. P. Trivedi, J. G. Fossum, and M. M. Chowdhury, "Nanoscale FinFETs with gate-source/drain underlap," *IEEE Trans. Electron Devices*, vol. 52, no. 1, pp. 56–62, Jan. 2005.
- [45] F. Boeuf *et al.*, "16 nm planar nMOSFET manufacturable within state-of-the-art CMOS process thanks to specific design and optimisation," in *Tech. Dig. Int. Electron Devices Meeting (IEDM 2001)*, vol. 1, pp. 637–640.
- [46] R. Gusmeroli *et al.*, "2D QM simulation and optimisation of decanano nonoverlapped MOS devices," in *Tech. Dig. Int. Electron Devices Meeting (IEDM 2003)*, , vol. 3, pp. 225–228.
- [47] Y.-M. Lin, J. Appenzeller, Z. Chen, Z.-G. Chen, H. M. Cheng, and Ph. Avouris, "High-performance dual-gate carbon nanotube FETs with 40-nm gate length," *IEEE Electron Device Lett.*, vol. 26, no. 11, pp. 823–825, Nov. 2005.
- [48] J. W. Mintmire, D. H. Robertson, and C. T. White, "Properties of fullerene nanotubules," *J. Phys. Chem. Solids*, vol. 54, no. 12, pp. 1835–1840, Dec. 1993.
- [49] M. P. L. Sancho, J. M. L. Sancho, and J. Rubio, "Highly convergent schemes for the calculation of bulk and surface green functions," *J. Phys. F. Met. Phys.*, vol. 15, no. 4, pp. 851–858, Apr. 1985.
- [50] M. Galperin, S. Toledo, and A. Nitzan, "Numerical computation of tunneling fluxes," *J. Chem. Phys.*, vol. 117, no. 23, pp. 10817–10826, Dec. 2002.
- [51] J. Guo, S. Hasan, A. Javey, G. Bosman, and M. Lundstrom, "Assessment of high-frequency performance potential of carbon nanotube transistors," *IEEE Trans. Nanotechnol.*, vol. 4, no. 6, pp. 715–721, Nov. 2005.
- [52] P. J. Burke, "Luttinger liquid theory as a model of the gigahertz electrical properties of carbon nanotubes," *IEEE Trans. Nanotechnol.*, vol. 1, pp. 129–144, 2002.

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