A 1.2V improved operational amplifier for bio-medical applications

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Abstract: In this paper, an improved low-power Complementary Metal Oxide Semiconductor (CMOS) programmable operational amplifier for bio-medical applications is presented. The op-amp includes a rail-to-rail input stage, folded cascode stage with class AB biasing and a constant Gm stage. The op-amp is programmed to operate in low-power mode and low noise mode. Simulation results show that the circuit attains a dc open loop gain of 97.75 dB and Common Mode Rejection Ratio (CMRR) of 112.41 dB under a 22 kΩ and 13.5 pF load. The op-amp is realised in 130 nm CMOS technology using Synopsis tool.

Keywords: operational amplifier; bio-medical; low power; low noise.

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1 Introduction

Currently, there is an ever-growing demand for low-power and low-noise mixed signal integrated circuits, in portable medical systems. So, a high level of system integration is required to handle bio-potential system. The most commonly observed bio-potentials used for medical diagnoses are monitored non-invasively with electrodes placed on the surface of the skin (Lee et al., 2006a, 2006b). These include the Electrocardiogram (ECG), which monitors heart activity; the Electromyogram (EMG), which monitors other muscle activity in the body, and the Electroencephalolgram (EEG), which monitors electrical activity in the brain via weak potentials on the scalp. Several approaches are carried out to integrate analogue front-end using CMOS technology. Generally, the integrated chip offers a relatively low-cost product for both ECG and EEG signals, but with high-power consumption. To overcome this problem, programmable components with adjustable trade-off between noise and power dissipation are embedded in the same chip. Since the main noise source in the recording chain of bio-medical signals is found in the first component, i.e., the preamplifier, which consists of operational amplifiers, a programmable operational amplifier (op-amp) is a key component (Van Helleputte et al., 2008).

Programmable op-amps are designed based on the circuit topology in Hogervorst and Huijsing (1996). The op-amps presented in Bronskowski and Schroeder (2007) and Meier auf der Heide et al. (2007) uses this topology for its design and is implemented using 0.35 μm CMOS technology with a supply voltage of 3.3 V. It occupies large area and has large power consumption. So, the supply voltage of programmable op-amps is kept around 1 V to ensure less power dissipation. But, conventional analogue circuit topologies will not work with this supply voltage because as the device sizes are scaled down, the threshold voltage of MOS transistors does not reduce, as this could cause increased leakage currents. This problem can be alleviated by using alternate MOSFETS like floating gate MOSFETs, bulk driven MOSFETs and DTMOS. A 1.2 V op-amp has been integrated in a 0.35 μm CMOS process (Riiisanen-Ruotsalainen et al., 2000) using floating-gate input transistors to increase the input common mode voltage range of the op-amp, but owing to the capacitive division, the input signal gets attenuated resulting in poor gain, less gain bandwidth product and inferior noise properties. In bulk driven transistors (Lasanen et al., 2000), the threshold voltage limitation disappears but the devices have lower transconductance value because of smaller control capacitance of the depletion layer, larger parasitic capacitance that lowers frequency and higher input referred noise. Op-amp design based on dynamic threshold voltage (DTMOS) transistors is preferred for low voltage, low power bio-medical applications (Achigui et al., 2003). The body and the gate of this DTMOS transistor are biased at the same potential. So, it is capable of processing ultra low-amplitude light signals and is used to build the front-end receiver part of a Near Infrared Spectrore Flectometry (NIRS) device. On the other hand, the op-amp is susceptible to flicker noise (*1/f*), which makes it very harmful in low-frequency bio-medical applications because of its power spectrum and voltage offset. So, the programming ability of the op-amp should be exploited to work in both low-noise mode and low-power mode if different medical applications are combined in one chip. An application of this type of Op-amp is used in the analogue front-end of a System on Chip (SoC) for bio-medical signal acquisition (Hafkemeyer et al., 2007). For example, the op-amp is programmed in low-noise mode for sensitive EEG recordings or low-power mode for mobile ECG applications. In contrast to conventional op-amps, programmable op-amps have the advantage of being adaptable to system specification.

In this paper, an improved programmable op-amp, which overcomes the disadvantages of conventional op-amps, is proposed and implemented using 130 nm CMOS technology with 1.2 V supply voltage. Section 2 describes the basic operation and design implementation of the existing op-amp architecture. The improved op-amp's architecture and its design are discussed in Section 3. Simulation results are provided in Section 4 and conclusions are presented in Section 5.

2 Bio-medical systems

2.1 Introduction

In recent years, there is an ever-growing demand for low-power and low-noise mixed signal integrated circuits for applications such as portable medical systems. In these applications, the supply voltage is being scaled down to reduce overall power consumption. The need for analogue circuits in nanometre CMOS technology is due to the necessity to combine both digital and analogue blocks into one system forming SoC (Busze et al., 2010). Digital CMOS is always the preferred technology for the fabrication process owing to its efficient economic costs. As a result, contemporary analogue circuits must not only operate with low supply voltages, but should also be realisable in typical digital CMOS processes.

One of the most crucial building blocks in analogue systems is the operational amplifier. Significant research has been devoted over the past 20 years for the development and enhancement of the op-amp structure (Harrison, 2007; Stockstad and Yoshizawa, 2002; Blalock et al., 1998). Yet most historical topologies fell short of providing satisfactory performance below 3 V power supplies. Historical structures typically consisted of an input stage and one or two intermediate gain stages. These gain stages had to provide high DC gain, which could be achieved by using cascading. Since op amps are the most critical building blocks in all analogue systems, the objective of this work is to study the theory and design of low-power and low-noise op amps and analyse it to make to be a programmable.

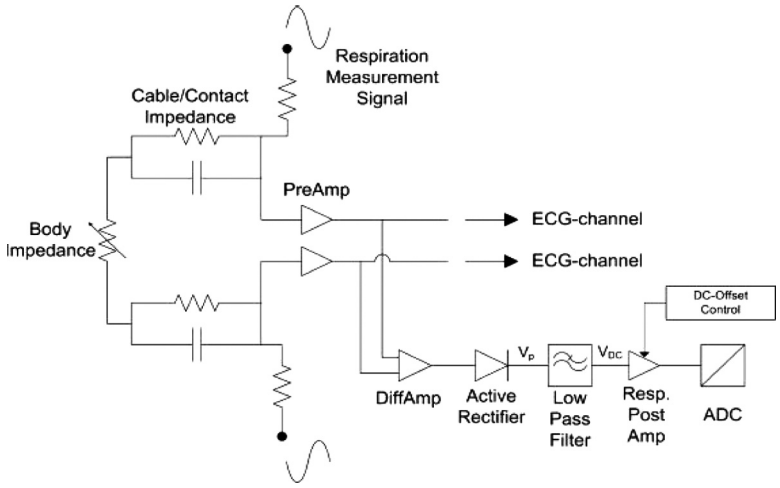
2.2 Applications

The operational amplifier (op-amp) is the most important building block for use in mixed signal SoC applications (Van Helleputte et al., 2008). It is an active element with high-gain designed to perform a specified signal-processing operation. A programmable op-amp used in bio-medical application amplifies the weak bio-potential signal to large amplitude signal and is programmed to handle both noise and power. The basic architecture of the analogue front-end of a respiration-monitoring system is as shown in Figure 1.

The respiration-monitoring system is fully integrated on chip with the exception of an external capacitor for low-pass filtering. The measurement principle is based on bio-electric impedance measurement on the patient's thorax and allows the measurement of respiration concurrently with an ECG-measurement using two ECG-electrodes. The circuit is also used to detect open-leads by measuring the absolute impedance between leads. If this impedance exceeds a certain threshold, the leads are assumed to be open. The on-chip oscillator generates two differential 40 kHz sine-signals, which are applied to

the body-electrodes through additional impedances forming a voltage divider. The applied carrier-signal is modulated by a change of body impedance owing to breathing of the patient.

Figure 1 Basic architecture of analogue front-end



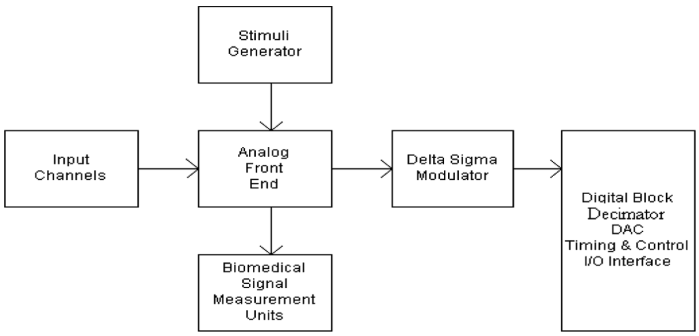
After the preamplifiers, both the ECG-signal and the modulated carrier are present. Because the carrier is located at 40 kHz, which is removed by the low-pass filter at the end of the analogue channel, respiration measurement does not disturb ECG measurement. After the preamplifiers, the differential carrier is converted to a single-ended signal. The very-low-frequency (<1 Hz) respiration signal modulated on the carrier signal can be considered as a slow varying DC-signal. To extract this DC-signal, an active full-wave rectifier is used followed by a Sallen-Key low-pass filter. The obtained respiration signal is too small (in the microvolt range) to be directly A/D converted. Therefore, an adjustable postamplifier is used to amplify this signal. The amplified respiration signal is finally A/D converted and the digitised signal can be read out by the on-chip DSP.

Additionally, different amplifier designs have been investigated and developed for recording bio-potentials such as cortical signals (Hogervorst and Huijsing, 1996; Lee et al., 2006a, 2006b; Mingjun et al., 2008). These amplifiers are usually used in implantable bio-medical devices with the amplifier inputs connected to microelectrode arrays. Bio-potentials obtained from the microelectrode arrays usually have a power spectrum between a few Hertz and a few kiloHertz with an amplitude range between a few tens of Volts and a few mV. The most commonly used bio-medical signals amplitude and frequency range is provided in Table 1. As a result, the amplifiers are required to have low input referred noise. Since there are many amplifiers in an implantable bio-medical device, the overall power dissipation of the amplifiers has to be kept very low such that the entire device can be powered directly by inductive coupling from an RF field or from an inductively rechargeable battery. To effectively use the available power in the implantable device, the supply voltage has to be low as long as the output signal swing and the dynamic range are not degraded. As a result, low power, low voltage rail-to-rail amplifiers must be developed for amplification, buffering, etc. The system architecture of entire SoC is as shown in Figure 2.

Table 1 Commonly used bio-medical signals

Signal	*Frequency*	*Amplitude*
ECG	0.05–250 Hz	5 μV–8 mV
EEG	0.5–100 Hz	2 μV–200 μV
EP	2 kHz–5 kHz	20 nV–20 μV
EMG	0.01 Hz–10 kHz	50 μV–10 mV

Figure 2 System architecture of entire system on chip



2.3 Future research

Currently, there is a great demand for low-power, small-size ambulatory bio-potential acquisition systems. The analogue readout front-end remains the crucial block in this system too. Normally, in the present scenario, patients are connected to a bulky mains-powered monitoring system, which restricts the mobility of the patients and provides discomfort. So, the goal is to implement a bio-potential acquisition system that is comfortable and offers mobility with long-term power autonomy, high signal quality and configurability for different bio-potential signals. Thus, the patient's quality of life is improved using this system (Zhang et al., 2009). The entire acquisition system is divided into two parts: Analogue Front End and ADC Back End. The Analogue Front End is a combination of an amplifier and filter, which amplifies the weak bio-medical signals to large amplitude and filters out unwanted noise. The back end is used for digitised signal processing.

In addition, recent development in wireless communication technologies has made home telemonitoring an emerging field. The monitoring is done at home (Hsu et al., 2007) and it has led to very high patient satisfaction. This in turn brings down the medical cost, as this patient has to spend fewer days in hospital than a normal patient. An important consideration in the integration of analogue and digital components is that the resulting SoC should be in wide range of use so that it is usable in low-cost 24 h/7 d medical homecare applications.

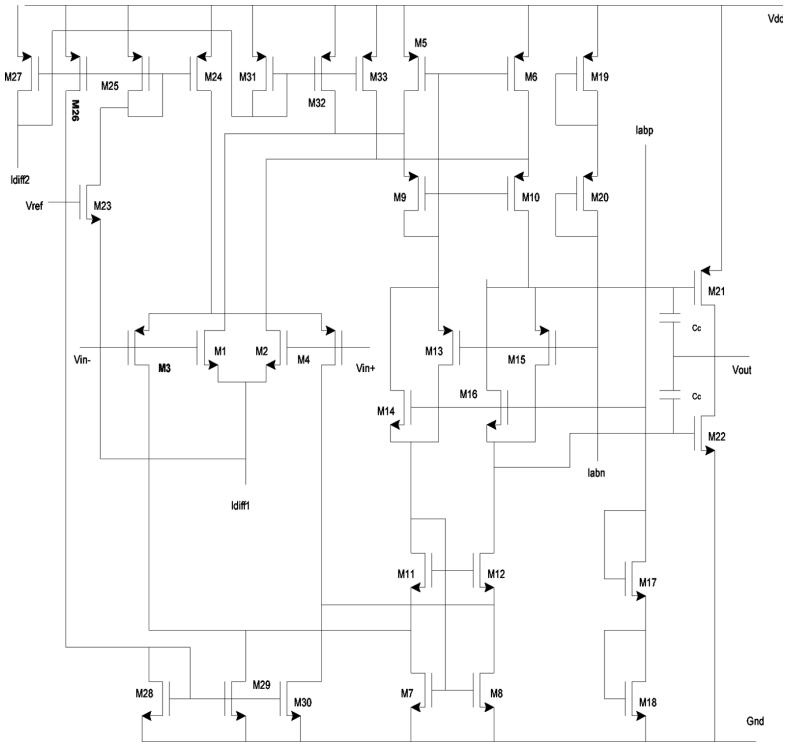
Also, wearable and portable systems have been employed in various healthcare systems. With the recent trends in wireless communication, human body channel communication (Huang et al., 2009) is getting popular in transmitting images and signals with high fidelities and good transmission rate (Mbps level). The energy consumption for this kind of wireless link has to be very minimum. Thus, the analogue front-end that uses the wide band signalling scheme operates at lower operational frequency with very high sensitivity.

3 Existing op-amp architecture and design

3.1 Introduction

The objective of work is to implement the most promising, programmable, low-power and low-noise operational amplifier as a preamplifier for bio-medical applications. It consumes less power, offers less noise and amplifies the weak cortical input signals to a larger extent. The existing op-amp architecture in Hafkemeyer et al. (2008) has improvements in terms of gain, power and noise performance and is made to work within a programming range of being in low-noise mode at one end and low-power mode at the other. The complete schematic of the op-amp is shown in Figure 3. The rail-to-rail input stage is formed by the transistors M1–M4. The folded cascode stage consists of transistors M5–M20 with M21 and M22 transistors forming the class AB output stage. The programmability of the op-amp is ensured by transistors M29, M30, M32 and M33, which forms the constant Gm stage. The external bias currents Idiff1, 2 and Iabn, p are set to make the op-amp work in low power, medium power and high power mode. This in turn accomplishes the programmability of the op-amp. The biasing voltage Vbcn and Vbcp acts as reference voltage for the cascode stage and Cc is used for miller compensation.

Figure 3 Existing op-amp architecture



When the common mode voltage, $V_{cm,in}$, is set at half the supply voltage, M23 is biased to carry an equal current of Idiff1/2 by the current mirror formed by transistors M24 and

M25. This equal distribution of current in NMOS and PMOS transistors results in constant transconductance value Gm. M26 and M27 transistors carry equal current of Idiff1/2 and current Idiff2 is distributed between M27 and M31. If $V_{cm,in}$ reaches higher value, PMOS input pair and M23 is turned off setting I_{D32}, I_{D33} to Idiff2/2. So, the current Idiff1 is carried only by the NMOS pair doubling the transconductance value. When $V_{cm,in}$ reaches lower value, NMOS input pair shuts off and I_{D29}, I_{D30} is set to Idiff1/2. So, the current Idiff2 is now carried only by the PMOS pair doubling the transconductance value. Thus, the programmability of the op-amp is achieved with input transistors biased in weak inversion region and output transistors biased in strong inversion region. So, the relation in equation (1) is obtained.

$$\frac{gm2_2}{gm_4} \sim \frac{\sqrt{ID2_2}}{ID_4}. \tag{1}$$

Idiff1 and Idiff2 are used as bias currents for the input stage and external currents Iabn and Iabp are used for the folded cascode and output stage. Proper setting of these currents makes the op-amp to work in low-power mode (P_{low}), medium-power mode (P_{medium}) and high-power mode (P_{high}) (Hafkemeyer et al., 2008).

3.2 Op-amp design using low supply voltage

The minimum supply voltage to be maintained by the op-amp is set by biasing the folded-cascode transistors in strong inversion region. Equations (2) and (3) represent the constraints for the minimum supply voltage with the overdrive voltage $Vov = Vgs - Vth$.

$$Vdd \geq 5 * Vov \tag{2}$$

$$Vdd \geq 2 * Vgs + Vov. \tag{3}$$

With maximum threshold voltage, equation (3) can be modified as

$$Vth, \max \leq \frac{1}{2} * (Vdd - 3 * Vov). \tag{4}$$

The minimum supply voltage obtained with an overdrive voltage of 0.2 V is 1 V. In this design, a 1.2 V supply voltage is maintained to satisfy equation (2).

4 Proposed op-amp architecture

In bio-medical measurements, the Common Mode Rejection Ratio (CMRR) is an important parameter indicating the ability to reject the power line interference. The Linearity, Power Supply Rejection Ratio (PSRR) and Signal to Noise Ratio (SNR) are all related with CMRR. There are two important limitations to be considered for CMRR calculation when active electrodes are used. One is the potential divider effect, i.e., any difference in the skin-electrode impedance will limit the maximal CMRR. Another important parameter is that while increasing the output resistance of the amplifier using the electrodes, the gain of

amplifier is affected. The CMRR and gain can be improved by replacing diode-connected transistors in the existing op-amp architecture by current mirror circuits. The current mirror is one of the basic building blocks of analogue integrated circuits. Current mirrors are used to achieve high accuracy and high output impedance and thereforth high gain. So in the existing architecture, the diode-connected transistors M17, M18, M19 and M20 are replaced with Simple, Widlar, Cascode and Wilson current mirror circuits and their performances are compared.

4.1 Current mirrors

An ideal current mirror (Johns and Martin, 1997) is a circuit with infinite output impedance, zero input resistance and minimum output voltage. The simple current mirror circuit is shown in Figure 4. The transistors M1 and M2 are in the saturation region. A reference current flows through the diode-connected transistor M1 and the same amount of current is mirrored at the output. The minimum output voltage is *Von* and the output resistance $Rout = r_{ds}$. The output impedance is low in submicron technologies and the current gain accuracy is poor since $V_{DS1} \neq V_{DS2}$.

Widlar current source circuit is shown in Figure 5. It uses source-degenerated resistors R_1 and R_2 in its configuration. There is practical limitation on choosing the resistor value. Though the performance is improved, it has trade-off between power and area. It is better if transistors are replaced for resistors.

Figure 4 Simple current mirror

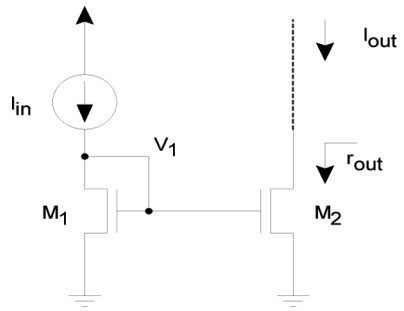
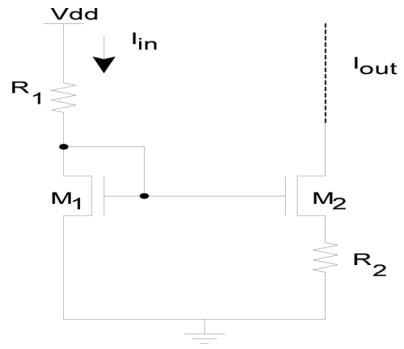


Figure 5 Widlar current mirror



In a cascode current mirror, cascoding increases the accuracy and transistors are connected as shown in Figure 6. The output resistance is given as $Rout = g_m r_{ds}^2$ and current gain is excellent as $V_{DS1} = V_{DS2}$. Thus, the output resistance and current gain accuracy is improved. The modification of cascode current mirror is a Wilson current mirror, which performs approximately same as a cascode current mirror. The circuit diagram of the Wilson current mirror is shown in Figure 7. It uses a shunt series feedback to increase the gain accuracy. The output resistance is quite the same as with cascode current mirror but setting up the output voltage constant is difficult. When the output current increases, the output voltage becomes larger by two times the square root of output current. Thus, a cascode current mirror circuit excels (Johns and Martin, 1997) in its performance comparing all the other current mirrors.

Figure 6 Cascode current mirror

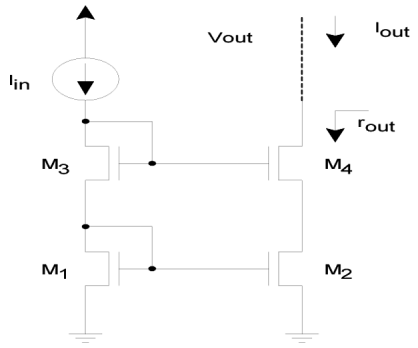
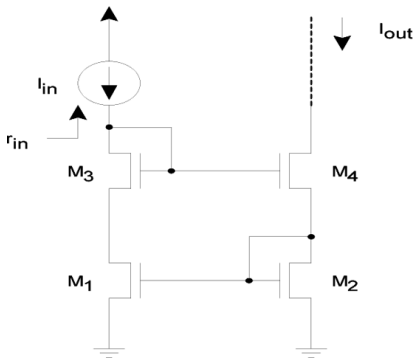


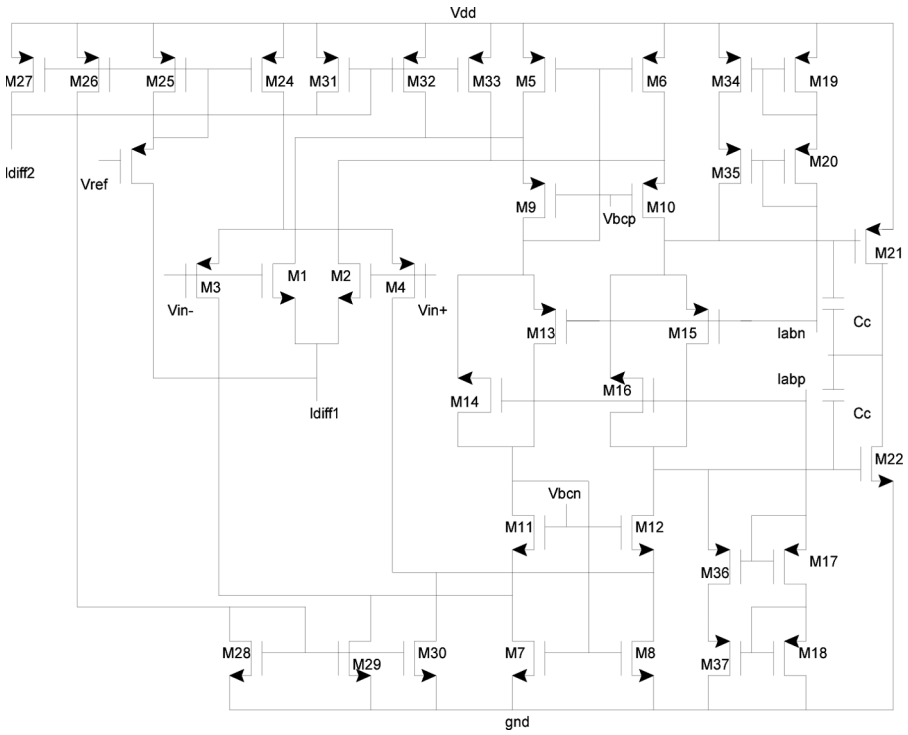
Figure 7 Wilson current mirror



Cascode stages are widely used in different circuits to boost gain in amplifiers or to obtain a higher precision on current mirrors, without adding new current-consuming stages. In the op-amp circuit, the cascode current mirror outperforms in terms of CMRR, Gain, Slew rate and noise. The proposed bio-medical op-amp with cascode current mirror is shown in Figure 8. In the existing op-amp architecture, diode-connected transistors M17 and M18 are replaced with NMOS cascode mirror transistors M17, M18, M36 and M37 and diode-connected transistors M19 and M20 are replaced with PMOS cascode mirror

transistors M19, M20, M34 and M35. So, it includes both NMOS and PMOS current mirror at the output stage to increase the gain and CMRR and reduce the noise level.

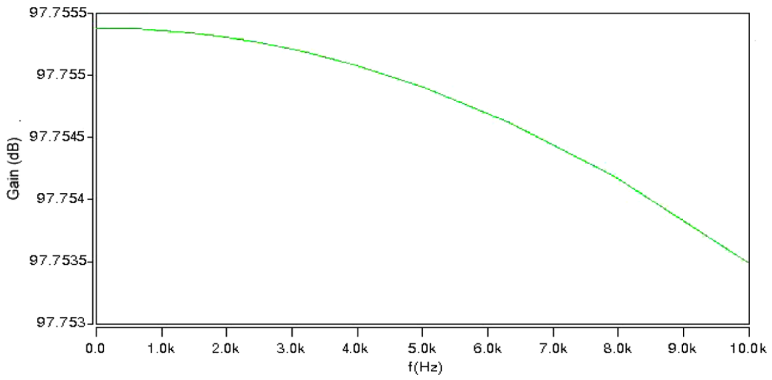
Figure 8 Proposed op-amp architecture



5 Simulation results

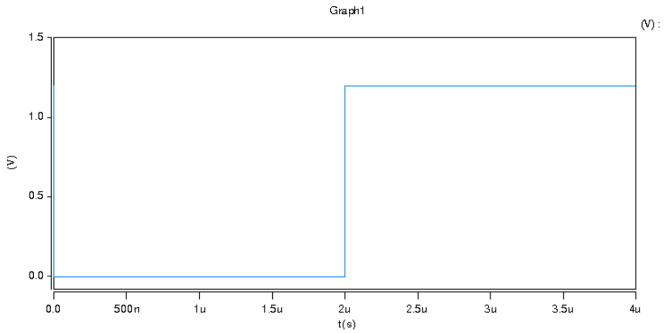
The op-amps architecture is implemented using HSPICE in Synopsis tool under 1.2 V supply with CMOS 0.13 µm technology. The open loop gain of the proposed op-amp is plotted in Figure 9.

Figure 9 Gain plot of the proposed op-amp (see online version for colours)



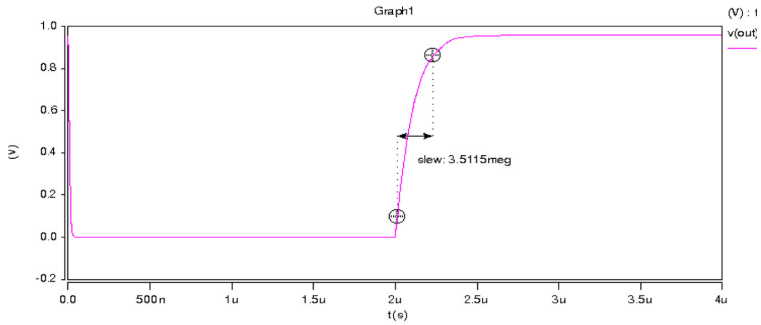
Settling time behaviour is performed for the proposed op-amp in Figure 8 with the voltage follower configuration. Figure 10(a) and (b) shows the settling time input and output of the proposed bio-medical op-amp.

Figure 10(a) Step input to the proposed op-amp (see online version for colours)



(a)

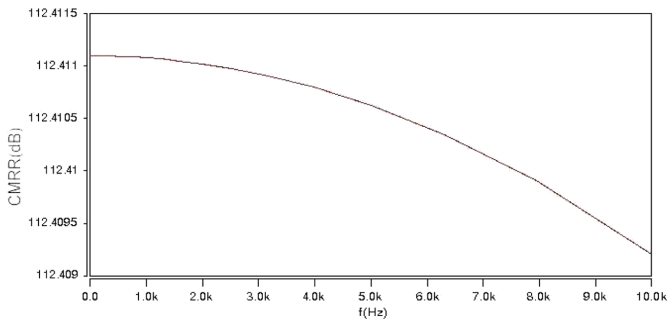
Figure 10(b) Settling time output of the proposed op-amp (see online version for colours)



(b)

AC analysis is performed for the proposed bio-medical op-amp with common mode configuration and Figure 11 shows the CMRR output of the proposed bio-medical op-amp.

Figure 11 CMRR of the proposed op-amp (see online version for colours)



Performance parameters of the existing op-amp with diode-connected transistors are compared against the proposed op-amp with current mirror circuits. The results are tabulated in Table 2. It is inferred from the table that the proposed bio-medical op-amp with cascode current mirror circuit excels in its performance compared with proposed op-amp with other current mirror circuits and existing op-amp structure. It achieves a gain of 97.7554 dB, low noise of about 2.155 nV/$\sqrt{Hz}$ at 200 kHz, CMRR of about 112.41 dB, Total Harmonic Distortion (THD) of about 75.354 dB and slew rate of about 3.5115 V/µS under 22 kΩ and 13.5 pF load.

Table 2 Comparison of existing and proposed architectures

Parameter	*Units*	*Existing op-amp*	*Proposed op-amp with simple current mirror*	*Proposed op-amp with wilson current mirror*	*Proposed op-amp with widlar current mirror*	*Proposed op-amp with cascode current mirror*
Open loop gain	dB	95	97.03	71.52	77.65	*97.75*
Unity gain frequency	MHz	9.74	9.53	9.82	9.65	*9.2*
Total harmonic distortion (input voltage- 1Vpp, Fre = 1Khz)	dB	–75.352	–75.352	–75.118	–75.35	*–75.354*
Input thermal noise (@ 200k)	nV/$\sqrt{Hz}$	4.84	2.92247	2.1016	2.7416	*2.155*
Slew Rate	V/µS	0.13	0.96045	0.16309	1.805	*3.5115*
Supply voltage	V	1.2	1.2	1.2	1.2	*1.2*
CMRR	dB	105	97.35	91.06	93.42	*112.41*
Power Dissipation	mW	0.719	0.722	0.719	0.759	*0.73*
Load conditions R_L	Ω	22k	22k	22k	22k	*22k*
C_L	F	13.5p	13.5p	13.5p	13.5p	*13.5p*

6 Conclusion

A 130 nm programmable CMOS operational amplifier with cascode current mirror has been proposed. The op-amp proposed consumes very less power, offers less noise and it amplifies the weak cortical input signals to a larger extent. Simulation results prove that the proposed op-amp shows an improvement in gain of about 2.755 dB, CMRR of about 7.41 dB, slew rate of about 3.3815 V/µS and reduction in noise of about 2.685 nV/$\sqrt{Hz}$ compared with

that of the existing op-amp. So, the proposed op-amp can be used as a preamplifier in bio-medical applications.

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