Single-stage fully recycling folded cascode OTA for switched-capacitor circuits

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A single-stage multi-path operational transconductance amplifier (OTA) is presented. The proposed amplifier uses the transconductance enhancing technique in an upgraded folded cascode (FC) amplifier. It significantly improves the DC gain, unity-gain bandwidth and slew rate compared with previous FC amplifiers with the same power consumption. Simulation results in 90 nm complementary metal-oxide semiconductor (CMOS) technology show that the proposed OTA achieves a 59.1 dB DC gain and a gain bandwidth of 650 MHz, which makes it suitable for fast-settling switched-capacitor circuits.

Introduction: The operational transconductance amplifier (OTA) is a basic building block used in many analogue and mixed-mode circuits such as analogue-to-digital (A/D) converters and switched-capacitor filters that require fast settling and precise amplifiers [1]. Recently, the folded cascode (FC) amplifier has gained preference over the telescopic owing to the low voltage nature of present and future CMOS technologies, despite the higher power budget [2]. Moreover, the pMOS input pair is preferred over the nMOS one because of its lower flicker noise, higher non-dominant pole and lower input common-mode voltage [3].

The conventional configurations of FC and recycling folded cascode (RFC) amplifiers are shown in Figs. 1*a* and *b*. Transistors M3 and M4 of the FC draw the most current and have the largest transconductance. Therefore the RFC amplifier utilises M3 and M4 as driving transistors and the input drivers M1 and M2 in Fig. 1*a* are divided into M1a-M2a and M1b-M2b as in Fig. 1*b*, which now conduct a current flow equal to $I/2$ [2]. These modifications lead to better transconductance and slew rate. However, to improve the power efficiency of the RFC amplifier, the double-RFC (DRFC) amplifier (shown in Fig. 2) has been presented in [4]. In this circuit, the differential input pair is now replaced by a triplet (M1a-M2a, M1b-M2b and M1c-M2c) and the current mirrors (M3c-M6c and M3d-M6d) are added as the double recycling structure to increase transconductance. Other techniques to enhance the performance of FC and RFC amplifiers such as the improved recycling structure [5] and multipath schemes [3, 6] can be also utilised.

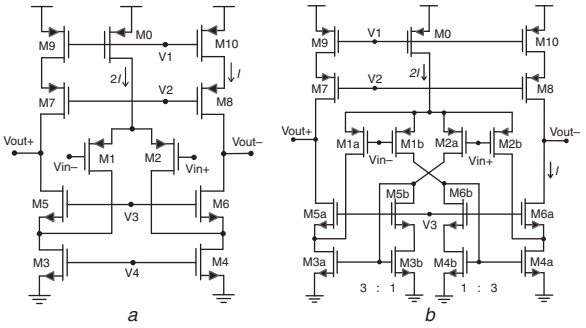

Fig. 1 *FC (Fig. 1a) and RFC (Fig. 1b) amplifiers*

A high-performance amplifier should have high GBW (for fast settling) and high DC gain (for an accurate final value) [1]. It is difficult to design an amplifier with both high gain and high bandwidth because of contradicting design requirements. Therefore the enhancing performance of OTAs is still an open challenge for designers. In this Letter, by using the current-shunt technique, a double recycling structure and additional drivers an enhanced multi-path FC amplifier is proposed. This structure significantly enhances the transconductance of a conventional OTA.

Proposed amplifier: Fig. 3 shows the proposed fully RFC (FRFC) amplifier. The input signal is amplified by the double recycling structure in node B. Thus, this amplified signal can be amplified again using additional drivers (M3e-M6e and M3f-M6f) to considerably enhance transconductane. Furthermore, the current-shunt technique (M7d-M10d) is utilised to increase the generated transconductance of pMOS drivers (M9 and M10) and transistors M9b and M10b are used to control the output common-mode voltage. The small signal transconductance of the FRFC amplifier is given by

$$\mathrm{Gm_{FRFC}} = \frac{(\mathrm{gm_{2c}gm_{4d}/gm_{4c}}) + \mathrm{gm_{1b}}}{\mathrm{gm_{4b}}}\left(\mathrm{gm_{4a}} + \mathrm{gm_{4f}} + \frac{\mathrm{gm_{4e}gm_{10}}}{\mathrm{gm_{10c}}}\right) + \mathrm{gm_{2a}} \quad (1)$$

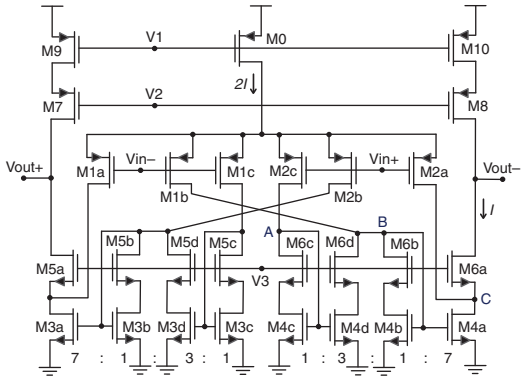

Fig. 2 *Double RFC amplifier*

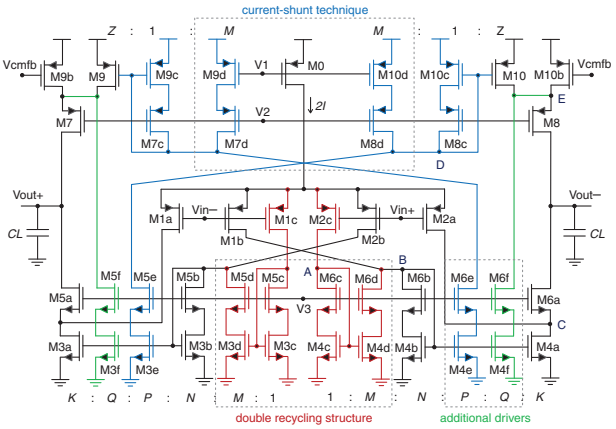

Fig. 3 *Proposed FRFC amplifier*

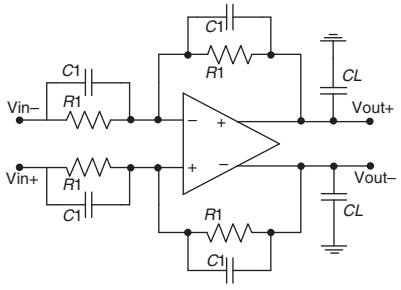

Fig. 4 *Unit gain buffer configuration*

It is assumed that all transistors have the same overdrive voltage and by replacing the current gain of transistors in (1), it can be seen that

$$\mathrm{Gm_{FRFC}} = \left[\frac{(2M+N)(K+Q+PZ)+N}{N}\right]\mathrm{gm_{2c}} \quad (2)$$

Note that $\mathrm{gm_{2c}}(2+M+N)_{\mathrm{FRFC}} = \mathrm{gm_{1,FC}}$

$$\mathrm{Gm_{FRFC}} = \left[\frac{(2M+N)(K+Q+PZ)+N}{N(2+N+M)}\right]\mathrm{gm_1} \quad (3)$$

The values of current gain factors M, N, P, Q, K and Z in (3) are chosen equal to 3, 1, 2, 1, 4 and 6, respectively. This selection maintains the power budget unchanged for both conventional and proposed amplifiers. Therefore the small signal transconductance of the FRFC is improved 20 times over the FC.

According to Fig. 3, the input signal passes from six nodes named A, B, C, D, E and the output. By associating one pole to each of these nodes, it is obvious that the proposed OTA has two new non-dominant

poles ω_D and ω_E compared with the DRFC amplifier. The non-dominant poles ω_B and ω_D of the FRFC are larger than the other poles that can be obtained by

$$\omega_B = -\frac{\mathrm{gm}_{4b}}{C_B} = -\frac{N}{(N+P+Q+K)C_{\mathrm{GS},4c}}\mathrm{gm}_{4c} \tag{4}$$

$$\omega_D = -\frac{\mathrm{gm}_{10c}}{C_D} = -\frac{P}{(M+1)(Z+1)C_{\mathrm{GS},10c}}\mathrm{gm}_{4c} \tag{5}$$

Therefore, enhancing the transconductance of the proposed OTA leads to larger non-dominant poles and phase margin degeneration.

Owing to the existence of transconductance enhancing techniques in the proposed amplifier, a large slew rate can be achieved. Assuming a large signal applied to Vin−, M1a, M1b and M1c will be turned off which forces M4b, M4e, M4f and M4a to turn off and M4d and M2a to go into the deep triode region. These occurrences lead M6a, M6f, M6e and M6b to turn off. On the other hand, the drain voltage of M6e rises, which forces M9 and M9c to turn off and the drain current of M9b flows into M3f. As a result, the tail current $2I$ flows into M2b and M2c and the drain current of M2b is mirrored by a factor of P, Q and K into M3e, M3f and M3a, respectively. Thus, the load capacitor at the positive output is discharged by M3a and the load capacitor at the negative output is charged by M10. Therefore it can be observed that

$$\mathrm{SR}^+ = \frac{Z.P}{(M+1)C_L}I_{D2b}, \quad \mathrm{SR}^- = \frac{K}{C_L}I_{D2b}, \quad I_{D2b} = \frac{2(M+N)}{M+N+1}I \tag{6}$$

where I_{D2b} is the drain current of M2b during slewing, and M, N and K are the current gain of transistors as defined in Fig. 3. Therefore the differential slew rate is given by

$$\mathrm{SR} = \frac{\mathrm{ZP}+K(M+1)}{M+1} \times \frac{2(M+N)}{M+N+1} \times \frac{I}{C_L} \tag{7}$$

By substituting the value of the current gains in (7), the SR of the FRFC is improved seven times over the FC for the same power consumption. In addition, during negative slewing a similar improvement in the value of slew rate is obtained.

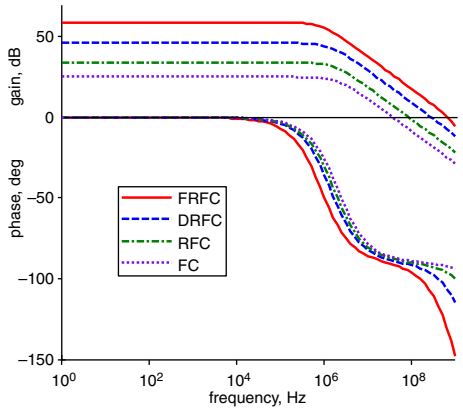

Fig. 5 *Frequency response of designed amplifiers*

Simulation results: The four amplifiers were simulated in 90 nm BSIM4v4 level 54 mixed-signal CMOS technology at a 1.2 V supply voltage by Hspice. To have the fastest response and reasonable stability in these designs, the channel length of all transistors was set to 90 nm (leads to a lower DC gain). As shown in Fig. 4, the FC, RFC, DRFC and FRFC were each used as a unity gain capacitive amplifier with a total capacitive load of 10 pF ($C1 = 1$ pF, $CL = 5$ pF and $R1 = 500$ kΩ). The frequency and transient response of the amplifiers are shown in Figs. 5 and 6, and Table 1 summarises the simulation results.

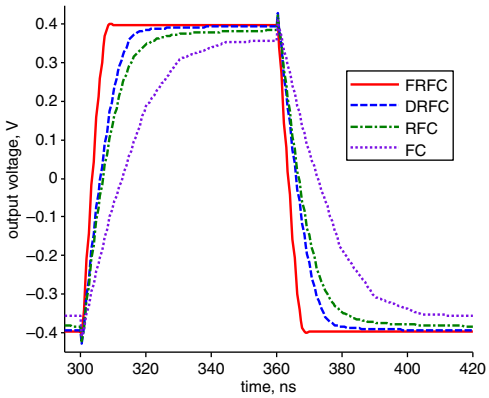

Fig. 6 *Transient response of designed amplifiers with differential 8.33 MHz, 0.8 $V_{p\text{-}p}$ input step*

Table 1: Summary of simulation results

Parameter	FC	RFC	DRFC	FRFC
Power supply (V)	1.2	1.2	1.2	1.2
Technology (nm)	90	90	90	90
Power dissipation (μW)	580	580	580	580
Capacitive load (pF)	2 × 5	2 × 5	2 × 5	2 × 5
Unity-gain bandwidth (MHz)	37.5	86.5	284.5	650
Phase margin (°)	90	88.5	82.9	50
Open loop DC gain (dB)	25.1	34.1	46.1	59.1
Average slew-rate (V/μs)	23.2	44.5	57.4	115.2
0.1% settling time (ns)	56.6	42.3	28.7	9.6
Input voltage noise at 100 kHz (nV/√Hz)	60.7	44.1	41.5	42.7
FOM (dB.MHz.(V/μs)/μW)	37.6	226.3	1298	7630

Note that in Table 1 all of the amplifiers have the same power consumption. It can be seen that the proposed amplifier has a better DC gain, unity gain bandwidth, slew rate and settling performance compared with the conventional amplifiers. Since the proposed amplifier has more non-dominant poles, the phase margin is degraded. Nevertheless, for the proposed amplifier, a better FOM has been achieved.

Conclusion: By using the transconductance enhancing technique, a fully RFC OTA with added current-shunt structures is presented. The amplifiers were designed with the same power consumption and simulation results show a DC gain enhancement of 34 dB as well as 612.5 MHz improvement in gain bandwidth compared with the conventional FC structure, without adversely affecting the input referred noise.

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One or more of the Figures in this Letter are available in colour online.

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