Multi-Frequency Class-D Inverter for Rectifier Characterisation in High Frequency Inductive Power Transfer Systems

George Kkelis, David C. Yates, Paul D. Mitcheson

Electrical & Electronic Engineering Department, Imperial College London, UK (g.kkelis13@imperial.ac.uk)

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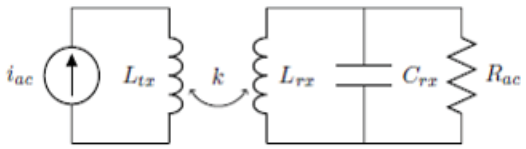
Abstract

This paper presents the development and utilisation of a voltage source multi-frequency Class-D inverter in a cost-effective test rig for rectifiers in 6.78 MHz to 13.56 MHz inductive power transfer (IPT) systems without the need of the magnetic link. Apart from the inverter, the rig compromises a tuned receiving (Rx) coil of the IPT system and a rectifier under test. With the inverter emulating a magnetically induced voltage in an Rx coil, rectifiers experience IPT conditions while they are isolated from the rest of the system. Therefore, they are accurately analysed with commercially available instruments, without affecting other parts of the IPT system. The Class-D inverter was implemented with Si MOSFETs and is capable of delivering power greater than 200 W with efficiencies higher than 80 %.

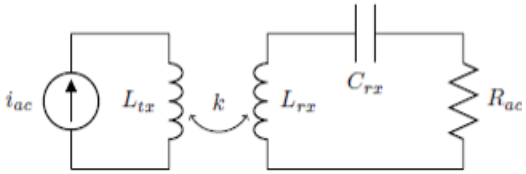
1 Introduction

From IPT theory it is well known that maximal link efficiency between a transmitting coil (L_{Tx}) and a receiving coil (L_{Rx}) is achieved when the L_{Rx} is tuned with a capacitor (C_{Rx}) at the frequency of operation and it is loaded with a certain ac resistance value (R_{ac}), Fig. 1a and Fig. 1b. This value is defined by the impedance of C_{Rx}, the unloaded quality factors of the coils forming the link, the magnetic coupling between them (k) and the tuning method of the receiving coil, series or parallel, [1]. In an IPT system R_{ac} is represented by the input resistance of the rectifier. Therefore, in order for a rectifier to be integrated to an IPT, it must be compatible with the output type of the tuned receiving coil, voltage output for parallel tuning (Fig. 1a) and current output for series tuning (Fig. 1b) [1], and be designed to present the required resistance for maximal link efficiency.

Measuring the efficiency and input resistance of a rectifier while integrated to an IPT system of operating frequency in the range of 6.78 MHz to 13.56 MHz is not a trivial task. In the multi-MHz region the intrinsic capacitance of a high frequency voltage probe becomes a non-negligible part of the circuit under test. Therefore, instrumentation of the voltage at the input terminals of the rectifier could detune the receiving resonant tank degrading the efficiency of the whole system and leading to wrong experimental conclusions. Also, due to resonance and the high operating frequency, the voltage across the receiving tank could be in orders of kV even for moderate power transfers (e.g. 100 W). Hence the limit of a high voltage probe might be exceeded because of frequency de-rating. To overcome those challenges and accurately characterise rectifiers for IPT systems, a test rig was developed.



(a) Parallel tuned receiving coil.



(b) Series tuned receiving coil.

Figure 1: Inductively coupled coils.

The rig (Fig. 2) consists of a voltage source inverter, a coil tuned by a capacitor at the frequency of operation and the rectifier under test. The resonant tank and the rectifier form the receiving end of an IPT system. The inverter generates a square wave voltage, which simulates voltage induction in a coil from the presence of an alternating magnetic field. Due to the high quality factor of the resonant tank (as required for maximal IPT link efficiency) all the harmonics of the square wave except the first are filtered and a sinusoidal current is drawn from the inverter (Class-D operation) creating an alternating (ac) power source for the rectifier.

Referring to Fig. 2, the average of the product of v_{in} and i_{in} over one period provides a measurement for the input power at the receiving end. Using the output power from the output terminals of the rectifier, the efficiency of the receiving end is calculated. Furthermore, using the rms of i_{in} and the input power the input resistance of the rectifier can also be calculated.

Although the voltage source Class-D inverter was not reported as the most efficient circuit for high frequency (HF) operation (3 to 30 MHz), it has properties that make it the most suitable topology for test rig utilisation. The Class-E inverter developed in [2] has been a more efficient inverter for operating in the HF range and beyond. Class-E inverters make use of a *LCC* network to eliminate turn-on losses and keep turn-off losses to a minimum. The evaluation however

of the *LCC* network is extremely sensitive on the value of the load resistor and the frequency of operation. Therefore, while a Class-E inverter would be the most efficient solution for the test rig, its operation would be successful only for a particular rectifier design. Class-D inverters on the other hand have an operation independent of the ac resistive load and they have the highest maximum power output capability amongst all switched mode inverters [3]. The transistor's voltage equals to the dc bus voltage (V_{in} in Fig. 2) which results in voltage stress well below *kV* for power throughputs lower than a *kW*. Therefore, the voltage output of the inverter could be successfully monitored with a high frequency high voltage probe [4].

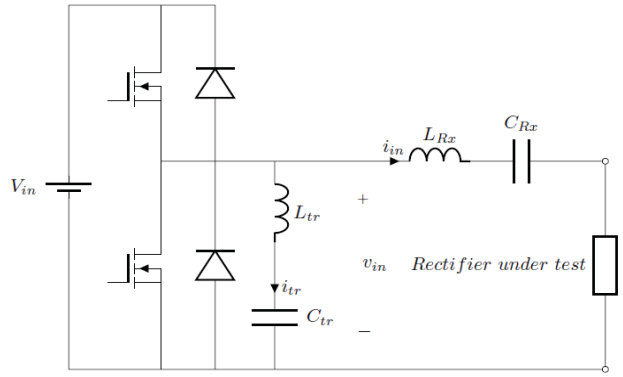


Figure 2: Circuit diagram of developed test rig.

2 Implementation of Class-D Inverter

2.1 Half-Bridge

Rectifiers will be characterised for integration into weakly coupled IPT systems (k<5 %), like the one presented in [5]-[7]. In such low coupling factors, maximum link efficiency is achieved when the series R_{ac} (Fig. 1b) is below 20 Ω. With coil equivalent ac resistances below 0.5 Ω, the minimum optimal R_{ac} would be around 5 Ω when k is below 2 %. For the first version of the test rig the power throughput was set up to 200W.

From the specifications, low voltage high current capability transistors had to be used in the inverter. The DE Si MOSFET series from IXYS were reported as good candidates for delivering RF power with the appropriate cooling [8,9]. The models DE275-201N25A (200 V, 25 A) and DE150-201N09A (200 V, 9 A) met the specifications. Due to the unavailability of the latter model the DE275-201N25A was selected.

The board layout of the bridge side followed a similar design to the one presented in [9] for keeping trace inductance and resistance to a minimum. The only difference was that space was carefully allocated for a BNC jack at which a probe was placed, through a BNC adaptor, for monitoring the output voltage of the bridge. This probing technique introduces the least ground lead inductance.

The output of the bridge is connected to the resonant tank and the rectifier (both implemented on the same board) via an RF SMA connector. In several application notes similar RF connectors have been used to transfer much higher levels of power [8]-[10].

2.2 AC Bypassing Circuit

The voltage driven Class-D inverter draws a high frequency current from its dc voltage source during the conduction of the high side transistor. Therefore, a high frequency bypass circuit had to be introduced between the power supply unit (V_{in} in Fig. 2) and the inverter.

The bypass circuit (Fig. 3) is composed from two capacitors (C_{byp1} and C_{byp2}) and a filter inductor (L_f). L_f has effectively infinite impedance at the frequency of operation and therefore allows only dc current to flow through it. C_{byp1} filters any noise at the input terminals of the power supply unit. The capacitor at the dc input terminals of the inverter (C_{byp2}) conducts the same current as the high side MOSFET. Hence it must have high quality factor at the frequency of operation and be large enough to function as a filter and not as part of the circuit. Any inductance in the path of the bypass capacitor will result in parasitic oscillations at the output waveform of the inverter. Thus, the bypass capacitor was placed as close as possible to across the dc terminals of the half-bridge.

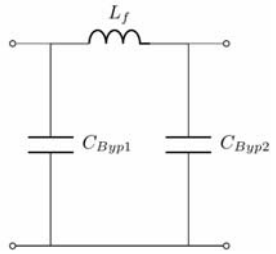


Figure 3: Bypassing circuit for ac current.

The filter inductor was implemented using a toroid ferrite core and both bypass capacitors were implemented with multi-layer ceramic capacitor banks.

2.3 Gate Drive Circuits

In order to gain multi-frequency capability standard Class-D square wave gate drivers were chosen for driving the transistors of the inverter. Apart from the required low inductance path between gate driver and MOSFET, in such operating frequencies negative bias is also essential to avoid parasitic turning on of a MOSFET from the discharge of its Miller capacitance (C_{GD}) [10]. The level of negative bias should not exceed a value where the MOSFET is overdriven, otherwise parasitic oscillations will occur at the output voltage.

The selected MOSFETs have an input capacitance (C_{iss}) near 4 nF at 0 V drain to source potential (V_{DS}). C_{iss} settles to 2.5 nF as V_{DS} increases from 20 V to 200 V. Those values result

to a required power of 2.712 W and 5.424 W for charging and discharging both C_{iss} from 0 V to 10 V at 6.78 MHz and 13.56MHz respectively. IXYS gate drivers IXRFD630 and IXRFD631 were found capable of operating in such speeds and power throughputs [9]. IXRFD630 was utilised in the test rig. Its power consumption for the required performances is approximately 7 W and 14 W for 6.78 MHz and 13.56 MHz respectively.

Both high and low side gate drive circuits were designed based on the isolated gate drive developed in [12] for SiC MOSFETs and based on the recommendations of [13] for achieving the best possible performance of IXRFD630. The circuit diagram is shown in Fig. 4.

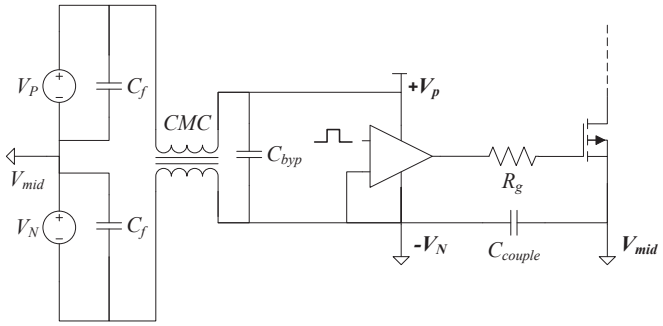


Figure 4: Gate drive circuit.

Two isolated dc to dc converters (represented by V_P and V_N in Fig. 4) had their outputs connected in series providing the positive and negative bias gate voltages when the point of their connection (V_{mid}) was tied to the source of the driven MOSFET. To test the performance of the rig under different positive and negative gate voltage levels, the two isolated outputs of an Agilent bench power supply (one power supply per gate drive circuit) were used for providing the two levels. This technique was adapted from [10].

The same type of ac bypassing as the one used between the half-bridge and the power supply had to be added across the output of each isolated converter, to bypass the ac component of the current of the gate driver. Furthermore, the filter inductors of the two bypass circuits were coupled together in a common-mode configuration (*CMC* in Fig. 4) to suppress any common mode noise across the supply terminals of IXRFD630. An extra bypass capacitor (C_{couple} in Fig. 4) was added between the ground terminal of IXRFD630 and the source terminal of the driven MOSFET, to provide a low inductance ac coupling between the two terminals.

Optical-isolators where preferred from magneto-isolators for providing the switching signal to the gate driver due to their tolerance to electromagnetic interference (EMI). Previous versions of the gate drive circuits failed due to the inability of the magneto-isolators to operate under relatively high EMI. A low power isolated dc to dc converter was used to power the output side of the optical-isolator. As with every dc supply terminal, an ac bypass circuit was added between the converter and the power terminals of the isolator.

2.4 LC Network for Minimising Switching Losses

Switching losses are always present in the Class-D inverter as the square wave voltage across the blocking transistor charges its output capacitance (C_{oss}), which then discharges through the on-resistance ($r_{DS,ON}$) of the transistor when it is turned on [14]. However, when the load is inductive, the output sinusoidal current lags the output square voltage. At the instance of switching the current through the blocking MOSFET will flow through its intrinsic diode and C_{oss} will not be discharged through the $r_{DS,ON}$ but energy will be freewheeled back to the dc power supply through the internal body diode of the MOSFET to be turned off. Therefore, turn-on losses are eliminated [14] and turn-off losses are then dependent on the amplitude of the current through the transistor at turn-off and its turn-off delay.

To ensure an inductive load at the output of the inverter, an *LC* network was introduced across the low side MOSFET (L_{tr} and C_{tr} in Fig. 2). This technique was adapted from [15]. The resonant frequency of the network must be orders of magnitude lower than the operating frequency in order for the network to appear inductive. Therefore, the capacitor of the network (C_{tr}) has to function only as a dc blocking capacitor. The square wave voltage across the *LC* network causes the waveform of the current through it to have a triangular shape (i_{tr}). The sum of the sinusoidal current through the resonant tank and the triangular *LC* network current ($i_{in} + i_{tr}$) results in the current drawn from the inverter to lag the output voltage. The current through the MOSFET at turn-off has amplitude equal to the peak current through the *LC* network.

In most transistors the intrinsic body diodes are lossy and the addition of external antiparallel diodes in a bridge configuration is always recommended by manufacturers. SiC Schottky diodes where used in the implementation of the inverter, due to their minimum reverse recovery effect and their fast switching capability. The CSD01060A (600 V, 1 A) model from Wolfspeed was selected.

The inductor (L_{tr}) in the *LC* network was realised with iron powder toroid core suitable for RF power applications. Its inductance was set to 800 nH to result in impedances approximately of 5j Ω at 6.78 MHz and 10j Ω at 13.56 MHz; values within the average of the range of input resistances expected to be reflected from rectifiers developed for IPT systems like [6,7]. The capacitor C_{tr} was realised with a bank of several ceramic capacitors connected in parallel. The total capacitance was 2 μF which resulted in the resonant frequency of the *LC* network to equal 790 kHz.

3 Test Rig Performance

3.1 No Load Test

The performance of the bridge was initially tested without the resonant tank and the rectifier. The gate drive voltage levels were set to 6 V and -4 V for positive and negative biasing respectively. These biasing levels will result in the pre-mentioned power consumption from IXRFD630 and will provide a saturation drain current of 25 A [16] for the conducting transistor. Due to propagation and switching delays of both gate drive and MOSFET, the duty cycle of the control signals was set to 30 % and their phase difference at 180°. The resultant low and high side gate drive waveforms at zero dc link voltage (V_{in} in Fig. 2) are shown in Fig. 5. Furthermore, the output voltage of the inverter at no load, with amplitude 125 V, at 6.78 MHz and 13.56 MHz, is presented in Fig. 6.

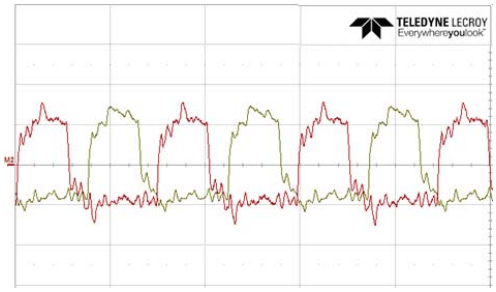
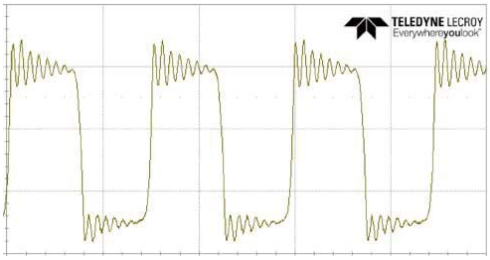
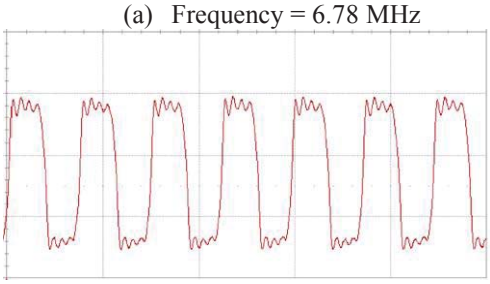


Figure 5: Waveforms across low and high side gate to source terminals (5 V/div, 100-ns/div).



(a) Frequency = 6.78 MHz



(b) Frequency = 13.56 MHz

Figure 6: Inverter output voltage at no load (50 V/div, 100-ns/div).

Due to the presence of the *LC* network across the low side transistor, the inverter conducts a triangular current waveform and so it dissipates power due to conduction and turn-off losses. To investigate whether the losses were also a result from cross conduction between the two MOSFETs, v_{GS} of both high and low side transistors was monitored while the bridge was outputting a 100 V square wave at 6.78 MHz. The observed waveforms are presented in Fig. 7.

In Fig. 7, when the dc link voltage (V_{in} in Fig. 2) is not zero both gate waveforms experience higher oscillations than the zero dc link voltage operation. However, even with the oscillations, due to sufficient negative bias, there is no point in time where both waveforms are above the threshold gate voltage. Note that the measured noise in the waveform of the high side v_{GS} is higher than the respective low side waveform because a differential probe was utilised which has longer leads than the passive probe used for monitoring the low side waveform.

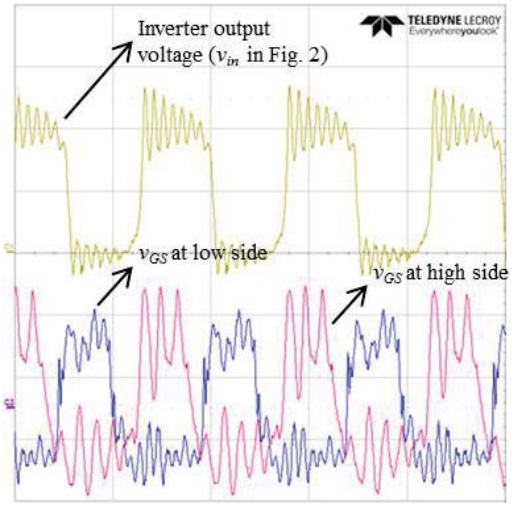


Figure 7: Low and high side V_{GS} while dc bus equals 100 V (V_{GS}: blue and red for low and high side respectively, 5 V/div; V_{DS}=V_{OUT}: yellow, 50 V/div, 100-ns/div).

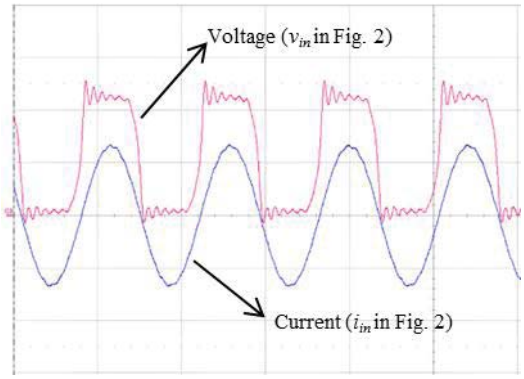
3.2 Performance During Rectifier Characterisation

After the correct open load operation the test rig was used in the characterisation of several rectifier topologies. The first experimental results were presented in [5]. For describing the performance of the inverter, the results from the characterisation of a half-wave current driven Class-D rectifier will be used.

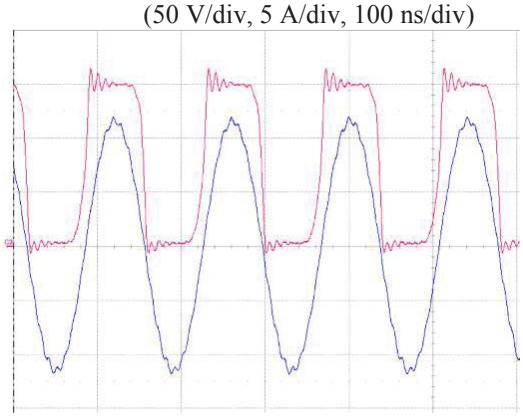
For measuring the current through the resonant tank a passive current monitor was used. The passive monitor, as reported by its manufacturers, is not affected by the presence of magnetic field, which is generated by the *Rx* coil, and therefore can provide accurate current measurements of up to 10 A peak at 13.56 MHz. Furthermore, due to its linear response with frequency its effect on the resonant tank can be easily calculated.

Fig. 8 presents the voltage and current waveforms at the input of the resonant tank during 150 W power delivered at the dc terminals of the rectifier.

It can be noted that the rise and fall times of the square wave are slightly higher when the current drawn is sinusoidal. This is an effect of the output capacitance (C_{oss}) of the MOSFET and the pn-junction capacitance (C_{pn}) of the anti-parallel diode. At this frequency range their impedances are actually in the same order as the impedance of the coil and its tuning capacitor. Because the current drawn from the inverter is sinusoidal it requires more time to charge and discharge C_{oss} and C_{pn} and therefore the output waveform has smoother rise and falling edges than it would if a square wave current was drawn.



(a) Rectifier Input Resistance = 10 Ω
(50 V/div, 5 A/div, 100 ns/div)



(b) Rectifier Input Resistance = 20 Ω
(50 V/div, 2 A/div, 100 ns/div)

Figure 8: Inverter output voltage (red) and current (blue) when testing a rectifier at 7 MHz and 150 W output dc power.

Since the input power has to be measured from alternating waveforms, the phase between the voltage and current waveforms is important. As maximal link efficiency occurs when the voltage induced in the *Rx* coil is loaded with a pure resistance, the input voltage and current to the resonant circuit (v_{in} and i_{in} on Fig. 2) should be in phase. The delay introduced by the current monitor has to be taken into account and therefore the deskew time of the current waveform should be evaluated accordingly. The accuracy of the input power measurement increases by increasing the measured samples.

The efficiency of the inverter was calculated during the characterisation of the Class-D rectifier. In the efficiency expression gate driver losses were taken into account. Two sets of experiments took place to test the impact of gate drive voltages on inverter performance. In the first set, v_{GS} was varying from 7 V to -4 V and in the second from -3 V to 5 V. In each set, the efficiency of the inverter was calculated when the rectifier was presenting a load of 10 Ω and 20 Ω. The results are illustrated in Fig. 9.

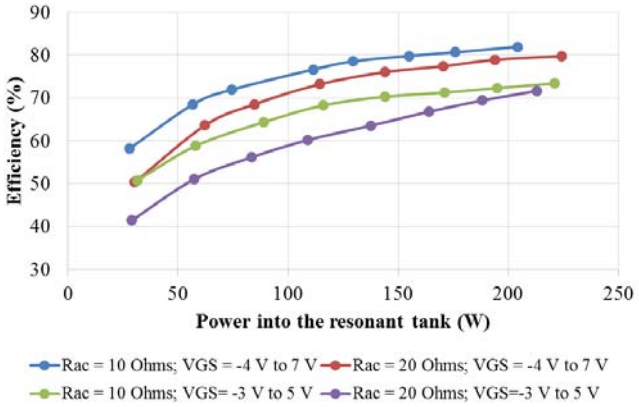


Figure 9: Inverter efficiency taking into account gate driver losses.

A peak efficiency of 81 % was reached when the output power from the inverter was approximately 200 W and v_{GS} had positive and negative bias levels equal to 7 V and -4 V respectively. The conduction losses were the main source of losses and hence, the higher biasing voltage range had the best performance. The gate drive losses were consuming at least 10 % of the losses.

Due to negative bias the IXRFD630 consumes power for a 11V potential while biasing the MOSFET at 7 V. Ideally, a gate drive transformer based circuit would have been a better solution, as the one presented in [9] as it provides sufficient negative and positive biasing. However, the frequency agility of the rig would have been limited.

The two following figures are images of the implemented inverter board (Fig. 10) and the test rig (Fig. 11).

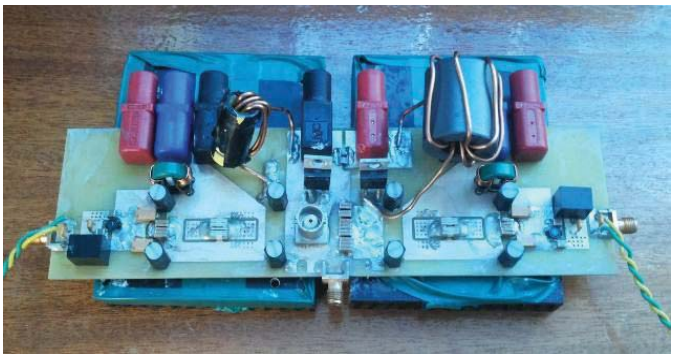


Figure 10: Image of the inverter.

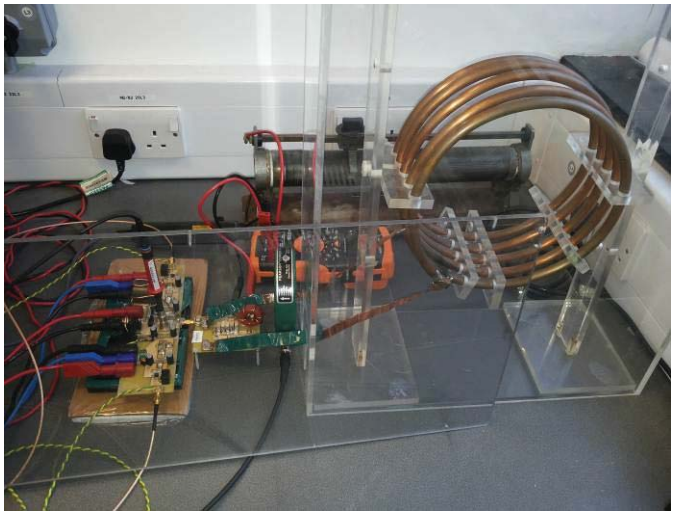


Figure 9: Image of rectifier test rig.

4 Conclusion

A voltage source Class-D inverter was exploited for the first time in a test rig for IPT rectifier characterisation independent of the magnetic link. The developed test rig makes the measurement of ac power feasible with commercially available passive voltage and current probes, while providing IPT conditions for the circuits under test. With square wave gate drivers the inverter has a multi-frequency ability and it's capable of outputting voltage waveforms within the range of 6.78 MHz to 13.56 MHz. Negative bias was essential for eliminating parasitic turn-on from the high dv/dt rates. Techniques have been adapted that eliminated the turn-on losses usually observed in Class-D topologies. The implemented inverter was capable of delivering power levels greater than 200 W at the tested rectifiers with peak efficiency greater than 80 %. The gate drive losses occupied 10 % of the total losses, which were dominated by conduction losses. A potential boost in the efficiency of the inverter could come from the replacement of the Si MOSFETs with GaN transistors.

Acknowledgements

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