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Low-Noise Isolated Digital Shunt for Precision Class-D Power Amplifiers

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***Abstract*—Power electronic converters regularly employ isolated analog to digital converters (ADCs) for the acquisition of voltage/current signals that are required for their digital control systems. In precision power converters, such as, e.g., those required in nanometer-accuracy positioning systems for integrated circuit manufacturing, the noise content of the measured signals is critical since it leads to undesired noise in the power converter output signals due to the feedback system's high sensor noise sensitivity. This paper illustrates how sampling jitter, i.e., stochastic deviations of the ADC's sampling instants from their ideal occurrences, which is mainly caused by the digital signal isolators used to isolate the ADC control signals, introduces a measurement error and critically influences the signal to noise ratio (SNR) of an isolated current measurement at the output of a half-bridge. Jitter figures of commonly used digital signal isolators are measured, as these values are rarely available in literature. It is revealed that RMS jitter varies significantly between the analyzed devices, from 13 ps up to 250 ps, even among those that utilize similar isolation techniques. Thus, in a second step, it is analytically derived how the half-bridge inductor, and the related half-bridge current ripple, directly influence the SNR of the current measurement. Using the resulting simple design equations, which are also verified with numeric simulations, the half-bridge inductor can be designed to significantly reduce the half-bridge current measurement noise, by a factor of up to ≈0.6 in common measurement configurations.**

***Index Terms*—ADC Sampling Jitter, Half-Bridge Inductor, High-Side, Isolated Current Sensing, Signal to Noise Ratio (SNR)**

I. Introduction

Digital control systems for power electronic converters offer, as compared to their analog counterparts, more flexibility since they can be easily adapted and scaled to fit similar systems, which lowers development time and cost. As the control laws are implemented in digital circuits or software, the quantities to be controlled, e.g., converter output voltages or currents, need to be digitized [1]. This is commonly achieved using integrated analog to digital converters (ADCs), which are available in a wide range of resolutions, accuracies and conversion rates. As a key part of a closed-loop feedback system, the signal acquisition and digitization circuits must provide low-noise signals, as their noise is directly injected into the feedback system which cannot separate the undesired noise components from the actual desired signal, i.e., the control output is equally sensitive to the reference signal as it is sensitive to the sensor's noise [2].

Power converters providing ultra-low-noise output voltages or currents, which are employed in industrial applications like magnetic resonance tomography, magnetically levitated actuators or precision mechatronic positioning systems, provide power waveforms with signal to noise ratios (SNRs) in excess of 100 dB [3], [4]. Consequently, sources of noise must be carefully analyzed and accounted for, including the ADC systems [5]. Usually, the ADC and its front-end circuitry (e.g., amplifiers, filters and/or signal buffers) can be designed such that the digitized output signal contains sufficiently low noise for the intended application. **Fig. 1** illustrates a circuit configuration performing a galvanically isolated current measurement in a half-bridge switching arrangement, a typical power electronics topology. The shunt resistor R_S offers low noise and a high linearity compared to other integrated, isolated current sensors [6], [7]. Compared to a low-side shunt placement, which would obviate the isolated sensing circuitry, the illustrated setup allows the quick detection of faulty output currents at all times [7], [8]. The analysis performed in this work is based on the half-bridge topology in the application of a full-bridge Class-D amplifier, and can thus easily be applied in an identical fashion to other topologies comprising half-bridge switching arrangements [5], [9].

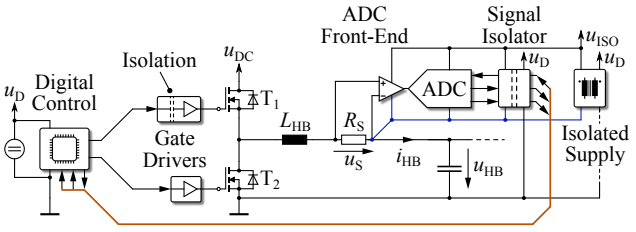

Fig. 1. Typical setup of a digitally controlled half-bridge switching stage employing a shunt resistor and an isolated ADC circuit in order to measure the half-bridge output current i_{HB} with low noise and distortion.

Placing the ADC on the isolated potential offers the benefit that only its digital signals need to cross the isolation barrier, which is easily achievable without corrupting their integrity by using digital signal isolators. However, the ADC control signal that starts the signal acquisition is also transmitted through the signal isolator, which can add significant amounts of jitter to it that expresses itself as a time-dependent and stochastically varying signal propagation delay of the isolator device [10]. It is well-known that this jitter, even if it is in the picosecond range, severely limits the ADC's SNR, as it introduces wide-band noise to the sampled signal [11]. This source of half-bridge current measurement noise is relevant for low-noise

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applications and has been discovered as a deteriorating effect in earlier work, but not described in detail [12].

Thus, this work first compares the jitter figures of different types of integrated signal isolation circuits. It shows that the amount of jitter varies significantly, not only between, but also within different isolator technologies, which renders their selection process more difficult. In a next step, it is demonstrated that the half-bridge current measurement noise is directly related to the slope of the half-bridge current ripple. Following this result, simple design equations for the half-bridge inductor are derived such that the SNR of the half-bridge output current can be improved.

II. Signal Isolator Jitter

In a first step, different commonly used signal isolators for power electronic applications, with isolation ratings up to $5\,\mathrm{kV_{RMS}}$, are compared experimentally with respect to their jitter performance, as such data is scarcely provided by manufacturers. The output jitter of the isolators is measured by generating a low-jitter square waveform with a fixed period using a signal generator (*Tektronix AFG3102*), and feeding it to the input of the considered signal isolator (with the appropriate signal level), whose supply is sufficiently bypassed and filtered. **Fig. 2** illustrates the circuit configuration. At the

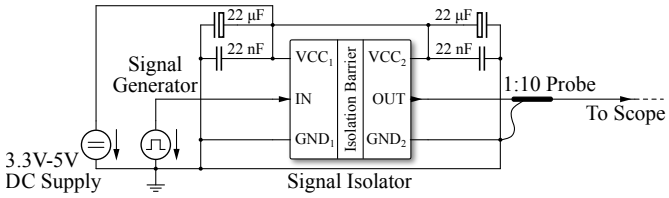

Fig. 2. Circuit configuration for the signal isolator jitter measurement. All components and the oscilloscope probe are directly placed at the device package. The signal generator is internally terminated with $50\,\Omega$. When possible, $3.3\,\mathrm{V}$ is used as supply voltage.

isolator output, the durations of randomly sampled periods are obtained with an oscilloscope (*Rohde&Schwarz RTO1014*), and the RMS jitter of the output signal is approximated based on the standard deviation of the measured durations [10], [13], [14]. More than 5000 period durations are recorded for each measurement in order to reliably record the standard deviation. For all measurements, the input square waveform has a frequency of $200\,\mathrm{kHz}$, which is a value close to regularly used sampling or switching frequencies in power electronic applications. The waveform generator's inherent RMS jitter is $7.3\,\mathrm{ps}$ and the oscilloscope's jitter contribution is below $5\,\mathrm{ps}$ [15], which, by considering these (uncorrelated) standard deviations, results in a lower measurement boundary of $\sqrt{5^2\mathrm{ps} + 7.3^2\mathrm{ps}} = 8.8\,\mathrm{ps}$ for the presented RMS jitter measurement method.

Fig. 3 illustrates the measurement results for the analyzed signal isolators which feature different signal propagation times and a wide range of common-mode transient immunities (CMTI), which indicates how fast the voltage across the device's isolation barrier may change without producing erroneous output signals. Note that the propagation times and CMTI values are obtained from datasheets. Isolators based on

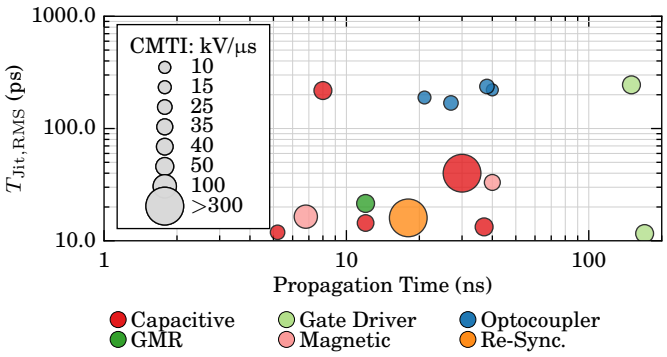

Fig. 3. RMS jitter of different types of digital signal isolators. CMTI: Common-mode transient immunity. GMR: Giant magnetoresistive effect. Re-Sync: Additional circuitry is used to re-synchronize the jittery signal from any isolator to a low-jitter clock signal [10]. Note that the (high-side) gate drivers do not provide a galvanically isolated interface, as they use a high-impedance signal path to the high-voltage potential. The lower jitter measurement limit is $\approx$8.8 ps.

a capacitive isolation method often modulate the input signal to increase its frequency and then transmit it via capacitive coupling across a dielectric to the isolated side, where it is demodulated and output [16]. Magnetic isolators use a similar approach, but the signal is inductively coupled to the isolated output [17]. Another method of magnetic coupling is based on the giant magnetoresistive effect (GMR) [18]. For the sake of completeness, high-side gate drivers are also investigated, even though they do not provide a galvanic isolation as they transfer the signal through a high-impedance path [19]. Finally, the analysis also includes a circuit proposed in [10], which allows the utilization of any signal isolator, as the jitter is eliminated to values below $15\,\mathrm{ps}$ by re-synchronizing the (jittery) isolator's output signal to an isolated, low-jitter clock signal. As an additional benefit, the signal isolation is rendered immune to very fast common-mode transients, exceeding $300\,\mathrm{kV\,\mu s^{-1}}$.

The measurements indicate that different isolators, providing a wide range of propagation times and CMTIs, can also show a wide spread of jitter values, even when utilizing a similar isolation technology. This renders the selection process for a low-jitter signal isolator, required for the transmission of the conversion control signals for ADCs, more difficult.

In the following, the implications of ADC sampling jitter on the SNR and the design of a synchronously sampling half-bridge current sensor are presented.

III. Low-Noise Half-Bridge Current Measurement

In order to evaluate the impact on the half-bridge output current measurement SNR due to the ADC sampling jitter, the circuit configuration of **Fig. 1** is considered in a single-phase DC/AC converter. **Fig. 4** illustrates the related waveforms. It is assumed that the time-average of i_{HB} over a switching period T_{PWM}, denoted as $\langle i_{\mathrm{HB}} \rangle$, and u_{HB}, are both sinusoidal (with fundamental frequency $f_{\mathrm{F}} = 1/T_{\mathrm{F}}$) and in phase to each other, which is valid for resistive loads and small half-bridge output filter capacitances C_{HB}. In the following analysis, the load is resistive (R_{L}) and connected to a second,

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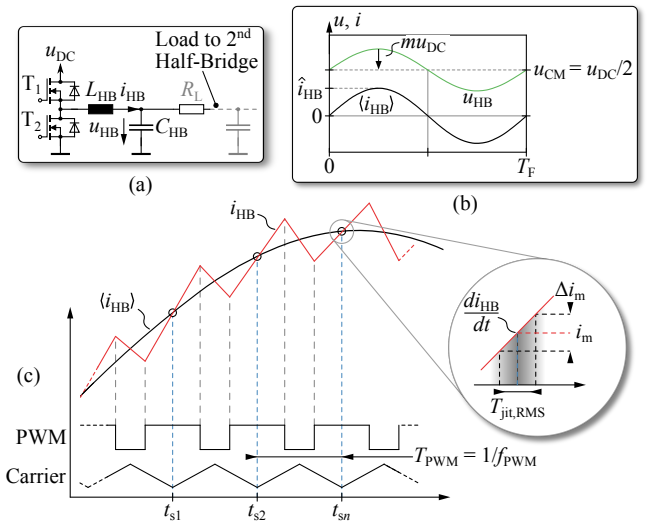

Fig. 4. Half-bridge current waveform subject to ripple. The current-sensing ADC samples once per PWM period at sampling instants t_{sn}. Due to jitter, t_{sn} is varied stochastically around its ideal time instant. The current slope at t_{sn} defines the current measurement error Δi_m that reduces the SNR of the current measurement.

identical half-bridge. This is a full-bridge Class-D amplifier topology with a bridge-tied load, cf. **Fig. 4** (a). Note that the following analysis is independent of the load configuration, it can be performed equally with any type of load (e.g., inductive-resistive) and other load connections (e.g., to a DC-link mid-point instead of to the output of a second half-bridge). For the considered bridge-tied load, in order to be able to provide a load current of both polarities, a constant common-mode voltage $u_{CM} = u_{DC}/2$ is added to the half-bridge output voltages. **Fig. 4** (b) illustrates the resulting waveforms for one fundamental period. The duty-cycle of the half-bridge's PWM gate control signal, which is the relative turn-on time of the high-side transistor T_1 during a PWM switching period T_{PWM}, is thus given as $d(t) = 1/2 + m(t)$, with the modulation index $m(t) = \hat{m}\sin(2\pi f_F t)$. Neglecting switching-frequency ripple components and the voltage drop at L_{HB}, this results in:

$$u_{HB}(t) = u_{DC}\left(1/2 + \hat{m}\sin(2\pi f_F t)\right) \quad (1)$$

$$\langle i_{HB} \rangle(t) = \hat{i}_{HB}\sin(2\pi f_F t), \quad (2)$$

During the turn-on time of T_1, the slope of the half-bridge output current is then given as:

$$\frac{di_{HB}(t)}{dt} = \frac{u_{DC} - u_{HB}(t)}{L_{HB}} = \frac{u_{DC}\left[1 - 2\hat{m}\sin(2\pi f_F t)\right]}{2L_{HB}}. \quad (3)$$

As illustrated in **Fig. 4** (c), the ADC is sampling when the PWM carrier reaches its bottom value, at time instants t_{sn}. This ensures that no half-bridge switching action takes place during the signal acquisition, which, due to the fast voltage transients occurring at the switch-node, could introduce spurious error voltages to the measurement. The jitter of the sampling signal moves the sampling instants away from the ideal instant, which would result in the current measurement i_m, as illustrated in the enlarged portion of **Fig. 4** (c). Consequently, the resulting measurement error Δi_m depends on the current slope di_{HB}/dt and is, due to the stochastic nature of the jitter, also behaving like noise and hence reduces the SNR of the current measurement. The jitter-induced current error can thus be given as:

$$\Delta i_m(t) = \frac{di_{HB}(t)}{dt} T_{jit,RMS}. \quad (4)$$

In order to calculate the SNR of the current measurement, the RMS value of the current error is determined over the fundamental period T_F [11]:

$$\Delta i_{m,RMS} = \sqrt{\frac{1}{T_F}\int_0^{T_F} \Delta i_m^2(t)dt} = \frac{T_{jit,RMS}\, u_{DC}\sqrt{2\hat{m}^2 + 1}}{2L_{HB}}. \quad (5)$$

By relating this RMS error current to the RMS value of the load current i_{HB}, the SNR is found as:

$$\mathrm{SNR}_{DC-f_s/2} = 20\log_{10}\left(\frac{\hat{i}_{HB}/\sqrt{2}}{\Delta i_{m,RMS}}\right). \quad (6)$$

Note that the SNR is valid in the frequency band ranging from DC to half of the sampling frequency f_s. In this case, $f_s = f_{PWM}$, as one sample is acquired per PWM period. Note that the presented derivation of the SNR can be easily modified to also incorporate ADC sampling twice during a PWM period, at the top and bottom values of the PWM carrier.

Considering additional noise sources that are not related to jitter, e.g., ADC quantization or noise from the ADC's input amplifiers/filters, which can be expressed by an equivalent RMS noise current i_n, the SNR is then given by extending (6):

$$\mathrm{SNR}_{DC-f_s/2} = 20\log_{10}\left(\frac{\hat{i}_{HB}/\sqrt{2}}{\sqrt{\Delta i_{m,RMS}^2 + i_n^2}}\right). \quad (7)$$

Fig. 5 illustrates this equation exemplarily, where i_n is selected such that it corresponds to the amplitude quantization noise of the indicated ADC resolutions [11]. **Fig. 5** (a) sets L_{HB} constant while sweeping $T_{Jit,RMS}$ and **Fig. 5** (b) fixes $T_{Jit,RMS}$ while varying L_{HB} in order to illustrate the sensitivity of the SNR to these important design parameters. The results of numeric computer simulations, which recreate the presented analysis by sampling a half-bridge current signal (which also contains the corresponding current ripple components) at jittery time instants are also illustrated, which verify the validity of the presented analysis. The time step used for the computer simulations is 13.33 ps, which provides a sufficient temporal resolution to cover RMS jitter values < 50 ps.

The analysis shows that low-noise, high-resolution acquisition systems are especially sensitive to the ADC's conversion jitter and the selection of the half-bridge inductance value L_{HB}. With the presence of other noise sources (represented by i_n), this sensitivity is, together with the best achievable SNR, reduced.

The following example demonstrates the impact of this analysis on the design of the half-bridge inductor. Precision power amplifiers for mechatronic positioning applications

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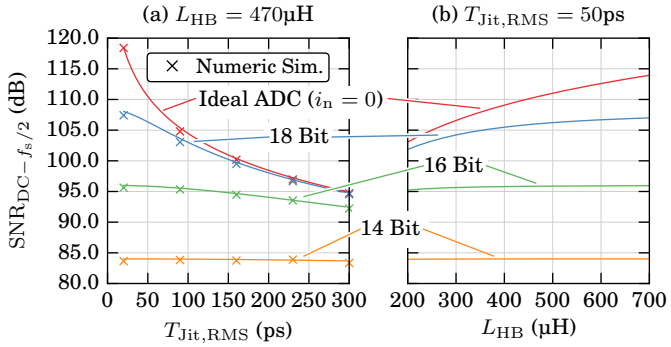

Fig. 5. Best achievable SNR of the half-bridge output current measurement as a function of (a) the ADC conversion signal's RMS jitter and (b), the half-bridge inductance. The analysis is done for different levels of additional noise i_{n} that corresponds to the ADC's amplitude quantization noise (cf. (7)). $u_{\mathrm{DC}} = 400\,\mathrm{V}$, $R_{\mathrm{L}} = 5\,\Omega$, $\hat{i}_{\mathrm{HB}} = 10\,\mathrm{A}$ (assuming that this is also the ADC's full-scale input).

can operate at DC-link voltages up to $400\,\mathrm{V}$ with a pulse repetition frequency of $100\,\mathrm{kHz}$ and a peak output current of $\hat{i}_{\mathrm{HB}} = 20\,\mathrm{A}$ [10]. The half-bridge inductance value is usually chosen such that the peak-to-peak current ripple is limited to $\approx 20\,\%$ of the current amplitude, which would result in a value of $L_{\mathrm{HB}} = 250\,\mu\mathrm{H}$ for this example. Assuming an ADC conversion jitter of $100\,\mathrm{ps}$, and a low-noise acquisition system with an effective resolution of 18 bits, as well as a bridge-tied (full-bridge Class-D topology), resistive load of $10\,\Omega$, a measurement SNR of $103\,\mathrm{dB}$ results. If, however, the half-bridge inductance value is selected as $680\,\mu\mathrm{H}$, the SNR can be increased to $107\,\mathrm{dB}$, which is equivalent to a reduction of sensor noise by a factor of 0.6, in this example.

IV. Conclusion

Low-noise sensor signals are important for digital control loops of precision switched-mode power amplifiers required to provide power output signals with an SNR of $>100\,\mathrm{dB}$. In power electronics converters, isolated ADCs are often employed to acquire current/voltage signals at a different potential. Digital signal isolators are commonly used to facilitate the transfer of the digital ADC output/control signals across the isolation barrier. The jitter of the ADC conversion control signal, which is introduced by such isolators, has to be carefully considered in order to prevent the addition of wideband noise to the acquired signal. Consequently, this work first presents RMS jitter measurements of a wide range of commonly used digital signal isolators with isolation ratings up to $5\,\mathrm{kV_{RMS}}$. Their jitter varies greatly from values as low as $13\,\mathrm{ps}$ up to $250\,\mathrm{ps}$, which renders their selection more tedious, as these values can vary considerably, even between isolators using the same isolation technology.

In a next step, it is analytically derived how the ADC conversion jitter affects the dimensioning of the half-bridge filter inductor in order to achieve low measurement noise. It is shown how the SNR of a synchronously sampled half-bridge output current measurement deteriorates with an increasing slope of the current ripple, which is directly linked to the half-bridge inductance value. Thus, the selection of the half-bridge inductor offers a degree of freedom that can be used to significantly improve the SNR of the half-bridge output current measurement.

In summary, this paper presents two important insights for the construction of ultra-low-noise switched-mode power conversion systems which are required to achieve SNR values in excess of $100\,\mathrm{dB}$ in the converter's power output.

References

[1] S. Buso and P. Mattavelli, *Digital Control in Power Electronics*. Morgan & Claypool, 2015, ISBN: 978-1-62705-753-0.
[2] G.F. Franklin, J.D. Powell and A. Emami-Naeini, *Feedback Control of Dynamic Systems*. Pearson, 2010, ISBN: 9781408264171.
[3] R. Munnig Schmidt, G. Schitter and J. van Eijk, *The Design of High Performance Mechatronics*. Delft University Press, 2011, ISBN: 978-1-60750-825-0.
[4] J. M. Schellekens, "A Class of Robust Switched-Mode Power Amplifiers with Highly Linear Transfer Characteristics," *PhD Thesis, University of Eindhoven*, 2014, ISBN: 978-94-6259-400-5.
[5] H. Takano, S. Watanabe and M. Nakaoka, "Multiple-Bridge PWM Current-Regulated Power Amplifier for Magnetic Resonance Imaging System and its Feasible Digital Control Implementation," in *Pro. of the Industrial Electronics Society*, vol. 2, 1999, pp. 785–790 vol.2.
[6] M. Mauerer, A. Tüysüz and J.W. Kolar, "Voltage/Current Measurement Performance and Power Supply Rejection in All-Digital Class-D Power Amplifiers," in *Proc. of the IEEE Industrial Electronics Society Conference (IECON)*, Oct. 2016, pp. 666–673.
[7] S. Ziegler, R. C. Woodward, H. H. C. Iu and L. J. Borle, "Current Sensing Techniques: A Review," *IEEE Sensors Journal*, vol. 9, no. 4, pp. 354–376, April 2009.
[8] H. P. Forghani-zadeh and G. A. Rincon-Mora, "Current-Sensing Techniques for DC-DC Converters," in *Proc. of the Midwest Symposium on Circuits and Systems*, vol. 2, Aug. 2002, pp. II–577–II–580 vol.2.
[9] Ploug, Rasmus Overgaard and Knott, Arnold and Poulsen, Søren Bang, "GaN Power Stage for Switch Mode Audio Amplification," in *Proc. of the 138th Audio Engineering Society Convention*, May 2015.
[10] M. Mauerer, A. Tüysüz and J.W. Kolar, "Low-Jitter GaN E-HEMT Gate Driver with High Common-Mode Voltage Transient Immunity," *IEEE Transactions on Industrial Electronics*, 2017, DOI: 10.1109/TIE.2017.2677354.
[11] W. Kester, *The Data Conversion Handbook*. Elsevier, 2005, ISBN: 0750678410.
[12] M. P. Chan and P. K. T. Mok, "On-Chip Digital Inductor Current Sensor for Monolithic Digitally Controlled DC-DC Converter," *IEEE Transactions on Circuits and Systems I*, vol. 60, no. 5, pp. 1232–1240, May 2013.
[13] S. S. Saad, "The Effects of Accumulated Timing Jitter on Some Sine Wave Measurements," *IEEE Transactions on Instrumentation and Measurement*, vol. 44, no. 5, pp. 945–951, Oct. 1995.
[14] M. Peng Li, *Jitter, Noise, and Signal Integrity at High-Speed*. Prentice Hall, 2007, ISBN: 9780132429610.
[15] Rohde&Schwarz Co., *Jitter Analysis with the R&S RTO Digital Oscilloscope*, Aug. 2013, Application Note 1TD03_2e.
[16] Texas Instruments Co., *Digital Isolator Design Guide SLLA284A*, Jan. 2009.
[17] G.T. Haigh and B. Chen, *Isolator for Transmitting Logic Signals Across an Isolation Barrier*, 2001, US Patent 6262600.
[18] NVE Co., *GMR in Isolation*, Mar. 2016, Application Bulletin SB-AP-007.
[19] W. Zhang, X. Huang, F. C. Lee and Q. Li, "Gate Drive Design Considerations for High Voltage Cascode GaN HEMT," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2014, pp. 1484–1489.