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2014 J. Semicond. 35 055009

(http://iopscience.iop.org/1674-4926/35/5/055009)

A 14-bit 50 MS/s sample-and-hold circuit for pipelined ADC*

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Abstract: A high performance sample-and-hold (S/H) circuit used in a pipelined analog-to-digital converter (ADC) is presented. Capacitor flip-around architecture is used in this S/H circuit with a novel gain-boosted differential folded cascode operational transconductance amplifier. A double-bootstrapped switch is designed to improve the performance of the circuit. The circuit is implemented using a 0.18 μm 1P6M CMOS process. Measurement results show that the effective number of bits is 14.03 bits, the spurious free dynamic range is 94.62 dB, the signal to noise and distortion ratio is 86.28 dB, and the total harmonic distortion is −91.84 dB for a 5 MHz input signal with 50 MS/s sampling rate. A pipeline ADC with the designed S/H circuit has been implemented.

Key words: sample/hold circuit; pipeline ADC; gain-boosted OTA; bootstrapped switch

DOI: 10.1088/1674-4926/35/5/055009 **EEACC:** 1265H; 1280; 2570

1. Introduction

The development of wireless communication technology has been a major driver for the progress of analog-to-digital converters (ADCs). Due to the advantages of high speed, high precision, and low power consumption, pipeline ADC is playing an important role in wireless communication applications. A block diagram of the designed pipeline ADC structure is shown in Fig. 1. The pipeline ADC is composed of an S/H circuit in the first stage, a 4-bit flash ADC in the second stage, eight 1.5-bit stages and a 3-bit back-end flash ADC. The S/H circuit as the first stage of the pipeline ADC is used to avoid skewing during signal sampling[1] and to reduce most dynamic errors especially those occurring with high frequency input signals. Before a signal is processed by a discrete-time system, it must be sampled and stored. The S/H circuit greatly relaxes bandwidth requirements of the following circuitry. The precision and speed of the S/H circuit critically limit the performance of the pipeline ADC[2]. So the S/H circuit should have better performance than other parts of the pipeline ADC. The proposed S/H circuit is required to achieve 14-bit 50 MS/s due to the demand of a 12-bit 20 MS/s pipeline ADC.

Performance of the S/H circuit is mainly decided by the operational transconductance amplifier (OTA). Using general OTA it is difficult to achieve high gain and wide bandwidth at the same time. Therefore, most of S/H circuits cannot have both high speed and high precision. The proposed S/H circuit includes a novel gain-boosted differential folded cascode operational transconductance amplifier, which presents high gain, high linearity, wide bandwidth and good frequency response properties. Many other techniques are adopted in this design, such as double bootstrapped switches, bottom-plate technique, etc. The measurement results show that, the S/H circuit can achieve the 14.03-bit ENOB, 94.62 dB SFDR, 86.28 dB SNDR and −91.84 dB THD for a 5 MHz input signal frequency with 50 MS/s sampling rate. Hence, the proposed S/H circuit can meet the demands of a 12-bit 20 MS/s pipeline ADC.

2. S/H circuit topology

Two kinds of traditional S/H circuit architectures are implemented widely in the pipeline ADC[3]. The first one is the charge transfer S/H architecture, as shown in Fig. 2(a), and the second one is the capacitor flip-around S/H circuit, as shown in Fig. 2(b).

For the charge transfer S/H architecture, the input signal is sampled into the sampling capacitor during the sampling phase. Only the differential charge is transferred to the feed-back capacitor during the holding phase[4]. The capacitor flip-around S/H circuit doesn't have the charge transferring process. The input signal is sampled into the sampling capacitor during the sampling phase and the sampling capacitor will be flipped to the output during the holding phase in order to achieve the signal transmission.

Compared to the charge transfer S/H architecture, the capacitor flip-around S/H architecture is more suitable for this design. Firstly, for the flip-around S/H architecture, the feedback factor (β) is ideally 1, while β of the charge transfer S/H architecture is ideally 0.5. In order to achieve the same closed-loop bandwidth, the gain bandwidth (GBW) of the charge transfer S/H circuit must be as twice that of the capacitor flip-around S/H circuit. This brings higher power consumption. Secondly, during the sampling phase, the noise of the capacitor flip-

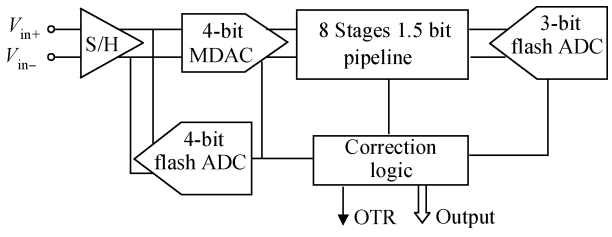

Fig. 1. Block diagram of the pipeline ADC structure.

* Project supported by the National Science and Technology Major Project of China (No. 2012ZX03004008).

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Received 23 October 2013, revised manuscript received 2 December 2013

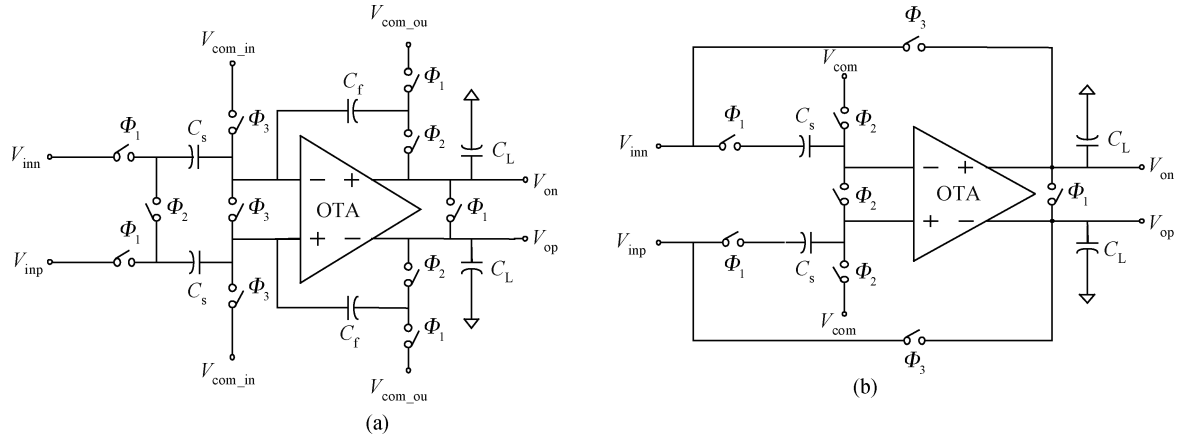

Fig. 2. (a) Charge transfer S/H circuit. (b) Capacitor flip-around S/H circuit.

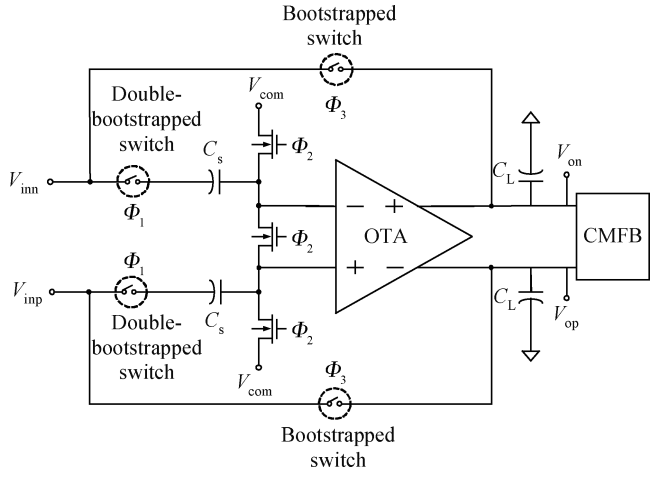

Fig. 3. Architecture of the differential S/H circuit.

around S/H architecture is

$$v_n^2 = \frac{KT}{C_s}. \tag{1}$$

But the noise of the charge transfer S/H architecture is

$$v_n^2 = \frac{2KT}{C_s}. \tag{2}$$

In Eqs. (1) and (2), C_s is the sampling capacitor. During the holding phase, the noise of these two structures is the same. Therefore the noise of capacitor flip-around architecture is lower than charge transfer architecture. Thirdly, the bottom-plate technique can be used in this design to make the charge injection independent of the input signal[5]. In addition, the number of capacitors in the capacitor flip-around architecture is two, which is half that of the charge transfer architecture. Thus, it saves the area and reduces the cost.

Taking all these factors into consideration, this design chooses the capacitor flip-around S/H circuit architecture. The S/H circuit architecture is shown in Fig. 3.

3. Circuit design

3.1. Operational transconductance amplifier design

OTA (operational transconductance amplifier) is the core part of the S/H circuit, which determines the static and dynamic performance of the circuit. According to the requirements of the circuit, there are two most important parameters of OTA. One is the DC-gain, the other is GBW (gain band width).

For the capacitor flip-around S/H circuit, the feedback factor (β) is 1. The static error, caused by limited gain of the OTA, is defined as V_{error}.

$$V_{error} = \frac{1}{1 + A_0}, \tag{3}$$

where A_0 is the DC-gain. The V_{error} must be less than $\frac{1}{2}$LSB.

$$V_{error} < \frac{1}{2}\text{LSB}. \tag{4}$$

In this design, $N = 14$ and the input signal range from –1 to +1 V. We can calculate the requirement of A_0, as is in Eq. (5).

$$A_0 > 84.3\ \text{dB}. \tag{5}$$

Knowing that half of T is the sampling time, we can set 1/3 of the rest time as slew time, and 2/3 of the rest time as set up time. T is the clock period. As is known, the set up time must be less than $\frac{T}{6}$[6].

$$V_{out\_real} = V_{out\_ideal}\left(1 - e^{-\frac{t}{\tau}}\right), \tag{6}$$

where the V_{out_real} is the actual voltage, the V_{out_ideal} is the ideal voltage, and τ is the time constant.

$$\Delta V = \frac{V_{out\_ideal} - V_{out\_real}}{V_{out\_ideal}}, \tag{7}$$

ΔV is as in Eq. (7), which must be less than $\frac{\text{LSB}}{2}$, too. The GBW is given by

$$\text{GBW} = \frac{1}{\beta \cdot 2\pi\tau}. \tag{8}$$

From Eq. (8), we can work out

$$\text{GBW} \geqslant 257\ \text{MHz}. \tag{9}$$

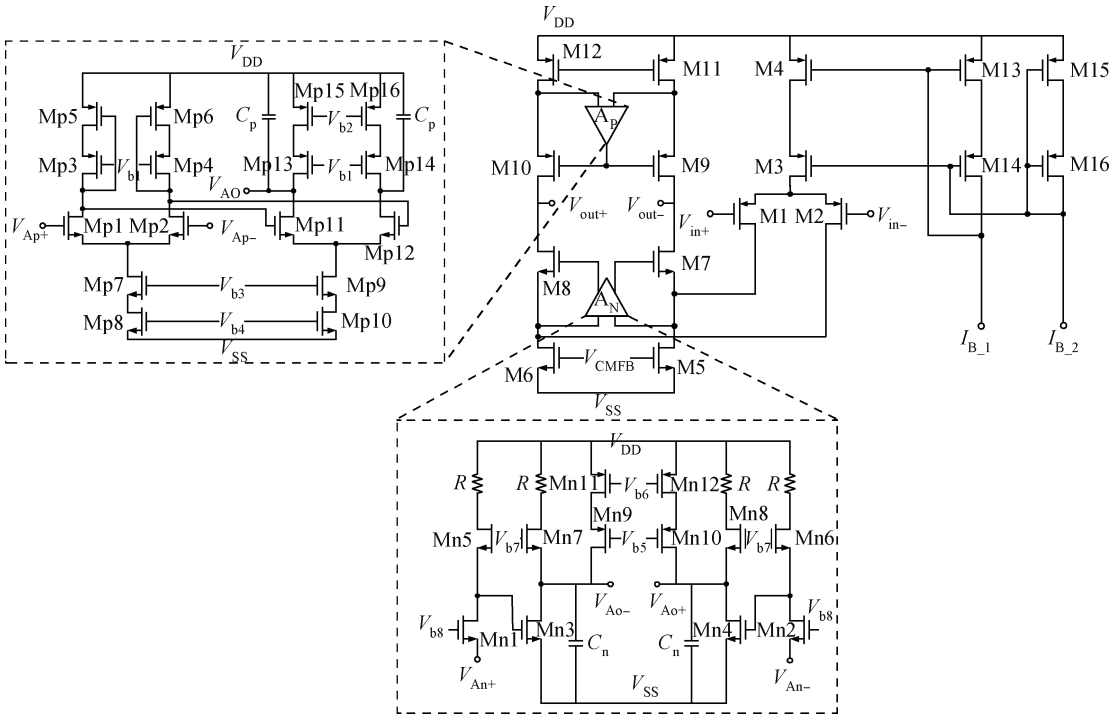

Fig. 4. Gain-boosted operational transconductance amplifier (OTA).

Table 1. Requirements of the OTA.

Supply power	Open-loop DC gain	Unity gain bandwidth	Phase margin	Load
3.3 V	> 84.3 dB	> 257 MHz	> 60°	8 pF

Requirements of the OTA are summarized as follows in Table 1.

The DC-gain of an ordinary single-stage folded cascode OTA is 50–60 dB. Bandwidth of the two-stage operational amplifier is not enough. In this design, we choose the gain-boosted OTA[7]. This structure can reach more than 90 dB DC-gain, and its bandwidth has little difference with single-stage folded cascode OTA[8].

The circuit schematic of the OTA in this design is shown in Fig. 4.

We choose the folded cascode architecture as the core OTA to achieve a higher output swing than the telescope architecture does. PMOS transistors M1 and M2 are used as input differential pairs, which can reduce the parasitic capacitance. Using PMOS transistors as input differential pairs can also improve the phase margin, because it provides a high nondominant pole. The core OTA is composed by the transistors M1–M12. A_P and A_N are auxiliary amplifiers. V_{CMFB} is the common-mode feedback voltage. V_{b1}–V_{b8} are bias voltages, and I_{B_1}–I_{B_2} are bias currents, both supplied by the bias circuit. An auxiliary amplifier improves the gain of the OTA. But it also introduces the zero-pole at the same time[9, 10], which could greatly increase the settling time of the OTA. In order to reduce the effect of zero-pole on settling time, the requirement of auxiliary amplifier is given by

$$\omega_{p1}\beta < \omega_{paux} < \omega_{p2}, \tag{10}$$

where ω_{p1} is the unity-gain frequency of the core amplifier, β is the feedback factor, ω_{paux} is the unity-gain frequency of the auxiliary amplifier, and ω_{p2} is the second pole of the OTA[8].

In this design, auxiliary amplifiers A_P and A_N have different structures. The two-stage operational amplifier is adopted as A_P, due to its high gain. Found from simulations, the gain of a single-stage amplifier is 27 dB, while that of the two-stage amplifier is 48 dB. The gain of the OTA with two-stage amplifier can reach more than 100 dB. On the other hand, for reasons of stability, the auxiliary amplifier unity-gain frequency must be lower than the second-pole frequency of the main amplifier as indicated by Eq. (10). Unity-gain frequency of the two-stage amplifier meets the requirement well. Since the input location of A_P is not the dominant pole or the second dominant pole of the core OTA, the auxiliary amplifier A_P has little impact on the OTA bandwidth. When designing the auxiliary amplifier A_N, there are some other factors which need to be considered. The input location of A_N is the second dominant pole of the core OTA, parasitic capacitance brought by A_N will influence the unity-gain frequency of the OTA. Compared to the common source amplifier, the common gate amplifier is a source input amplifier, which has much smaller input capacitance. In this paper, a common gate amplifier is used in A_N as the input stage to get a wide GBW, and a common source amplifier is connected to the common gate amplifier to achieve appropriate gain.

For a fully differential amplifier, the common-mode feedback circuit is essential[11]. In this design, switch-capacitor CMFB is used, because it has no static power consumption and no constrain to the output swing. The SC-CMFB used in this design is shown in Fig. 5.

In Fig. 5, Φ_1 and Φ_2 are two-phase non-overlapping clocks, V_{bias} is the desired biasing voltage of M5 and M6, and V_{cm} is the desired common mode output voltage. The SC-CMFB implements the adjustment of output common-mode

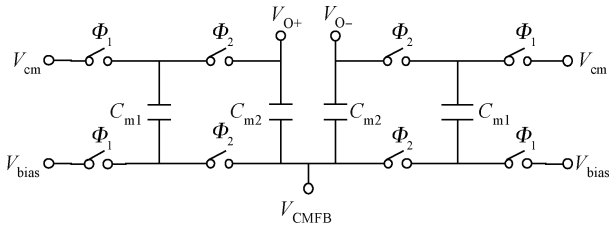

Fig. 5. Switched-capacitor CMFB.

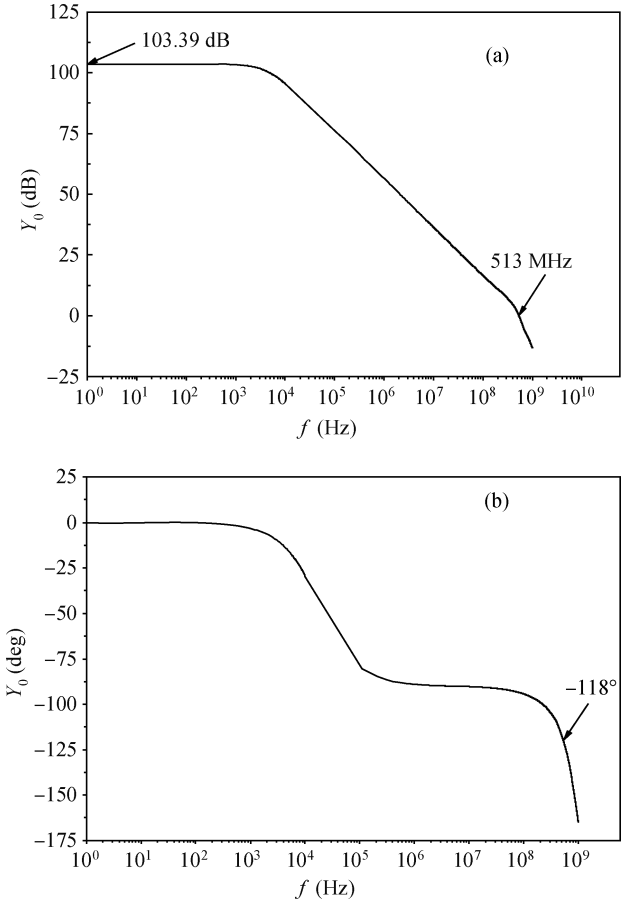

Fig. 6. AC response of the OTA. (a) Amplitude-frequency curve. (b) Phase-frequency curve.

Table 2. Simulation results of the OTA.

Supply power	Open-loop DC gain	Unity gain bandwidth	Phase margin	Load
3.3 V	103.39 dB	513 MHz	62°	8 pF

voltage.

The AC simulation result of the OTA is as follows in Fig. 6.

The results of OTA simulation are listed in Table 2.

Comparing Table 2 with Table 1, we can conclude that the designed OTA meets the requirement of the S/H circuit.

3.2. Double-bootstrapped switch

The switching circuit is one of the key modules of S/H circuit, especially the sampling switch (controlled by Φ_1 in Fig. 3). Because it can affect the accuracy of S/H circuit and lead to non-linearity. Channel charge injection, clock feedthrough, and on-resistance are the main factors influencing the switch performance. Using the bottom-plate technique and dummy technique can restrain the effect of channel charge injection and clock feedthrough. However, these measures have nothing to do with improving the non-linearity of on-resistance of the switch.

For a short channel device, R_{on} (on-resistance) is given by[5]

$$R_{on} = \frac{1 + \dfrac{V_D - V_S}{E_C L}}{\mu_n C_{ox} \dfrac{W}{L}\left(V_G - \dfrac{V_S}{2} - \dfrac{V_D}{2} - V_{TH}\right)}, \quad (11)$$

$$V_{TH} = V_{TH0} + \gamma\left(\sqrt{|2\Phi_F + V_S - V_B|} - \sqrt{|2\Phi_F|}\right), \quad (12)$$

where V_G, V_S, V_D and V_B are the voltages on the transistor's gate, source, drain and bulk terminals, E_C is electric field intensity. From Eq. (11), we can see that the factors influencing R_{on} mainly from two aspects: one is the voltage $V_G - \frac{V_S}{2} - \frac{V_D}{2}$; the other is the change of V_{TH} caused by bulk effect. In addition, the drain–source voltage, the electric field intensity E_C, and the device channel length can all affect R_{on}.

The proposed double-bootstrapped switch is shown in Fig. 7. The same structure is used on gate-to-source and gate-to-drain terminals. It can improve the linearity effectively.

Taking the left side circuit as an example, the circuit operates as follows: as CK = 0, $\overline{\text{CK}}$ = 1, M12a, M13a are on, M5a is off. The gate of MS is connected to V_{SS} through M12a and M13a. MS is off. At the same time, the capacitor C_{3a} is charged through M3a and M7a to V_{DD}. As CK = 1, $\overline{\text{CK}}$ = 0, M5a opens. The up plate of C_{3a} is connected to the gate of MS, and the bottom plate of C_{3a} is connected to V_{in} through M2a. The capacitor is connected simultaneously between the gate-source of the switch MS. The voltage $(V_G - \frac{V_S}{2} - \frac{V_D}{2})$ is equal to V_{DD}. The gate–source voltage is V_{DD}, so is the gate–drain voltage. Because gate–source voltage and gate–drain voltage do not change with V_{in}, the linearity of R_{on} is improved greatly. In addition, the transistor Md is a dummy structure, which is used to restrain the effect of channel charge injection and clock feedthrough. The simulation result of the double-bootstrapped switch is shown in Fig. 8. The setup time is 2 ns, and the hold time is 7 ns.

The feedback switch (controlled by $\Phi 3$ in Fig. 3) also needs higher linearization. In this design, a simple bootstrapped switch is used as feedback switch. The structure is as shown in Fig. 9.

4. The measurement result

The pipeline ADC is implemented in a standard 0.18 μm 1P6M CMOS process. Figure 10 shows the die photomicrograph of the fabricated chip. The S/H circuit is laid out on the right of the chip, and the area is 1 mm^2.

In the test experiment, a Rigol DG5071 arbitrary waveform generator is used to supply the input sine wave and Tektronix MSO4054 oscilloscope is used to observe the transient response. The measured results with an input of 5 MHz analog

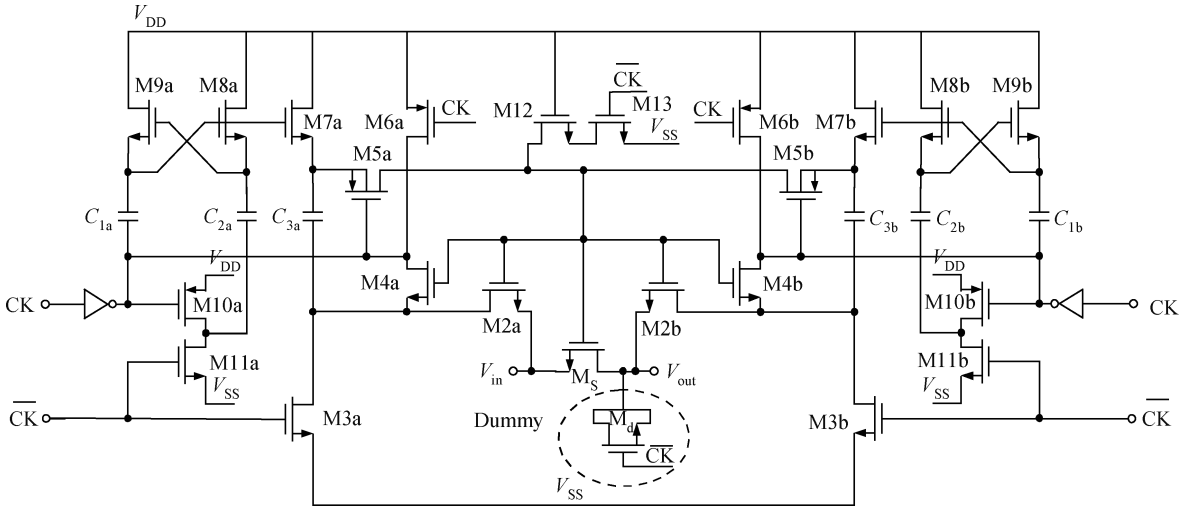

Fig. 7. Double-bootstrapped switch.

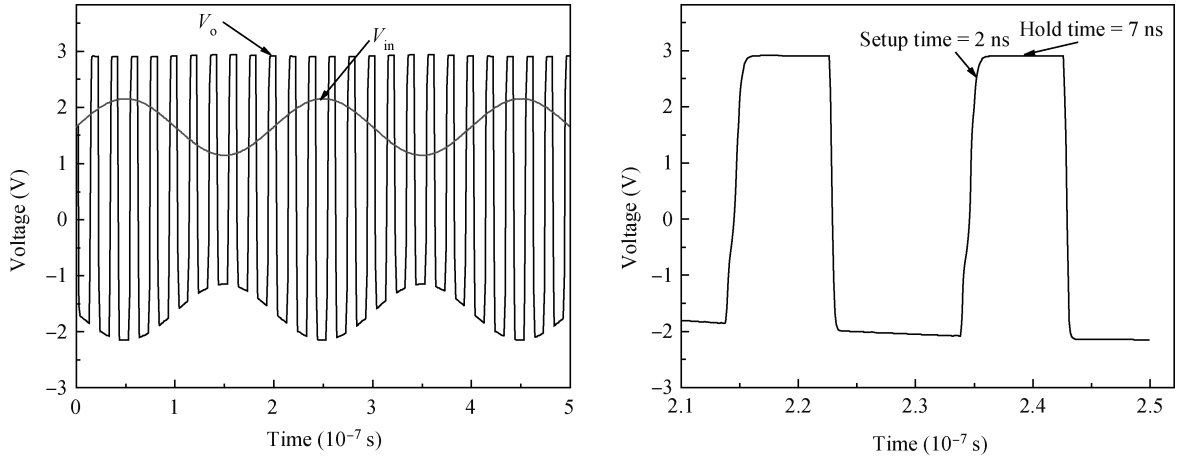

Fig. 8. Simulation result of the double-bootstrapped switch.

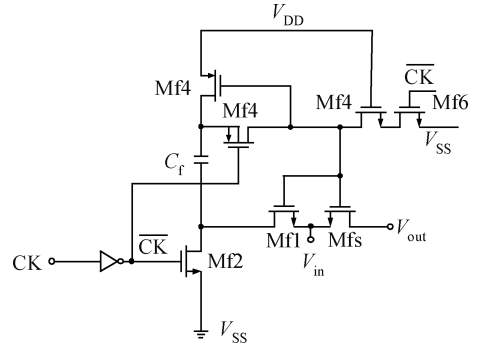

Fig. 9. Bootstrapped switch.

Table 3. Measured results of the S/H circuit.

Parameter	Value
Signal frequency	5 MHz
Sampling rate	50 MS/s
SFDR	94.62 dB
THD	−91.84 dB
SNDR	86.28 dB
ENOB	14.03 bits
Input range	2 Vpp
Supply voltage	3.3 V

sine waveform and a sampling rate of 50 MS/s are summarized in Table 3. Figure 11 shows the output spectrum with 5 MHz analog input. Figure 12 shows the variation of the SFDR across several frequencies of input signals, and it can be clearly seen that the SFDR is falling from 110.97 dB when the input signal is 100 kHz to 88.84 dB when the input signal is 20 MHz. Test results show that performance of the S/H circuit degrades slightly when the input frequency is up to 20 MHz.

The comparison of the presented work with other recently published S/H circuits is shown in Table 4. This work has the best balance of precision and speed while maintaining a competent overall performance.

5. Conclusion

In this paper, a fully differential S/H circuit at a frequency of 50 MHz has been described. By using a novel gain-boosted differential folded cascode operational transconductance amplifier (OTA), and a double-bootstrapped switch, the S/H cir-

Table 4. The comparison of the performance with other S/H circuit.

Specification	S/H in Ref. [12] 2009	S/H in Ref. [13] 2010	S/H in Ref. [14] 2011	This work
Technology (μm)	0.35	0.35	0.18	0.18
Resolution (bits)	10	12	10	14
Sampling rate (MS/s)	50	50	100	50
SFDR (dB)	67 @ 2.5 MHz	87.6 @ 1 MHz	85.4 @ 10 MHz	94.6 @ 5 MHz
Power consumption (mW)	13.6	/	7.6	15.4
Supply voltage (V)	3.3	3.3	3.3	3.3

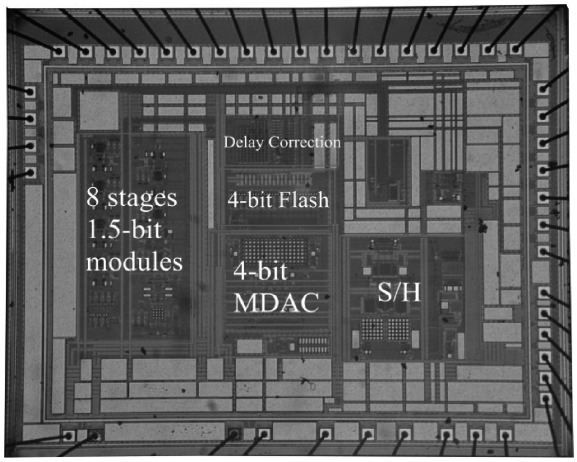

Fig. 10. Micrograph of the pipeline ADC.

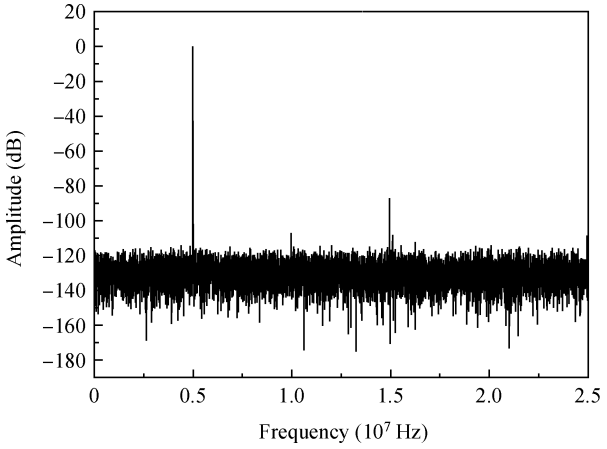

Fig. 11. The output spectrum with a 5 MHz analog input.

cuit reaches high speed, high resolution and good linearity. The measurement results show that the S/H circuit achieves a good performance. The S/H circuit meets the requirement of the designed pipeline ADC.

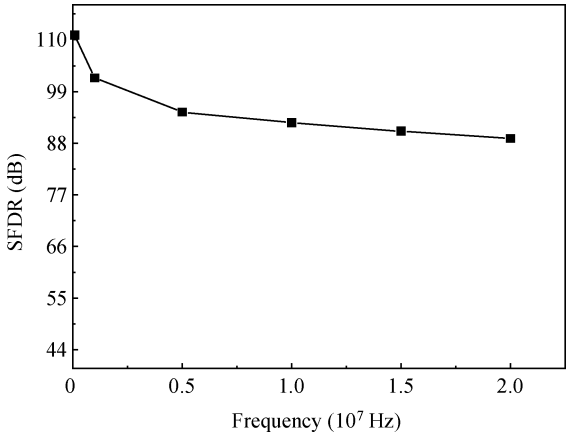

Fig. 12. SFDR versus input signal frequency.

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