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CAD tools for efficient RF/microwave transistor modeling and circuit design

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Abstract In today's radiofrequency and microwave communication circuits, there is an ever-increasing demand for higher integration and miniaturization. This trend leads to massive computational tasks during simulation, optimization and statistical analyses, requiring robust modeling tools so that the whole process can be achieved reliably. In this paper, the authors proposed frequency- and time-domain computer-aided design tools that can characterize RF/microwave field effect and heterojunction bipolar transistors and efficiently predict a circuit performance. The proposed tools are demonstrated through examples.

Keywords CAD · FET · Fuzzy logic · HBT · KBNN · Neural networks · PKI · Time domain

1 Introduction

Communication equipment is now fully integrated in our daily life: cellular phones and pagers, computer peripherals, security systems, wireless positioning systems for cars and airplanes, remote devices, to name a few. Combined to constraining factors like cost, size, and weight, the drive in the microelectronics industry for ever-higher integration and reliability requires a permanent upgrading of existing radiofrequency (RF) and microwave Computer-Aided Design (CAD) tools [1–5]. As such, there is a challenge for further research towards development of efficient modeling and design tools for RF/microwave communication systems.

In the recent years, neural (NN) and fuzzy-neural networks (FNN) gained popularity as fast and flexible vehicle to RF/microwave modeling, simulation and optimization [6–10]. Trained from measured/simulated data, fast and accurate neural models can be utilized in place of computationally intensive physics/EM models to speed-up the overall design process.

In this paper, the authors developed robust neural-based CAD tools to efficiently model field effect (FETs) and heterojunction bipolar transistors (HBTs) and accurately predict frequency-domain circuit responses. A time-domain approach was also investigated to help developing enhanced transistor models. The proposed tools are demonstrated through examples.

2 Neural and fuzzy-neural networks

A neural network (NN) is a model that has the ability to learn and generalize arbitrary continuous multi-dimensional input–output relationships. The most commonly used configuration is the Multi Layer Perceptrons (MLP) where the neurons are grouped into layers [8]. However, since MLP is a kind of black-box model structurally embedding no-problem dependant information, the training process could necessitate a huge amount of data to efficiently learn the input/output relationships [8–10].

Generating large amounts of training data could be very expensive for microwave problems, e.g., those involving electromagnetic (EM) simulation samples in the model

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input parameter space [6–9]. Existing microwave knowledge can provide additional information to the original problem that may not be adequately represented by the limited training data. In Knowledge-Based Neural Networks (KBNN), the neural network can help bridge the gap between empirical models and EM solutions [8, 9].

Compared to MLP structures, the prior knowledge in KBNN gives neural network more information about the original microwave problem, besides the information included in the training data. Consequently, KBNN models have better reliability when training data is limited or when the model is used beyond training range [8].

Similarly to the KBNN, the Prior Knowledge Input (PKI) neural structure could complement the capability of learning and generalizing of the neural network. The structure uses an empirical model as the prior knowledge part and a neural network to map between the inputs of the original problem, outputs of the empirical model and the outputs of the NN model. Compared to MLP, the outputs of the empirical model help getting better accuracy [8].

Furthermore, combining fuzzy systems and neural networks can significantly improve the learning ability of a model, especially when the solution is not unique or in presence of uncertainties/noise in data used in model training. This is the case when RF/microwave designers use an electrical equivalent circuit to characterize a transistor behavior: this circuit is not unique but strongly dependent on the technology, the operating frequency, and the accuracy of the input measured data [11–14]. Among existing fuzzy methods, the fuzzy c-means (FCM) method is a data clustering technique wherein each data point belongs to a cluster to some degree that is specified by a membership grade [15].

3 Frequency-domain transistor modeling

Since FETs and HBTs are widely used in RF/microwave communication circuits, a large number of modeling approaches have been proposed [16–20]. Detailed physics-based transistor models are accurate but slow. Table look-up models can be fast, but suffer from the disadvantages of large memory requirements and limitations on number of parameters.

Nevertheless they are difficult to develop, frequency-domain equivalent circuit models remain the most used modeling approach, where the element values can be determined either by direct extraction [16] or by optimization-based extraction [17]. Fast and simple to implement, direct-extraction techniques provide adequate values for the more dominant circuit model elements but they cannot determine all the extrinsic elements uniquely [11, 19]. On the other side, optimization-based extraction techniques are more accurate but computationally intensive and relatively sensitive to the choice of starting values. Also, to make them attractive to non-experienced users, such extraction techniques often assume a *prior universal* circuit topology referred as the *FET standard topology* or FET circuit #1 (Fig. 1) [18] and the *HBT standard topology* or HBT circuit #1 (Fig. 2) [21].

Determining the most suitable small-signal equivalent circuit topology and accurately extracting its element parameters is the aim of the proposed approach. Based on a large literature review, the authors created a library with different circuit topologies displayed in Figs. 3, 4, 5, and 6 [22–25] and Figs. 7, 8, 9, and 10 [21, 26–28] for FETs and HBTs, respectively.

Based on frequency-domain transistor S-parameters, a standard topology extraction was first performed and the obtained S-parameters $\left(S^{s}_{ij},\ i,j=1,2\right)$ from the standard topology were compared to the given measured S-parameters (noted as $S^{m}_{ij},\ i,j=1,2$). If the difference is greater than a user-defined error, a new circuit topology should be selected from the topology library. By combining the FCM

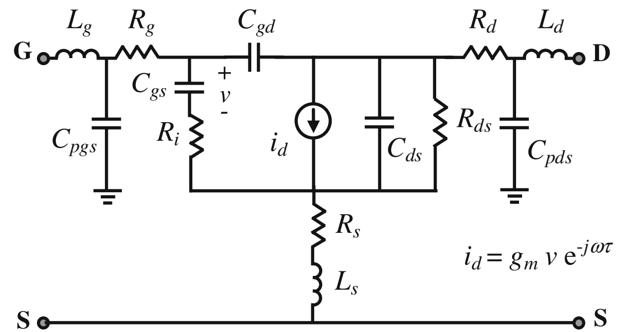

Fig. 1 FET standard circuit topology (# 1) [18]

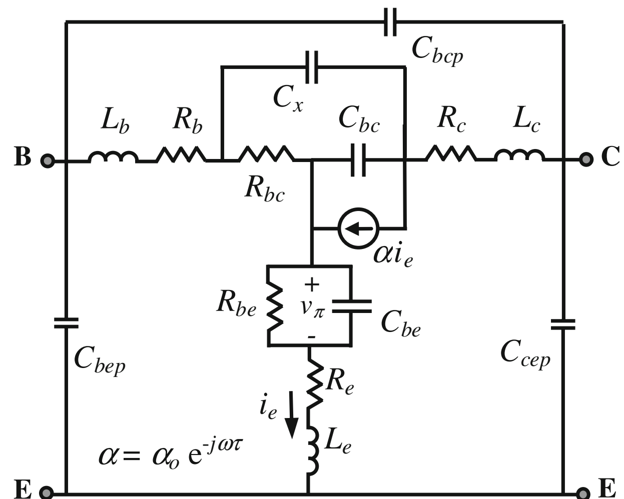

Fig. 2 HBT standard circuit topology (#1) [21]

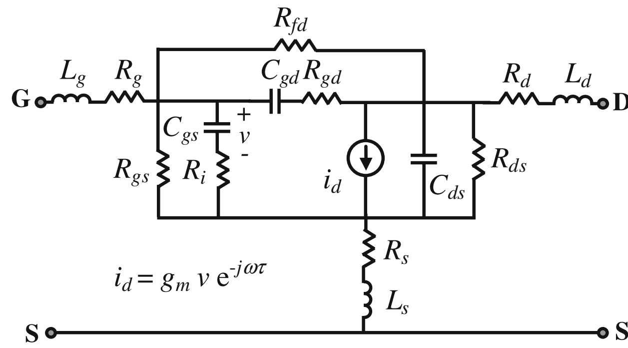

Fig. 3 FET circuit topology #2 as reported in [22]

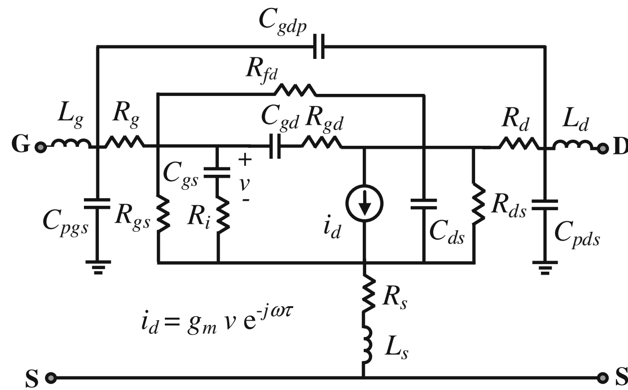

Fig. 4 FET circuit topology #3 as reported in [23]

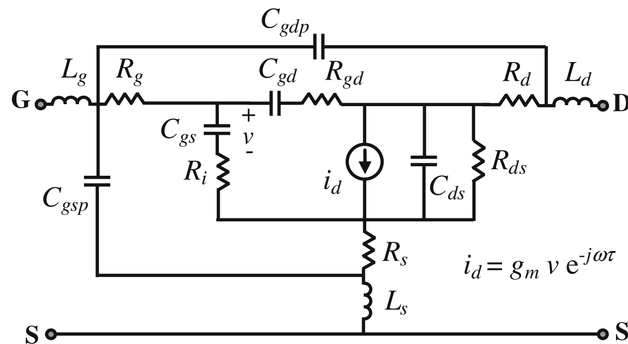

Fig. 5 FET circuit topology #4 as reported in [24]

method and the small-signal representation of the device behavior, the most suitable transistor topology can be obtained following the algorithm shown in Fig. 11.

In fact, for any circuit #k of the library, the related S^k matrix was compared to the given input S^m matrix and each element of the 2×2 error matrices $E^{k,\mathrm{Re}}$ and $E^{k,\mathrm{Im}}$,

$$E_{ij}^{k,\mathrm{Re}} = \mathrm{Re}\left(S_{ij}^{k} - S_{ij}^{m}\right),\ E_{ij}^{k,\mathrm{Im}} = \mathrm{Im}\left(S_{ij}^{k} - S_{ij}^{m}\right) \quad i,j = 1,2 \tag{1}$$

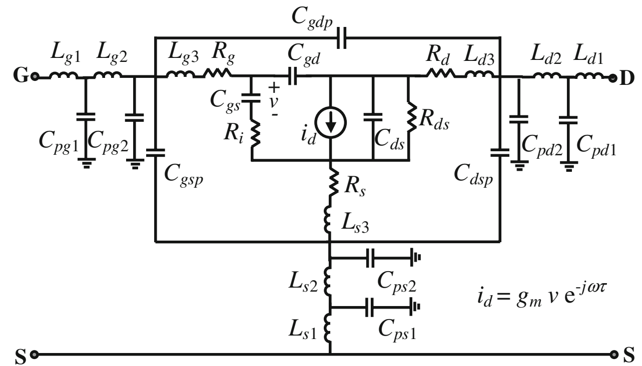

Fig. 6 FET circuit topology #5 as reported in [25]

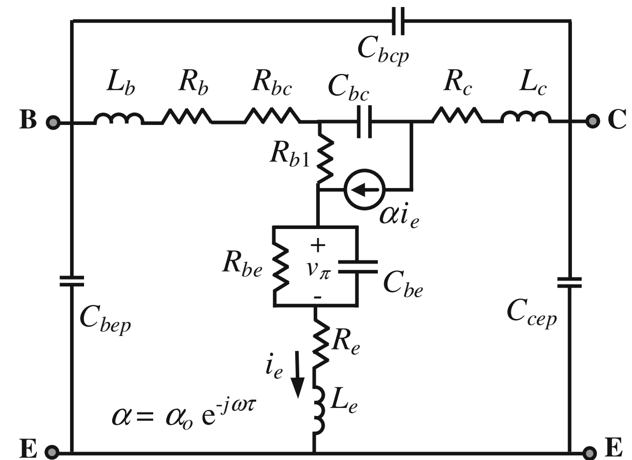

Fig. 7 HBT circuit topology #2 as reported in [21]

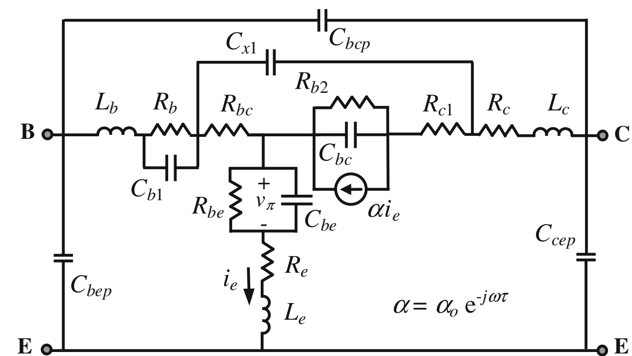

Fig. 8 HBT circuit topology #3 as reported in [26]

can receive a fuzzy score depending on its value. Therefore, topology #k with smallest $E^{k,m}$,

$$E^{k,m} = \sum_{i=1}^{2}\sum_{j=1}^{2}\left\{\left[\mathrm{Re}\left(S_{ij}^{k} - S_{ij}^{m}\right)\right]^2 + \left[\mathrm{Im}\left(S_{ij}^{k} - S_{ij}^{m}\right)\right]^2\right\} \tag{2}$$

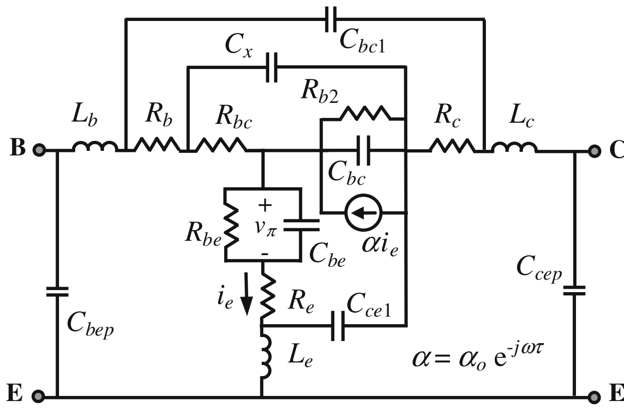

Fig. 9 HBT circuit topology #4 as reported in [27]

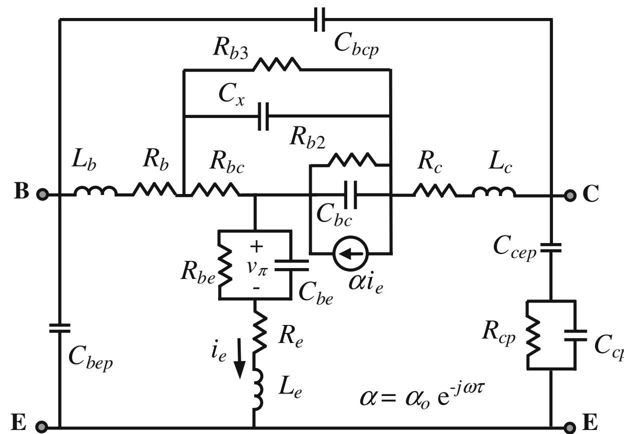

Fig. 10 HBT circuit topology #5 as reported in [28]

i.e., smallest score, can be selected as the most suitable equivalent model topology. Here, Re(*) and Im(*) denote real part and imaginary part, respectively. However, since there is *no prior* knowledge on the input S-parameters, it was impossible to compute numerically (2). Let $\{\Omega^s\}$ be the set of P_s elements $\Omega_p^s(p = 1\ldots P_s)$ in the standard topology. A symbolic code was developed using [29] to analytically derive the following nonlinear functions

$$S_{ij}^k = f_{ij}^k\left(S_{ij}^s, \{\Omega^k\}\right) \quad i,j = 1,2 \quad k = 1\ldots5 \qquad (3)$$

where $\{\Omega^k\}$ is the set of the P_k elements added in circuit #*k* versus the standard topology, e.g.,

$$\{\Omega^2\}_{\mathrm{FET}} = \{R_{fd}, R_{gd}, R_{gs}\}\big|_{C_{pgs}=C_{pds}=0}$$
$$\{\Omega^3\}_{\mathrm{FET}} = \{R_{fd}, R_{gd}, R_{gs}, C_{gdp}\}$$
$$\{\Omega^4\}_{\mathrm{FET}} = \{R_{gd}, R_{gdp}, C_{gsp}\}\big|_{C_{pgs}=C_{pds}=0}$$

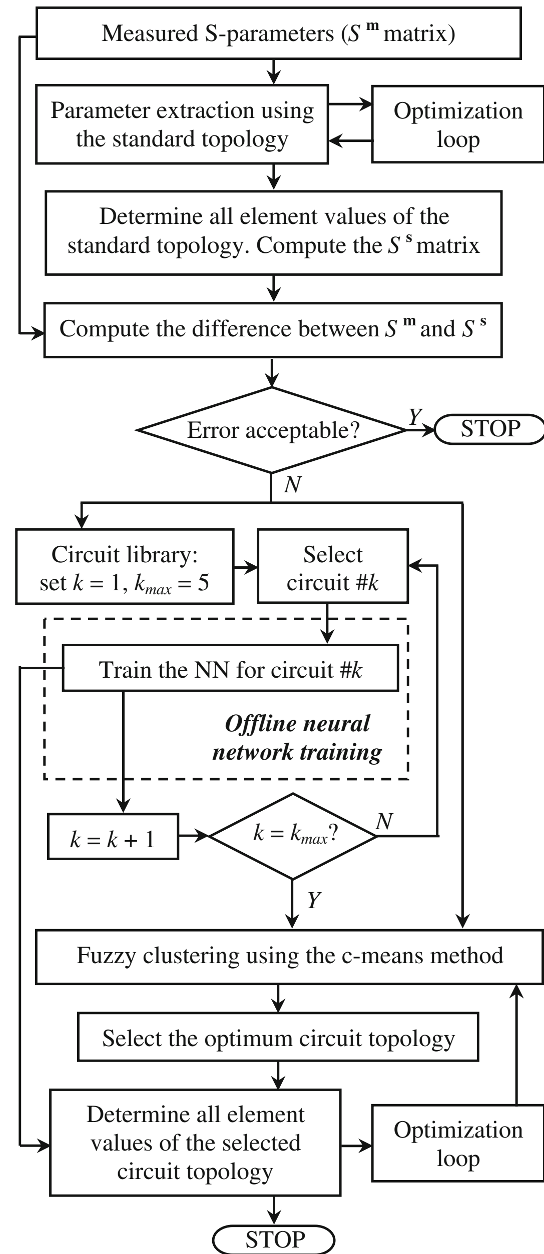

Fig. 11 Algorithm of the proposed method

for the FET, and

$$\{\Omega^2\}_{\mathrm{HBT}} = \{R_{b1}\}\big|_{C_x=0} \quad \{\Omega^3\}_{\mathrm{HBT}} = \{C_{b1}, C_{x1}, R_{b2}, R_{c1}\}\big|_{C_x=0}$$

$$\{\Omega^4\}_{\mathrm{HBT}} = \{C_{bc1}, R_{b2}, C_{ce1}\}\big|_{C_{bcp}=0}$$
$$\{\Omega^5\}_{\mathrm{HBT}} = \{R_{b3}, R_{b2}, R_{cp}, C_{cp}\}$$

$$\{\Omega^5\}_{\mathrm{FET}} = \left\{ \begin{array}{r} C_{gdp}, C_{gsp}, C_{dsp}, C_{pg1}, C_{pg2}, C_{ps1}, C_{ps2}, C_{pd1}, C_{pd2}, L_{g1}, \\ L_{g2}, L_{s1}, L_{s2}, L_{d1}, L_{d2} \end{array} \right\}_{C_{pgs}=C_{pds}=0}$$

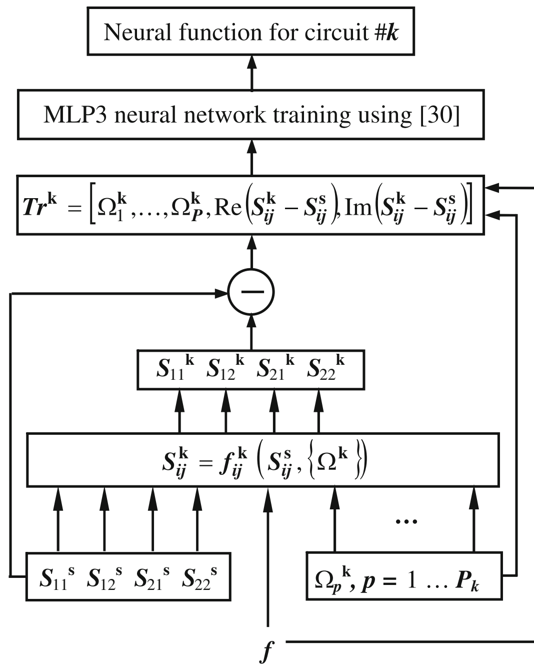

Fig. 12 Neural network model development for circuit #k

for the HBT. Thus, the following alternative fuzzy criteria was defined for each topology #k

$$E^{k,s} = \sum_{i=1}^{2}\sum_{j=1}^{2}\left\{\left[\mathrm{Re}\left(S_{ij}^k - S_{ij}^s\right)\right]^2 + \left[\mathrm{Im}\left(S_{ij}^k - S_{ij}^s\right)\right]^2\right\}. \tag{4}$$

Since these equations are strongly interdependent and highly nonlinear, we used neural networks to learn them. By varying the values of the elements $\Omega_p^k (p = 1, \ldots, P_k)$ of set $\{\Omega^k\}$, we can compute the S^k scattering matrix and therefore, the difference $\{S^k - S^s\}$. As shown in Fig. 12, the resulting data in the form of

$$Tr^{\mathbf{k}} = \left[\underbrace{\mathrm{Re}\left(S_{ij}^k - S_{ij}^s\right), \mathrm{Im}\left(S_{ij}^k - S_{ij}^s\right)}_{8\text{ inputs } (i,j=1,2)}, \underbrace{\Omega_1^k, \ldots, \Omega_{p_k}^k}_{p_k\text{outputs}}\right] \tag{5}$$

was submitted to a three-layer (MLP3) neural network structure for training using [30]. The input layer has 9 neurons (the 4 real and 4 imaginary parts in (5) and the operating frequency f) while the output layer contains P_k neurons. The hidden layer is composed of 22–45 neurons depending on the circuit data file under training. A final extraction was then performed using

$$\Omega = \left[\Omega_1^k, \ldots, \Omega_{P_k}^k, \Omega_1^s, \ldots, \Omega_{P_s}^s\right] \tag{6}$$

as starting vector for the final optimization round. Since this vector is close to the final solution, this procedure assures a very fast convergence. In fact, the maximum number of iterations for 100 different sets of S-parameters did not exceed ten iterations with a maximum computing time of 11 s and a user-defined error of 2%.

4 Frequency-domain transistor modeling: examples

4.1 Example 1: MESFET with simulated data

The first device to be characterized is the GaAs MESFET reported in [24] using FET topology #4. Since in this paper all circuit element values are given as well as the final error between measured and calculated S-parameters, a reliable comparison can be performed for a full validation.

In fact, by comparing the S-parameters (Fig. 13) and the extracted values given in [24] with those obtained in 2.3 s using our technique (Table 1), topology #4 achieved the closest agreement with a smaller final error (2.9 vs. 8.4% as in [24]) defined for a set of N_f selected frequency values fq ($q = 1,\ldots, N_f$) as [24]

$$E^{k,m} = \sum_{q=1}^{N_f}\sum_{i=1}^{2}\sum_{j=1}^{2}\left|1 - \frac{S_{ij}^k(f_q)}{S_{ij}^m(f_q)}\right|^2. \tag{7}$$

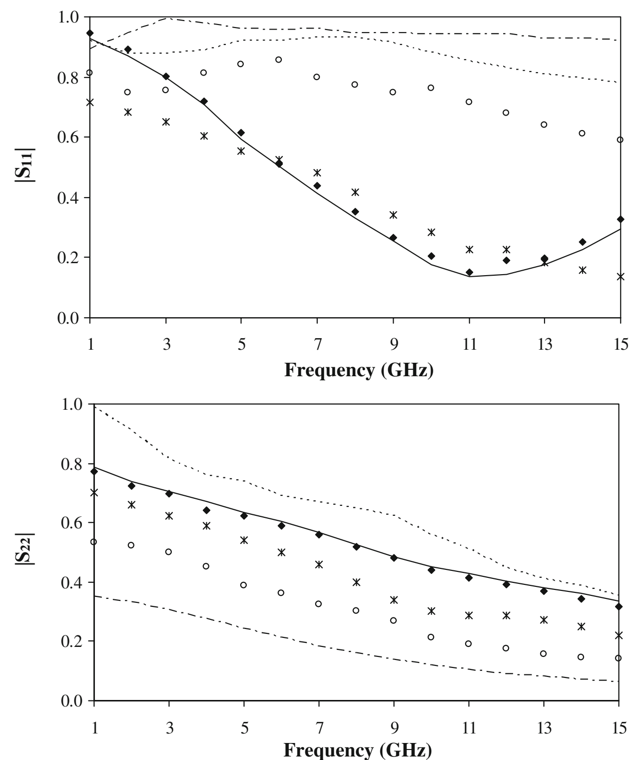

Fig. 13 MESFET: comparison of S_{11} and S_{22} parameters given in [24] (◆) with those extracted using: - - - -, standard topology; – –, topology #2; **o**, topology #3; —, topology #4; *, topology #5

Table 1 MESFET: comparison between the parameters reported in [24] and our computed results

	[24]	Our values
C_{gs} (pF)	0.277	0.215
C_{gd} (pF)	0.0207	0.0211
C_{ds} (pF)	0.0993	0.101
g_m (mS)	26.9	27.3
τ (ps)	1.22	1.25
R_i (Ω)	15.3	15.1
R_{gd} (Ω)	43.8	43.6
R_{ds} (Ω)	215	218
R_g (Ω)	8.9	9.1
R_s (Ω)	7.5	7.3
R_d (Ω)	13.6	13.2
L_s (nH)	0.437	0.441
L_d (nH)	0.452	0.447
L_g (nH)	0.254	0.258
C_{gsp} (pF)	0.0409	0.0397
C_{gdp} (pF)	0.001	0.001
Error (%)	8.4	2.9

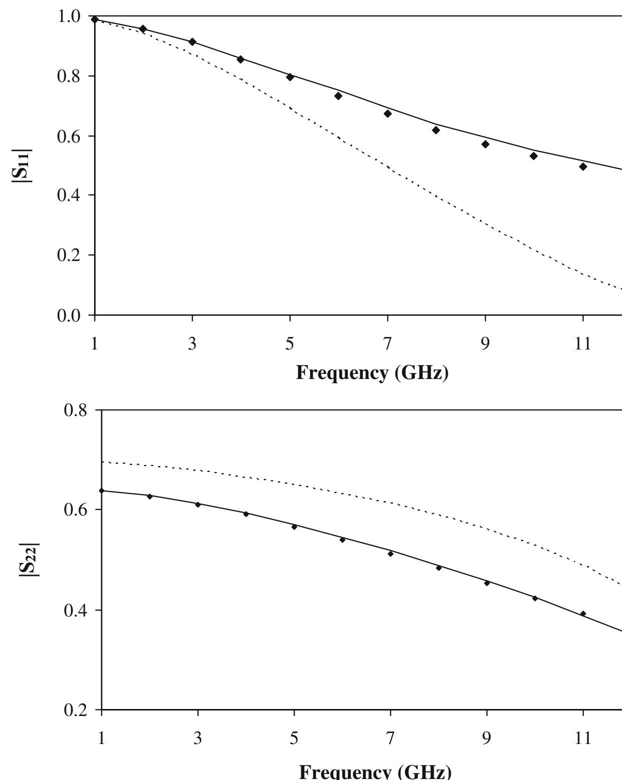

Fig. 14 PHEMT: comparison of measured S_{11} and S_{22} parameters (◆) with those extracted using: - - - -, standard topology; —, topology #3

4.2 Example 2: PHEMT with measured data

In a second example, we measured the S-parameters of an on-wafer AlGaAs/InGaAs-GaAs pHEMT at $V_{DS} = 5$ V and $I_D = I_{DSS}/2 = 60$ mA. After 2.1 s, our method showed that FET topology #3 is the most appropriate (Fig. 14) with a final error of 1.8%, smaller than the specified user-defined error (i.e., 2%).

4.3 Example 3: HBT

The third device to be modeled is a 1 × 10 InP/GaInAs HBT proposed in [27] using HBT topology #4. A similar close agreement was shown with published results (Fig. 15; Table 2).

A KBNN structure was also built using the same data range to enhance the two-stage model prediction beyond the training range. The empirical coarse model was given from an MLP neural model generated from the same data.

As expected, the PKI model allowed significant reduction of the CPU time (0.2 vs. 12 s for the original simulation run in the commercial simulation ADS [25]). Furthermore, and as expected, KBNN showed a better agreement with original data from [25] than those given by the MLP for input values beyond the training range (Table 3).

5 Circuit modeling and design

For circuit level, we trained a PKI structure of a one-stage amplifier to learn the input–output relationships and therefore to predict a two-stage amplifier response. The PKI input vector contained the input power, the DC bias, and the frequency. The output vector contained the output power of the two-first harmonics. The data generation was performed from 0.5 to 1.5 GHz, step size of 0.025 GHz, while the DC voltage was varied from 2 to 4 V, step size of 0.2 V. The input power was swept from −100 to −90 dBm, step size of 1 dBm.

6 Discussions about the proposed approach

Equivalent circuit representations of high-frequency transistors are widely used in the centimeter range. However, such circuits are based on frequency-domain data (i.e., S-parameters) and utilize lumped elements so, as operating frequency increases to the millimeter wave range, the physical dimensions of the transistor electrodes become comparable to the wavelength making this model inefficient. Thus, time-domain full-wave analysis involving fully distributed elements should be considered. However, this type of analysis is highly time consuming [31], even if

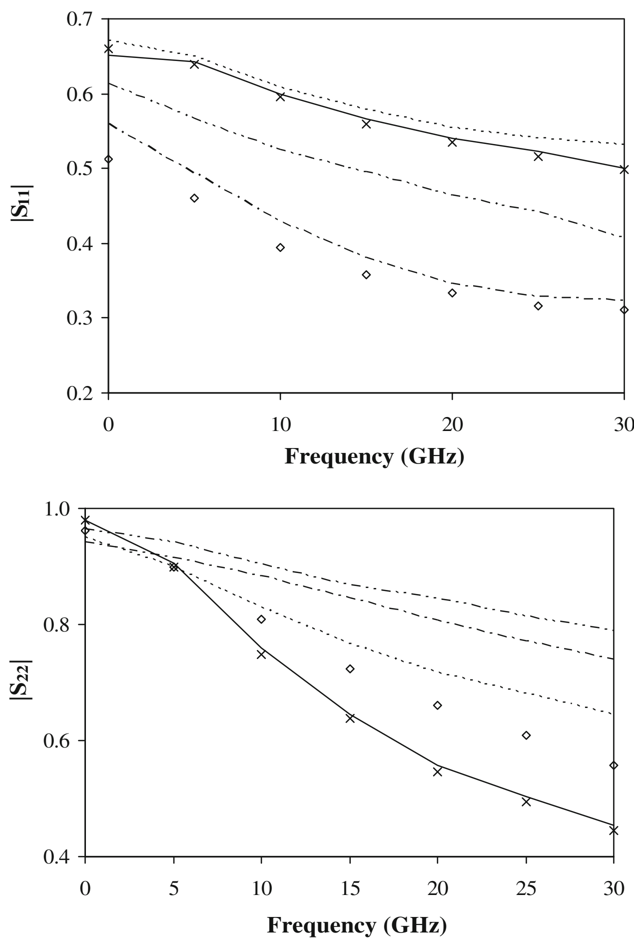

Fig. 15 HBT: comparison of S_{11} and S_{22} parameters given in [27] (×) with those extracted using: - - -, standard topology; – - - –, topology #2; ◇, topology #3; —, topology #4; – - –, topology #5

Table 2 HBT: comparison between the parameters reported in [27] and our computed results

	[27]	Our values
R_e (Ω)	8.73	8.71
R_b (Ω)	2.6	2.5
R_c (Ω)	0.85	0.86
R_{be} (Ω)	3.4	3.3
R_{bc} (Ω)	15.4	15.5
R_{b2} (Ω)	30	30
L_e (pH)	1.8	1.8
L_b (pH)	60	61
L_c (pH)	65	67
C_{be} (fF)	10	9.7
C_{bc} (fF)	5.1	5.2
C_{ce1} (fF)	3	3
C_{bc1} (fF)	2	1.8
C_{bep} (fF)	25	26
C_{cep} (fF)	25	26
C_x (fF)	31	33
α_o	0.947	0.939
τ_1 (ps)	0.37	0.36
τ_2 (ps)	0.64	0.66
Error (%)	–	1.7

some numerical methods have been recently proposed for simulation time reduction [20].

As a result, semi-distributed models, which can be easily implemented in CAD routines of simulators, become a suitable alternative to overcome this limitation [32]. In fact, a fully distributed model can be considered as a modified version of a semi-distributed model, in which the number of slices goes to infinity [33]. Thus, the proposed fully distributed model can include the effect of wave propagation along the electrodes more accurately than the semi-distributed model although the CPU time of this model is a little greater than the slice model.

For accurate device modeling, when the device physical dimensions become comparable to the wavelength, the input active transmission line has a different reactance from the output transmission line [20]. Therefore, they exhibit different phase velocities for the input and output signals. So by increasing the frequency or device dimension the phase cancellation due to the phase velocity mismatching will affect the performance of the device [34, 35].

In the proposed modeling approach, the transverse electromagnetic (TEM) wave propagation can be inspected on the electrodes of the device and a fully distributed model with three active coupled lines can be embodied in the active multi-conductor transmission lines equation. To achieve this, the transmission line theory can be applied to a segment of transistor to obtain the wave equation in a transistor structure and the obtained system of differential equations (active multi conductor transmission line equations) will be solved.

Since a time domain analytical solution does not exist, this system needs to be solved numerically. The Finite Difference Time Domain (FDTD) method is widely used in solving various kinds of electromagnetic (EM) problems, wherein lossy, nonlinear, inhomogeneous media and transient problem can be considered [36]. Each unit segment will be divided into two parts, active and passive, whose elements are per unit length. The passive part describes the behavior of the transistor as a three passive coupled line. The active part relates to the standard performance of a transistor that can be modeled by a linear circuit.

For illustration, let us consider a typical distributed model of a millimeter-wave FET as shown in Fig. 16. It consists of three coupled electrodes (three active transmission lines). In the lower part of the high frequency spectrum, the longitudinal EM field is very small in magnitude as compared to the transverse field [35]. Therefore, a

Table 3 Two-stage amplifier: fundamental output power $\{P_{\text{out}}\ (\omega)\}$ and second harmonic output power $\{P_{\text{out}}\ (2\omega)\}$

	$P_{\text{in}}(\omega) = -95$ dBm		$P_{\text{in}}(\omega) = -85$ dBm	
	$P_{\text{out}}\ (\omega)$ in dBm	$P_{\text{out}}\ (2\omega)$ in dBm	$P_{\text{out}}\ (\omega)$ in dBm	$P_{\text{out}}\ (2\omega)$ in dBm
[25]	−76.67	−191.05	−62.81	−168.24
MLP	−70.45	−159.91	−81.35	−187.46
KBNN	−75.44	−189.20	−60.97	−165.29
PKI	−76.67	−190.31	−57.41	−160.22

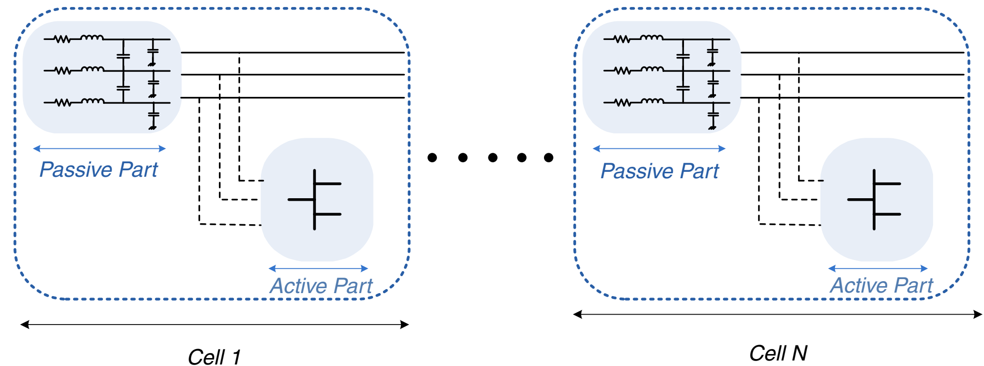

Fig. 16 Distributed representation of a FET as three active transmission lines

quasi-TEM mode can be considered to obtain the generalized active multi conductor transmission line equation. This equation can be used to describe the instantaneous voltage and current relationships in the transistor. So the purpose will be to find an equivalent circuit for this line and derive the transistor equations.

An equivalent circuit of a section of the transistor is shown in Fig. 17. Each segment is represented by a 6-port equivalent circuit which combines a conventional FET small-signal equivalent circuit model with another circuit element to account the coupled transmission line effect of the electrode structure where the all parameters are per unit length. By applying Kirchhoff's current laws to the left loop of the circuit in Fig. 17 and with $\Delta z \to 0$, we obtain the following three equations:

$$\frac{\partial I_d(z,t)}{\partial z} + C_{11}\frac{\partial V_d(z,t)}{\partial t} - C_{12}\frac{\partial V_g(z,t)}{\partial t} - C_{13}\frac{\partial V_s(z,t)}{\partial t} + g_m V'_g(z,t) + G_{ds}(V_d(z,t) - V_s(z,t)) = 0 \quad (8)$$

$$\frac{\partial I_g(z,t)}{\partial z} + C_{22}\frac{\partial V_g(z,t)}{\partial t} - C_{12}\frac{\partial V_d(z,t)}{\partial t} - C_{23}\frac{\partial V_s(z,t)}{\partial t} + C_{gs}\frac{\partial V'_g(z,t)}{\partial t} = 0 \quad (9)$$

$$\frac{\partial I_s(z,t)}{\partial z} + C_{33}\frac{\partial V_s(z,t)}{\partial t} - C_{23}\frac{\partial V_g(z,t)}{\partial t} - C_{13}\frac{\partial V_d(z,t)}{\partial t} - C_{gs}\frac{\partial V'_g(z,t)}{\partial t} - g_m V'_g(z,t) + G_{ds}(V_s(z,t) - V_d(z,t)) = 0. \quad (10)$$

Also, the gate-source loop leads to another equation which could be written as

$$V'_g(z,t) + V(z,t) + R_i C_{gs}\frac{\partial V'_g(z,t)}{\partial t} - V_g(z,t) = 0. \quad (11)$$

where
$C_{11} = C_{dp} + C_{ds} + C_{dsp} + C_{dg} + C_{dgp}$, $C_{22} = C_{gp} + C_{gsp} + C_{dg} + C_{dgp}$, $C_{33} = C_{sp} + C_{ds} + C_{dsp} + C_{gsp}$, $C_{12} = C_{dg} + C_{dgp}$, $C_{13} = C_{ds} + C_{dsp}$, $C_{23} = C_{gsp}$.

Similarly, applying the Kirchhoff's voltage law to the main node of the circuit and in the limit as $\Delta z \to 0$ in Fig. 17 gives:

$$\frac{\partial V_d(z,t)}{\partial z} + R_d I_d(z,t) + L_d\frac{\partial V_d(z,t)}{\partial t} + M_{dg}\frac{\partial V_g(z,t)}{\partial t} + M_{ds}\frac{\partial V_s(z,t)}{\partial t} = 0 \quad (12)$$

$$\frac{\partial V_g(z,t)}{\partial z} + R_g I_g(z,t) + L_g\frac{\partial V_g(z,t)}{\partial t} + M_{dg}\frac{\partial V_d(z,t)}{\partial t} + M_{gs}\frac{\partial V_s(z,t)}{\partial t} = 0 \quad (13)$$

$$\frac{\partial V_s(z,t)}{\partial z} + R_s I_s(z,t) + L_s\frac{\partial V_s(z,t)}{\partial t} + M_{ds}\frac{\partial V_d(z,t)}{\partial t} + M_{gs}\frac{\partial V_g(z,t)}{\partial t} = 0. \quad (14)$$

The above equations could be simplified in two matrix equations as follows:

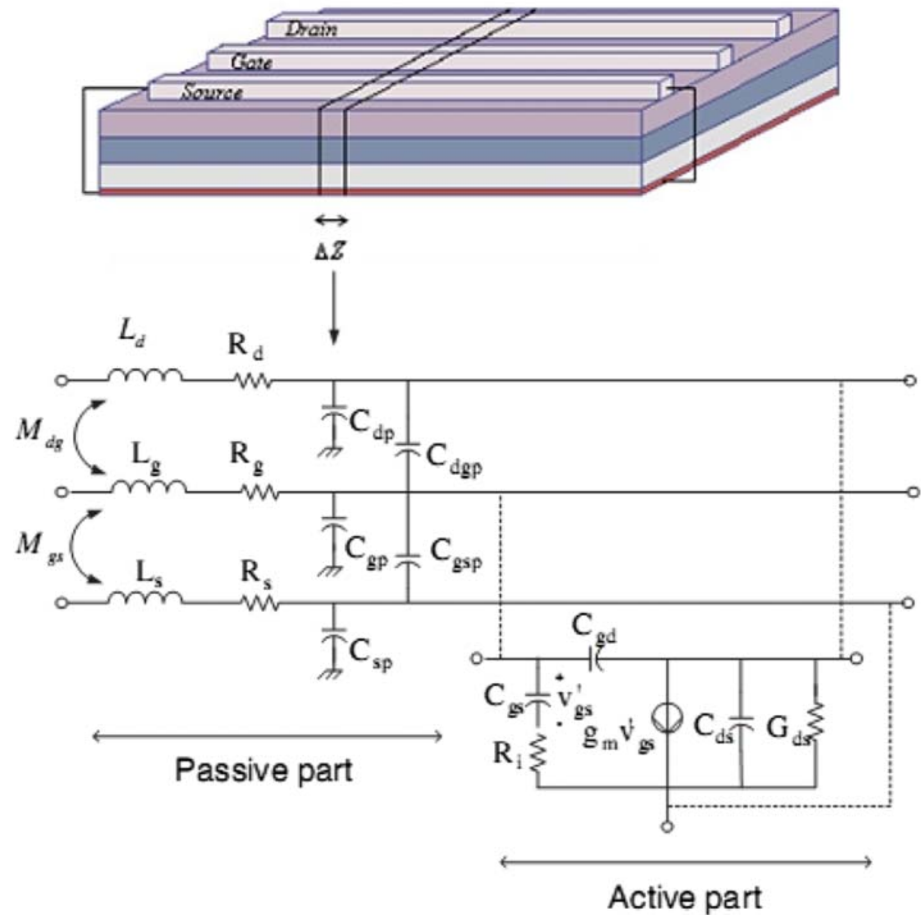

Fig. 17 An equivalent circuit model of a differential length of a FET

$$
\begin{aligned}
&\frac{\partial}{\partial z}\begin{pmatrix} I_d(z,t) \\ I_g(z,t) \\ I_s(z,t) \\ 0 \end{pmatrix}
+ \frac{\partial}{\partial t}\begin{pmatrix} C_{11} & -C_{12} & -C_{13} & 0 \\ -C_{12} & C_{22} & -C_{23} & C_{gs} \\ -C_{13} & -C_{23} & C_{33} & -C_{gs} \\ 0 & 0 & 0 & R_i C_{gs} \end{pmatrix}\begin{pmatrix} V_d(z,t) \\ V_g(z,t) \\ V_s(z,t) \\ V'(z,t)_g \end{pmatrix} \\
&+ \begin{pmatrix} G_{ds} & 0 & -G_{ds} & g_m \\ 0 & 0 & 0 & 0 \\ -G_{ds} & 0 & G_{ds} & -g_m \\ 0 & -1 & 1 & 1 \end{pmatrix}\begin{pmatrix} V_d(z,t) \\ V_g(z,t) \\ V_s(z,t) \\ V'_g(z,t) \end{pmatrix} = 0
\end{aligned} \tag{15}
$$

$$
\begin{aligned}
&\frac{\partial}{\partial z}\begin{pmatrix} V_d(z,t) \\ V_g(z,t) \\ V_s(z,t) \end{pmatrix}
+ \frac{\partial}{\partial t}\begin{pmatrix} L_{dd} & M_{gd} & M_{ds} \\ M_{gd} & L_{gg} & M_{gs} \\ M_{ds} & M_{gs} & L_{ss} \end{pmatrix}\begin{pmatrix} I_d(z,t) \\ I_g(z,t) \\ I_s(z,t) \end{pmatrix} \\
&+ \begin{pmatrix} R_d & 0 & 0 \\ 0 & R_g & 0 \\ 0 & 0 & R_s \end{pmatrix}\begin{pmatrix} I_d(z,t) \\ I_g(z,t) \\ I_s(z,t) \end{pmatrix} = 0.
\end{aligned} \tag{16}
$$

Here, V_d, V_g, V_s are the drain, gate and source voltages, respectively, while I_d, I_g, I_s are the drain, gate and source currents, respectively. These variables are functions of the position z along the device width and time. Therefore, the time-domain current–voltage relationships shown in (15) and (16) were solved using the FDTD. A Fast Fourier Transform (FFT) can be performed to obtain the corresponding S-parameters in order to compare them with the given measured/simulated input data and/or with those obtained by our fuzzy-neural frequency-domain approach described above.

7 Time-domain transistor modeling: example

The two frequency- and time-domain proposed methods were used to characterize the MESFET *NE71000* [37] from 1 to 40 GHz.

As reported in Fig. 18 and based on the fuzzy-neural approach, topology #2 was found to be the most suitable equivalent circuit for the given set of measured S-parameters. However, some discrepancies can be shown at the higher part of the frequency spectrum (between 35 and

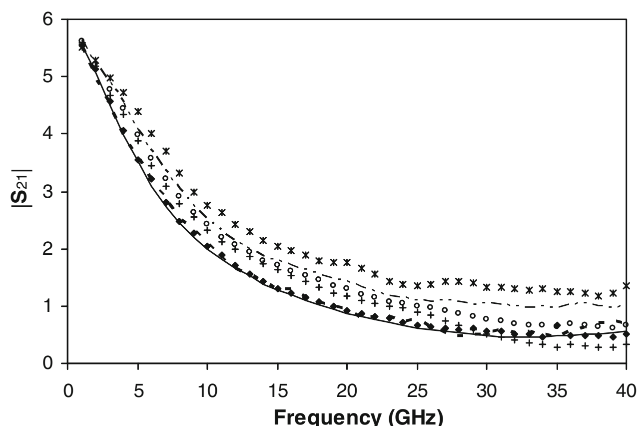

Fig. 18 NE 71000: comparison of measured S_{21} parameter (◆) with those obtained by the fuzzy-neural model using: +, standard topology; - - -, topology #2; o, topology #3; – - - –, topology #4; *, topology #5 and by the distributed model (—) after extraction and Fourier transform. The selected bias point was $V_{ds} = 3$ V and $I_{ds} = 10$ mA

40 GHz). In this range and as expected, the S-parameter values obtained by the time-domain approach agreed better with measured data than those obtained by the fuzzy-neural method.

To further investigate this issue, we plotted in Fig. 19 the S_{11} and S_{22} parameters of the transistor. As for the small-signal gain (S_{21}) of the transistor, the two methods fitted well with the measurements while in the frequency range 35–40 GHz, the distributed model is closer to the input data than the fuzzy-neural model.

The obtained distributed element values (per unit length) of the time-domain model are grouped into two tables: Table 4 for the passive sub-network and Table 5 for the active sub-network.

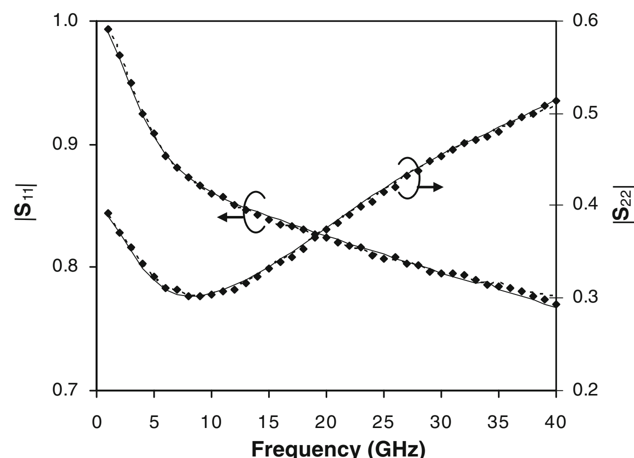

Fig. 19 NE 71000: comparison of measured S_{11} and S_{22} parameters (◆) with those obtained by the fuzzy-neural model using topology #2 (- - -) and by the distributed model (—) after extraction and Fourier transform. The selected bias point was $V_{ds} = 3$ V and $I_{ds} = 10$ mA

Table 4 NE71000. Passive part: distributed element values

Nomenclature (per unit length)	Values
L_d (nH/m)	780
L_s (nH/m)	780
L_g (nH/m)	161
M_{gd} (nH/m)	360
M_{gs} (nH/m)	360
M_{ds} (nH/m)	240
R_d (Ω/m)	900
R_s (Ω/m)	900
R_g (kΩ/m)	34.3
C_{gp} (pf/m)	0.6
C_{dp} (pf/m)	87
C_{sp} (pf/m)	148
C_{gdp} (pf/m)	29
C_{gsp} (pf/m)	29
C_{dsp} (pf/m)	61

Table 5 NE71000. Active part: distributed element values

Nomenclature (per unit length)	Values
C_{gs} (nf/m)	0.771
C_{ds} (nf/m)	0.0178
C_{gd} (nf/m)	0.1178
g_m (S/m)	146.42
R_i (Ω/m)	0.002
G_{ds} (mS/m)	15.46

8 Conclusion

In this paper, two advanced CAD tools have been presented for efficient characterization of high-frequency FETs and HBTs. The first combines fuzzy and neural techniques to obtain the most suitable electrical equivalent circuit of a given transistor while the second one is based on a distributed circuit model. Such approaches will be shortly extended to include nonlinear as well as thermal transistor behaviors at the component level, and highly nonlinear circuits at the circuit level.

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