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A Novel Single-Phase AC-AC Converter for Circuit Breaker Testing Application

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***Abstract*—This paper presents a novel single-phase ac-ac converter with power factor correction and output current control for circuit-breaker testing according to the IEC 60898 standard. The important advantages of the proposed circuit are low component count and fast responses for the standard requirement, especially a current step at the beginning of the test. The proposed single-phase ac-ac converter can operate in either buck or boost mode to accommodate the need for a wide range of output current while satisfying the ramping and step current requirements in the standard. The control circuits consist of two parts, dc voltage control of dc-link capacitors and ac output current controls operating simultaneously. The proposed circuit is verified through both computer simulation and hardware experiment. An example of a 50A circuit breaker testing according to the IEC 60898 is demonstrated in the paper.**

***Index Terms*—power factor correction (PFC), single-phase ac-ac converter, buck-boost capability, continuous current mode (CCM), current control, circuit- breaker.**

I. Introduction

A CIRCUIT-BREAKER (CB) is indispensable equipment in residential, commercial and industrial systems. It is designed to protect an electrical circuit from damage caused by overload or short circuit. The capability of interrupting the flow of the current to protect devices enables its utilization in virtually every applications. The time tripping characteristics of the CB and the test procedures detailed in IEC 60898 [1] are necessary in the process of quality control. Commercially available current sources for CB testing are designed using a motor-driven tap-changing auto-transformer for ac output current regulation. Recently, several ac-ac converters have been developed and improved in terms of higher current rating capability and higher efficiency. Also, they have included the power factor correction (PFC) to regulate the input current to be sinusoidal wave shaping with nearly unity power factor. In practice, the ac-ac converters are widely applied to various industrial applications such as UPS, voltage stabilizer, electric welding, and etc [4]-[5].

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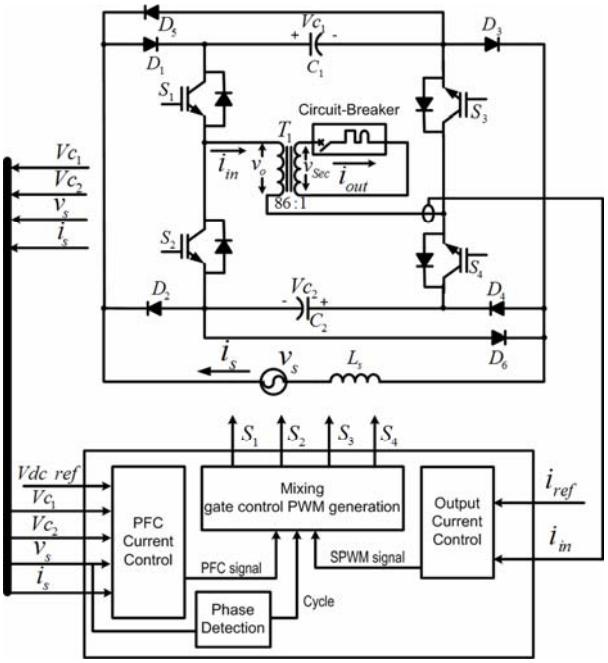

Fig. 1. Proposed ac-ac converter with dc-link voltage and ac output current controllers.

Several topologies of single-phase ac-ac converter had been reported. The single-phase ac-ac two-leg, three-leg and four-leg (two full-bridges) converters have been presents [4]-[7]. They are widely adopted choices of converters in UPS, motor drive or grid-connected applications [4]-[5]. These topologies consist mainly of two stages; a controlled rectifier (e.g., boost PFC topology) and a single-phase inverter. They can be operated in either buck or boost mode for the desired level of ac output voltage. The output frequency is controllable and can be set to the values different from the input frequency. The three-leg and two-leg single-phase ac-ac converters are operated in hard switching scheme, producing the switching loss and electromagnetic interferences [5], [6]. In addition, the two-leg single-phase converter has high ripple voltage at the dc-link capacitors.

In a buck-type ac-ac converter reported in [8], the ac output voltage is controlled using the modified sinusoidal pulsed-width modulation (SPWM). This topology introduces a distortion on the ac output voltage at the zero-crossings. Also, the output voltage is limited to the values less than the input voltage due to its buck-type topology.

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TABLE I
TIME-CURRENT OPERATING CHARACTERISTICS

Test	Type	Test current	Limits of tripping or non tripping time	Results to be obtained
a	B, C, D	$1.13I_n$	$t \geq 1h$ ($I_n \leq 63$ A) $t \geq 2h$ ($I_n > 63$ A)	No Tripping
b	B, C, D	$1.45I_n$	$t < 1h$ ($I_n \leq 63$ A) $t < 2h$ ($I_n > 63$ A)	Tripping
c	B, C, D	$2.55I_n$	$1s<t<60s$ ($I_n \leq 32$A) $1s<t<120s$ ($I_n>32$A)	Tripping
d	B	$3I_n$	$t \geq 0.1$ s	No Tripping
	C	$5I_n$		
	D	$10I_n$		
e	B	$5I_n$	$t < 0.1$ s	Tripping
	C	$10I_n$		
	D	$20I_n$		

Resonant converter topologies have also been used in the ac-ac conversion applications [9], [10]. The resonant converter is suitable for applications with a fixed frequency where the output frequency cannot be significantly differed from this frequency. For instance, the 60 Hz signal is not achievable with the 50 Hz input signal.

In ac-ac z-source converters, the z-source network is primarily used to store energy and the output voltage is load dependent [10]-[11]. The output voltage is varied through the duty ratio created from a PWM signal.

The key requirements of ac-ac converter for circuit-breaker testing are a wide range of output voltage with low harmonic distortion and high input power factor. Therefore, it must be capable of operating in buck and boost modes with the required dynamics of step current and ramp rate specified in [1].

The single-phase ac-ac converter has been presented in the system application for CB testing [2] according to the CB testing standard (IEC 60898) in Table I. It used four switches to control input current and output current with the same ground. The first part integrates rectifier and boost converter to regulate the dc-link voltages and control the ac input current with sinusoidal waveform in phase with the ac input voltage. The output current control is based on half-bridge topology to drive the positive and negative pulses by means of *SPWM* technique to the output.

Recently, a novel single phase ac-ac converter has been presented [3] and it is also suitable for CB testing application because it supports all key requirements of CB testing standard. This converter operates similarly with converter in [2], but its difference is about the converter output separated ground instead of shared ground. The ac-ac converter application for CB testing does not require the ac current output sharing the same ground with ac input voltage. As a result, the novel ac-ac converter has been selected to implement the proposed system for CB testing application. In addition, the proposed system is realized by the digital implementation according to the CB testing standard (IEC 60898).

The novel ac-ac converter topology can be compared with the four-leg converters (two full-bridges) [7]. They are the same operation both input current control and output voltage control with separated ground between input and output sides.

TABLE II
A NUMBER OF COMPONENTS IN TWO CONVERTERS

Device	Four-leg	Novel
inductor	1	1
switch	8	4
DC-link Capacitor	1	2
diode	0	6

A number of components is counted and compared between novel converter and four-leg converter as shown in Table II.

The novel topology has the reduced number of switches from eight to only four switches. Although the number of diodes is increased but the cost of switches is much more expensive than one of diodes.

The CB testing under the over current test condition consists of five tests, a, b, c, d, and e where the test currents vary from 1.13 to 20 times of the nominal rated current of CB (I_n) as shown in Table I [1]. The first three tests (a, b, and c) require that the peak of the test current is gradually varied whereas a step change is required in the other tests. The time current characteristics for over current CB test provided in Table I are the requirements for various CB types (B, C and D). Note that the current characteristics of each test are determined by the initial condition specified in the standard. For instance, the initial condition for tests a, c, d, or e is cold, meaning that there is no previous loading of CB before testing. However, the initial condition of the test b is performed immediately after the end of test a.

This paper is organized as follows. Section II presents principles of proposed system such as circuit operation and control strategy. Section III presents the simulation results which are then compared with experimental results in section IV. Finally, section V concludes the proposed system.

II. PROPOSED SYSTEM

The proposed system is shown in Fig.1. The ac-ac converter topology consists of four main switches (S_1-S_4), two dc-link capacitors (C_1 and C_2), an inductor (L_s), diodes (D_1 - D_6), and a power transformer (T_1). In the system, the V_{C1}, V_{C2}, i_s and v_s are measured and fed back to the digital controller. The dc-link capacitor (C_1) is charged and V_{C1} is maintained constant during the positive cycle of v_s while the capacitor voltage V_{C2} is charged and maintained constant during the negative cycle. The input voltage is used as the reference signal for controlling the input current, i_s. The output current is regulated by the switches S_1 and S_3 during the positive pulse while the switches S_2 and S_4 operate during the negative pulse, using the sinusoidal PWM (*SPWM*) technique. The primary winding of the power transformer T_1, with a turn ratio of 86.3, is connected to the output of the dc-ac converter. The transformer's secondary winding is short-circuited through the CB during testing. The output current is amplified by an order

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of the T_1's turn ratio. The proposed topology yields power factor in the range of (0.97-0.99) under various output frequencies.

A. *Integrated Rectifier/Boost Converter*

The integrated rectifier and boost converter in the proposed system include three functions as follows.

a) Rectifying the input voltage into a dc voltage signal;
b) Boosting the dc voltage;
c) Shaping the ac input current to be sinusoidal waveform.

The switches S_1 and S_2 are operated during the positive half cycle of the input voltage v_s to boost the voltage of the dc-link capacitor C_1. The waveform of the input voltage v_s is used as a reference for shaping the inductor current (i_s). The aim is to force the input current i_s to be in phase with the input voltage for unity power factor. Meanwhile, the capacitor voltage, V_{C1}, is maintained to a constant value. Figs. 2 and 3 show the circuit configurations during the charging and discharging cycles of the inductor current i_s. During the positive cycle of the input voltage, the switches S_1 and S_2 are turned on and the inductor current i_s increases as shown in Fig. 2(a). To complete the boost cycle, the switch S_1 or S_2 is turned off, depending on the output pulses, and the inductor current i_s is decreased, as shown in Fig. 2(b). Similarly, the operations of charging and discharging inductor current during the negative half cycle of the input voltage are repeated through switches S_3 and S_4, as shown in Fig. 3.

B. *DC-AC converter*

The proposed dc-ac converter is described in this section. The switches S_1 and S_3 are turned on to drive positive pulses to the converter output from the dc-link voltage, V_{C1}, as shown in Fig. 4(a). Similarly, during the negative output pulse, the dc-link voltage V_{C2} is connected to the converter output by turning on the switches S_2 and S_4, as shown in Fig. 4(b). The output of the dc-ac converter is directly connected to the primary winding of the transformer T_1. The transformer's secondary winding is short-circuited through the CB under test. At this stage, the transformer leakage reactance and resistance form a low-pass filter path for the converter's output signal. With a proper selection of the switching frequency, a low distortion sinusoidal current at the transformer secondary can be obtained. The output voltage is given as,

$$v_o = \frac{m_a}{\sqrt{2}} \cdot V_{Ci} \tag{1}$$

where m_a is the amplitude modulation index and V_{Ci} is the dc-link capacitor voltage.

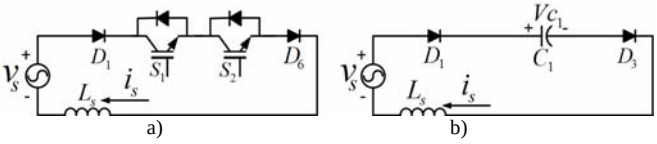

Fig. 2. Equivalent circuits of a) charging and b) discharging inductor current during positive cycle

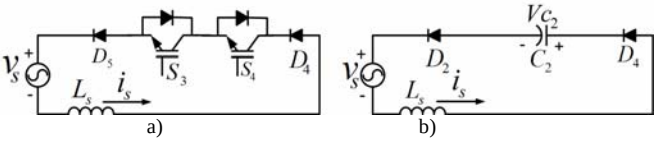

Fig. 3. Equivalent circuits of a) charging and b) discharging inductor current during negative cycle

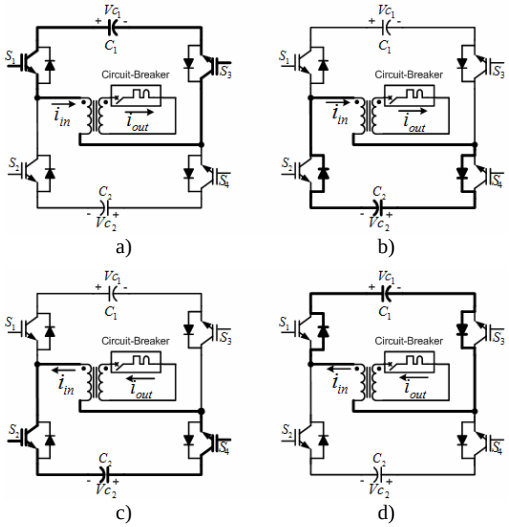

Fig. 4. Circuit configurations under a) positive and c) negative pulses of bipolar *SPWM* operation, b) and d) commutation current

C. *Power Transformer*

Since the current required for the CB testing is in the range of hundreds of amperes, a transformer is included in the proposed system. The addition of the transformer serves two purposes, a low-pass filter circuitry and a current amplification for the desired output current.

Taking the transformer's impedance into consideration, the cutoff frequency (f_c) of the low-pass filter circuit is given as

$$f_c = \frac{R_{eq}}{2\pi L_{eq}} \tag{2}$$

where X_{eq} and R_{eq} are the equivalent leakage reactance and resistance of the transformer, respectively. The important benefit of the current amplification capability enables the use of low current rating switching devices in the converter. Even though the converter supplies a bipolar *SPWM* signal to the transformer, the majority of the transformer's current is the line frequency component therefore, an iron core transformer is chosen. Note that during the CB testing, once the tripping mechanism is initiated, the current through the circuit breaker becomes zero indicating that the secondary of the transformer is open. However, there is a small amount of current supplying the transformer under no-load condition.

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The proposed system has been designed the turn ratio of 86 for power transformer, using as the current gain amplifier. The output current is controlled by feeding primary side current back into controller for current regulation.

D. Controller

The controls of the proposed system are divided into two parts. The first part is the ac input current control for PFC and the dc-link capacitor voltage control. The block diagram of the first part is shown in Fig.5. The reference signal is obtained from the input voltage for shaping the input current. Each dc-link capacitor voltage is measured and fed through a PI controller. The outputs of two PI controllers are toggling alternately with the cycle of input voltage. The absolute ac input voltage is multiplied by the output of multiplex block to generate a reference signal for the input current. Next, the error of the input current is sent to a PID controller. The output of the PID controller is then modulated with a triangular signal to generate a PWM signal for the PFC part.

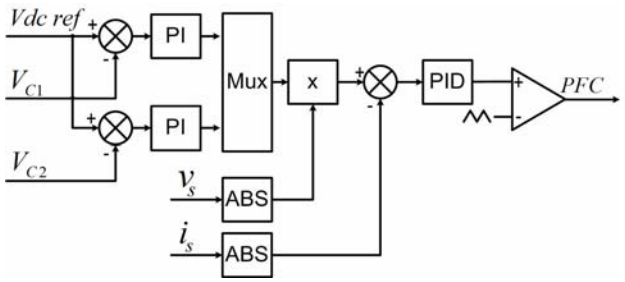

Fig. 5. Block diagram for PFC current control.

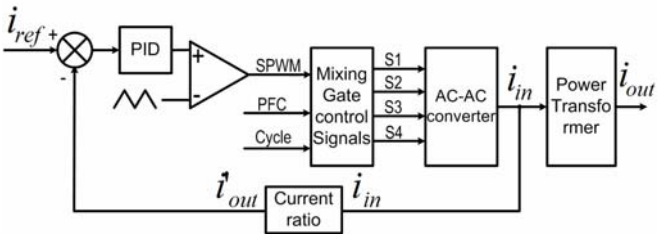

Fig. 6. Block diagram for output current control.

The second part is the output current control illustrated in Fig.6. The PID controller is used as a control signal to create PWM signals for the switches S_1, S_2, S_3 and S_4, in Fig. 1. The output of dc-ac converter is connected to the primary winding of the transformer T_1. Note that the current control is through the transformer's primary current. This means that the current transformation ratio must be known a priori to properly compensate for the secondary current control. In the mixing gate control signals block, there are two mixing controls, *SPWM* signals and *PFC* signal for ac input current control. The mixing of gate control signals can be logically expressed as follows,

$$S_1 = SPWM\,OR\,(PFC\,AND\,Cycle) \quad (3)$$

$$S_2 = \overline{SPWM}\,OR\,(PFC\,AND\,Cycle) \quad (4)$$

$$S_3 = SPWM\,OR\,(PFC\,AND\,\overline{Cycle}) \quad (5)$$

$$S_4 = \overline{SPWM}\,OR\,(PFC\,AND\,\overline{Cycle}) \quad (6)$$

where *SPWM* is a digital logic signal created by the SPWM switching scheme, *PFC* is a digital logic signal of the input current control and *Cycle* is a digital logic signal representing the positive cycle of the input voltage. The switches S_1 and S_3 deliver the positive pulse to the output when the *SPWM* logic status is high. On the other hand, the $\overline{SPWM}$ is active low to drive the switches S_2 and S_4 for negative pulse of the output signal. At the same time, the *PFC* logic and the cycle logic dictate the switching operation for the desired input power factor. When the *Cycle* signal is high, the switches S_1 and S_2 are employed to control the input current for the positive cycle of the input voltage. For the negative cycle of the input voltage, the $\overline{Cycle}$ is active low to enable the switches S_3 and S_4 for input current control.

III. Simulation Results

A computer simulation has been carried out to examine the performance of the proposed system. Simulation results confirm the validity of the control algorithms including, input current control, power factor correction, dc-link voltage control, and output current control. The parameters in the proposed system shown in Fig. 1 are summarized in Table III.

TABLE III
PARAMETERS IN THE PROPOSED SYSTEM

Parameters	Value	Parameters	Value
L_s	1.5mH	v_s	220Vrms/50Hz
C_1	6,000μF	i_{out}	0-600A/50, 60 Hz
C_2	6,000μF	V_{C1}	400V
f_s	20kHz	V_{C2}	400V

Fig. 7 shows the simulation results for steady-state response of the input current where the dc reference signal is set to 400 V. The input current, i_s, is sinusoidal and in phase with the input voltage. Fig. 8 shows the simulated steady-state behavior of the system with the reference set at 200 A(rms). Fig. 9 shows the simulation results for a step response of the output current from 100 to 200 A(rms). Once the output current is increased, the dc-link capacitor voltage decreases. The PFC controller increases the input current to regulate the dc-link capacitor voltage at the targeted value. Fig. 10 shows simulation results for steady-state response of the output current control at 60 Hz, 100 A(rms) which is differed from the input line frequency at 50 Hz. Next, the simulation results of the current controls according to CB test case (a) where the test current is ramped from zero to $1.13I_n$ and the test case (d) where the test current is stepped from zero to $3I_n$ are demonstrated. A type-B CB with the current rating at 50 A is used as a device under test and the simulation results for test cases (a) and (d) are given in Figs, 11 and 12, respectively. Note that the tripping mechanism of the CB is not shown in the simulation study.

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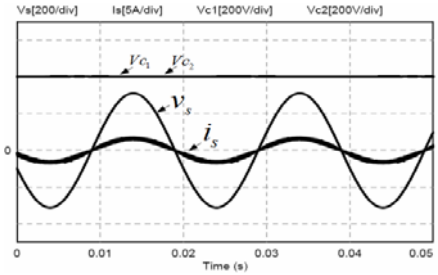

Fig. 7. DC-link voltage (V_{C1} and V_{C2}) at 400 V and ac input voltage (v_s) and current (i_s) waveforms.

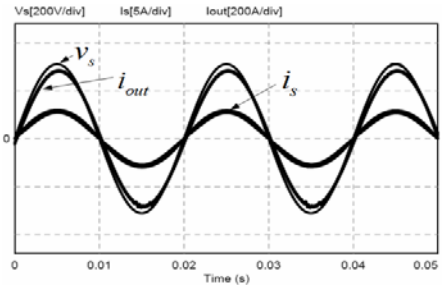

Fig. 8. Output current control at 200 Arms.

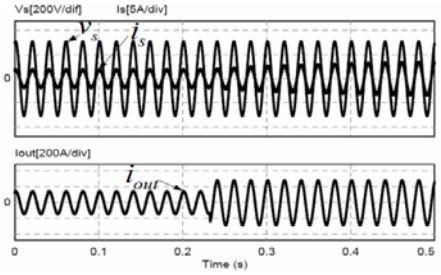

Fig. 9. Response to step change of ac output current from 100 to 200 Arms.

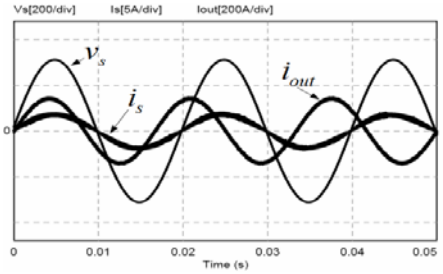

Fig. 10. Output current at 100 A(rms) with the frequency of 60 Hz.

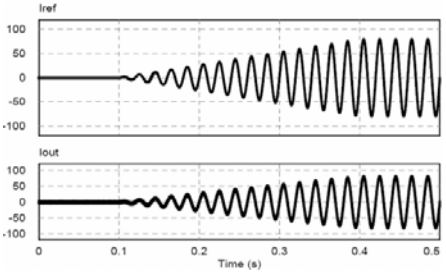

Fig. 11.Ramped current (0 to 56.5 Arms) for test case a).

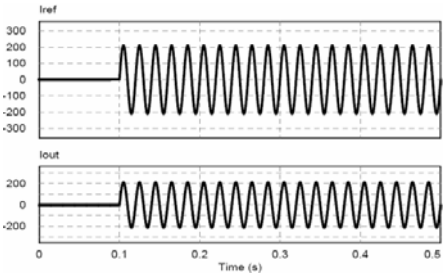

Fig. 12. Test current at 150 Arms for test case d).

IV. EXPERIMENTAL RESULTS

The laboratory prototype is constructed to verify the proposed system. The digital controller is designed by using a 32-bit fixed-point microcontroller (STM32F103VET6) for implementing all algorithms in the proposed system. The parameters in the real system implementation are the same as ones used in simulations, previously seen in Table III. The dc-link voltage reference is set to 400 V(dc). The switching frequency (f_s) of the PWM signals for regulating the ac input current and ac output current is 20 kHz. The dead time of leg switches is set to 1μs. The hardware is designed for 0-600 A(rms) output with 220V, 50/60Hz input voltage. The dual-pack IGBT module is rated 1200V/50A and specification of four diodes is 1200V/30A. The laboratory prototype of the proposed system is shown in Fig. 13.

The proposed system used the iron core transformer T_1. It has specification show in table IV. The average turn ratio and total current harmonic distortion (THD_i) of T_1 shows in table V. It is utilized as low pass filter without additional inductors. The equivalent circuit under test CB of power transformer T_1 is illustrated in Fig. 14.

The category of CB has one-pole, two-pole, three-pole and four-pole. These CB types can be tested in time-current operating characteristics from standard test by using series contact connected as shown in Fig.14. The tripping of these CB types may cause tripping due to any pole which causes to pull the other poles to trip CB.

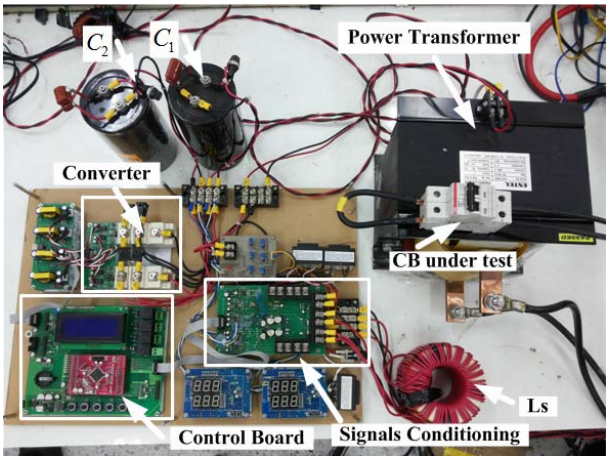

Fig. 13. Laboratory prototype proposed system.

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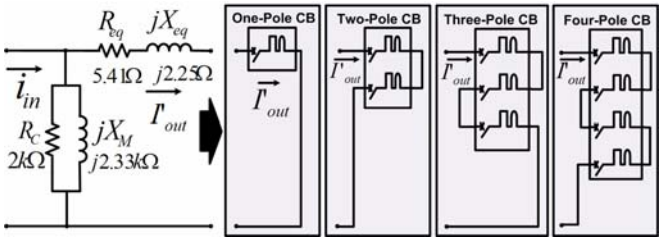

Fig. 14. Equivalent circuit of power transformer T_1 and series contact connecting technique.

The category of CB has one-pole, two-pole, three-pole and four-pole. These CB types can be tested in time-current operating characteristics from standard test by using series contact connected as shown in Fig.14. The tripping of these CB types may cause tripping due to any pole which causes to pull the other poles to trip CB.

TABLE IV
SPECIFICATIONS OF POWER TRANSFORMER

Parameters	Value
Phase	Single phase
Frequency	50 Hz
Maximum KVA	2.4 KVA
Vpri/Vsec	380/4.42 V(rms)
Ipri/Isec	6.98/600 I(rms)
Turn ratio	86

TABLE V
CURRENT RATIO OF POWER TRANSFORMER (T_1) AND THD OF AC OUTPUT CURRENT

i_{in}^{rms} (A)	i_{out}^{rms} (A)	i_{out}/i_{in}	(%THD i_{out})
0.5	43.1	86.2	1.3
1.0	86.2	86.2	1.2
1.5	129.4	86.3	1.1
2.0	173.2	86.6	1.1
2.5	216.0	86.4	0.9
3.0	259.0	86.3	0.9
3.5	303.0	86.6	0.9
4.0	346.0	86.5	0.9
Average i_{out}/i_{in}		86.38	

The ac current control used current feedback i_{in} flowing in the primary side of T_1. On the other hand, the ac current output i_{out} in the secondary side of T_1 is calculated by using the average turn ratio given in Table V. The winding impedances represented by R_C and X_M in the primary winding of T_1 represents the core-loss resistance and magnetizing reactance. The R_{eq} and X_{eq} represent the combined resistances and leakage reactance of both primary and secondary windings. In fact, the T_1 is acted as the low pass filter, having the transfer function as follow.

$$\left|H(j\omega)\right| = \frac{1}{\sqrt{1+(\omega L/R)^2}} \tag{7}$$

The cut-off frequency of low pass filter is thus derived as

$$f_{cut-off} = \frac{R_{eq}}{2\pi L_{eq}} \tag{8}$$

Substituting the parameters of T_1, yields $f_{cut-off}$ =120 Hz.

Fig. 15 shows the experiment results of steady-state response of dc-link voltages according to the same conditions presented in simulation result in Fig. 7. The integrated rectifier/boost converter and dual dc-link voltage/PFC control performance is successfully implemented. The ac input current is sinusoidal in phase with ac input voltage. Fig. 16 shows the experimental results for steady-state response of ac output current controlled at 200 A(rms). Similar to simulation result shown in Fig. 8, the ac output current is synchronously controlled with ac input voltage. In addition, the step response of ac output current from 100 to 200 A(rms) is successfully tested and shown in Fig. 17. The ramping-up response of higher ac output current from 0 to 300 A(rms) is tested and shown in Fig.18. And the step response of high ac output current from 0 to 400 A(rms) is given in Fig. 19. Both tests show the capability of high current control in the proposed system.

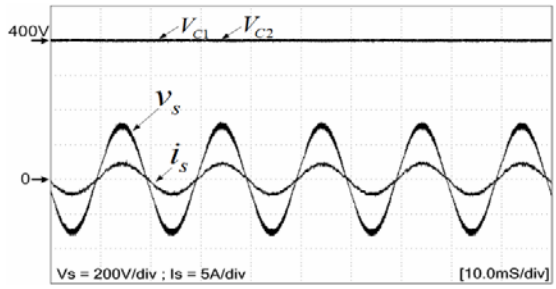

Fig. 15. DC-link voltage (V_{C1} and V_{C2}) at 400 V and ac input voltage (v_s) and current (i_s) waveforms.

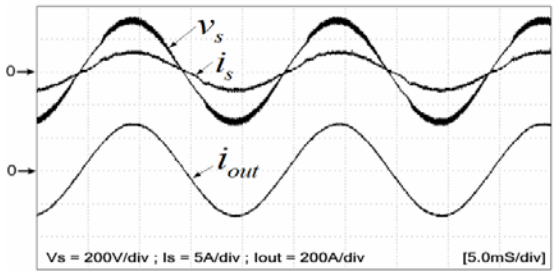

Fig. 16. Output current control at 200 Arms.

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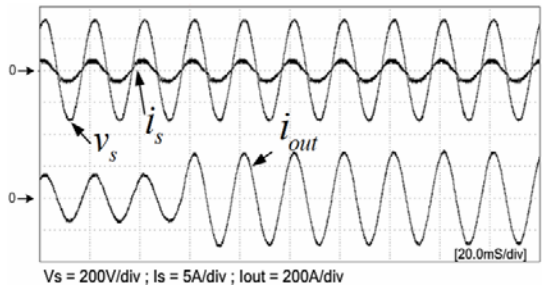

Fig. 17. Response to step change of ac output current from 100 to 200 Arms.

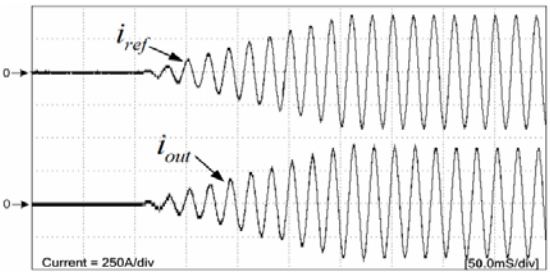

Fig. 18.Ramped current from 0 to 300 Arms.

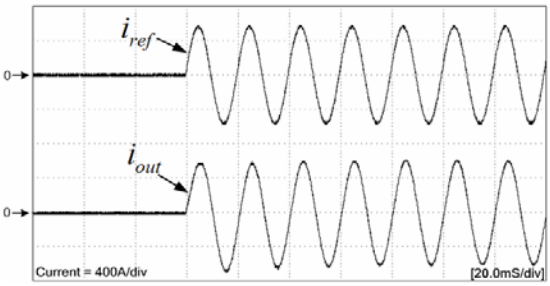

Fig. 19. Step response of the output current at 400 Arms.

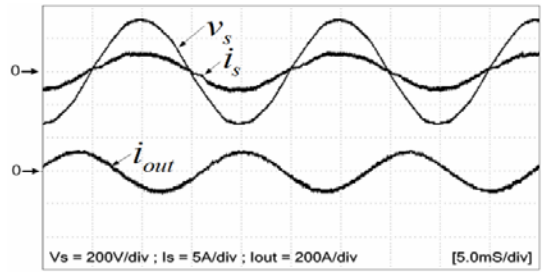

Fig. 20. Output current at 100 A(rms) with the frequency of 60 Hz.

Fig. 20 shows the ac output current controlled at 100 A(rms) and 60 Hz while the input frequency is 50 Hz. This result shows the possibility for the CB testing at 60 Hz. Next, Figs. 21 through 25 show the experimental results for the current control according to CB test a (with $1.13I_n$), b (with $1.45I_n$), c (with $2.55I_n$), d (with $3I_n$) and e (with $5I_n$), respectively.

All these figures, the reference signal i_{ref}, the primary side transformer current i_{in} and the secondary side transformer current i_{out} are shown. A miniature CB with 50 A(rms), two-pole and type B is chosen for testing. With its rating, the testing currents are set to 56.5, 72.5, 127.5, 150 and 250 A(rms) according to the time-current operating characteristics in Table I. The tests a, b and c require the ramping current control at the beginning while the tests d and e require the step current control. The primary side transformer current i_{in} is measured and fedback to the digital controller because the cheaper current sensor can be used. Then, the secondary side current i_{out} is calculated by multiplying the average turn ratio of 86.38 with i_{in} and regulated. The test a is firstly performed by ramping current from 0 to rated current of 56.5 A(rms) within 200 ms as shown in Fig. 21. After the test a has been conducted for 1 hour, the sample CB is not still tripped. Then, the test b is immediately started by ramping current from 56.5 A(rms) into 72.5 A(rms) within 200 ms. Fig. 22 shows the steady-state response of currents at this time. With continuing the test b, the sample CB is tripping at the time of 42 minutes. In this case, this particular sample CB passes the tests a and b. Before initiating the test c, the sample CB must be ensured that it is in cold condition. The test c is started by ramping current from 0 to 127.5 A(rms) within 200 ms as shown in Fig. 23. The experimental result of this test showed that the sample CB is tripping at 17.6 s. With this result, the sample CB passes the test c because it was tripped within 120s for I_n>32A. Similar to the test c, the test d is started in cold condition. However, the current control is in step mode. This test sets the rated current to be controlled at 150 A(rms) as shown in Fig. 24. The short circuit voltage of primary side is 122 V(rms). During testing, the sample CB is tripped at 7.8 s. In Table I, the test d must not be tripped within 0.1s and the tripping time should be more than 0.1 s. As a result, the sample CB passes in this test again. Lastly, the test e is performed. This test also starts with cold condition and step current control as shown in Fig. 25. This test employs a high testing current of 250 A(rms) (short circuit voltage is 203V(rms)), compared with the rating of CB. Thus, it causes very short tripping time of CB. In the test e, the tripping time is 6.8 ms which passes the requirement. In this Fig. 25, after CB is tripped, the current i_{out} is gradually to be 0 A(rms) while the current i_{in} appeared small one at the steady-state. The testing currents and tripping time for each test are summarized in Table VI.

When the tripping mechanism of the CB is initiated, the current flowing through CB becomes zero, resulting in an open-circuit in the secondary winding of the transformer. During this time, the power transformer is under no-load condition, i.e., i_{out} = 0. While the transformer is supplied by the output voltage, v_o, there exists a non-zero excitation current flowing to its primary winding. Fig. 26 shows the transformer's currents and voltages on both sides while the CB is tripped. The output current is set to 150 A(rms). The voltage on the secondary winding of the transformer is noted as v_{Sec}. Note that there is voltage across the CB due to the contact resistance before it is tripped. After the CB is tripped, the

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current error signal becomes large and the output of the PID controller is saturated. At this moment, the output voltage of the converter is similar a square wave signal illustrated in Fig. 26, and can be used as an indicator for the CB tripping time.

TABLE VI
TEST RESULTS OF SAMPLE CB 50A TYPE B

Test	Testing current(Arms)	Tripping time
a	56.5	No tripping for 1 hour
b	72.5	42 minutes
c	127.5	17.6 seconds
d	150.0	7.8 seconds
e	250.0	6.8m seconds

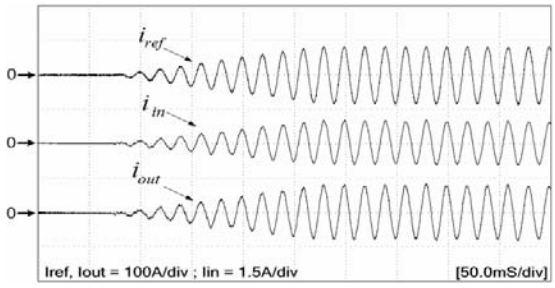

Fig. 21.Ramped current from 0 to 56.5 Arms for test case a).

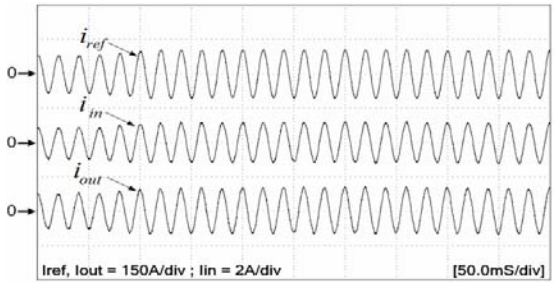

Fig. 22. Test current (ramped from 56.5 to 72.5 Arms) for test case b).

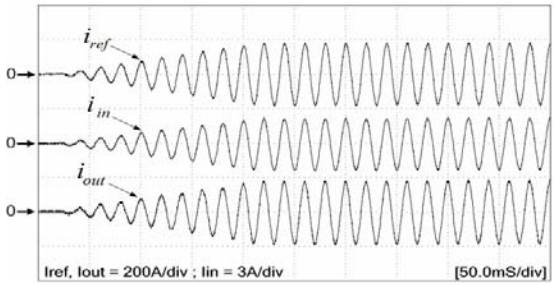

Fig. 23. Test current (ramped from 0 to 127.5 Arms) for test case c).

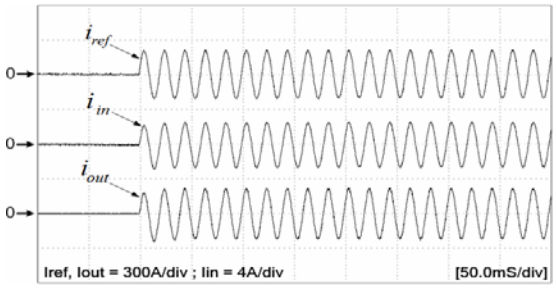

Fig. 24. Test current at 150 Arms for test case d).

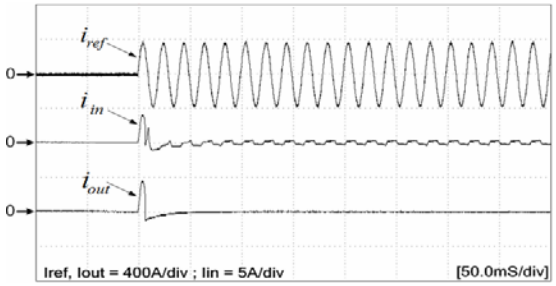

Fig. 25. Test current at 250 Arms for test case e).

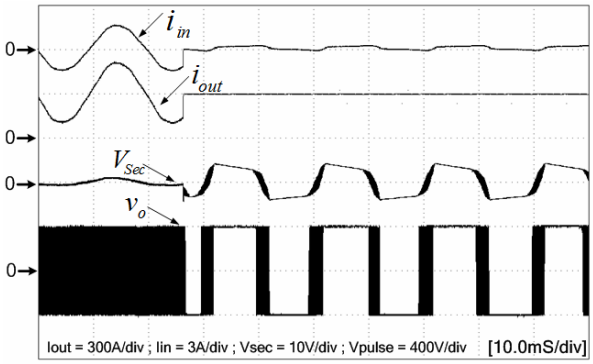

Fig. 26. Currents and voltages during CB tripping.

V. CONCLUSIONS

In this paper, the novel single-phase ac-ac converter with ac output current controls is proposed and digitally implemented according to the circuit-breaker (CB) testing standard (IEC 60898). Both simulation and experimental results show the improved transient step current control performance over the traditional ac current source based on the motor driven tap changing of auto-transformer. The proposed system is simple and low cost with minimum number of switches employed. The boost PFC topology with dual dc-link voltage controls is also incorporated in the proposed system. A laboratory prototype rated 600A(rms) output was constructed to verify the proposed system. According to results, the proposed topology accomplishes the sinusoidal input line current with unity power factor and low THD_i of output current. The satisfactory transient step responses of output current are obtained.

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