Fully Integrated AND and OR Optical Logic Gates

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***Abstract*— We propose two novel designs of compact, linear, and all-optical OR and AND logic gates based on photonic crystal architecture. The proposed devices are formed by the combination of the ring cavities and Y-shape line defect coupler placed between two waveguides. The performance of the proposed logic gates has been analyzed and investigated using finite difference time domain method. The suggested design for AND gate offers ON to OFF logic level contrast ratio of not less than 6 dB and the suggested design for OR gate offers transmitted power of not less than 0.5. On top of that, the proposed OR and AND logic gates can operate at bit rates of around 0.5 and 0.208 Tb/s, respectively. Further, the calculated fabrication tolerances of the suggested devices show that the rods radii of the ring cavities need to be controlled with no more than ±10% and ±3% fabrication errors for optical OR and AND gates, respectively. It is expected that such designs have the potential to be key components for future photonic integrated circuits due to their simplicity and small size.**

***Index Terms*— Photonic crystals, logic gates, FDTD.**

I. Introduction

TO DATE, optical computers are attractive for future broadband optical communication systems since they have some advantages such as high speed, high throughputs and low power consumption. In order to build the optical computer, all-optical flexible signal processing devices are needed [1]. Optical logic gates are considered as key elements in real time optical processing and communication systems which perform the necessary functions at the nodes of network such as data encoding and decoding, pattern matching, recognition and various switching operations [2].

Recently, different schemes have been demonstrated to realize various all-optical logic gates such as quantum dots [3], semiconductor optical amplifiers (SOAs) [4], multimode interference in S_iG_e/S_i [5] and nonlinear SOI waveguide [6]. In spite of the enormous technological progress, most of these works suffer from certain limitations such as big size, difficult to perform chip scale integration, high power consumption, low speed and the spontaneous emission noise. On top of that, photonic crystal (PhC), a type of artificial periodic dielectric structures, are designed to construct compact high speed logic gates with dimensions of a few wavelengths of light being confined [7]. They have many applications as coupler [8] drop filters [9], logic gates [10], optical routers [11], image encryption system [12] and dense chip-scale photonic integrated circuits [13] due to their unique properties.

The scope of this letter is to propose and simulate two compact novel designs for AND and OR logic gates based on 2D PhC platform. Each structure proposed for the realization of OR or AND logic gates is composed of two line defects, ring cavities and Y-branch waveguide. Here, the procedure for designing complete structure is based on designing and optimizing its half first. The physical dimensions of the half of the structures are appropriately optimized with the purpose of transmitting a signal with optimized peak or optimized null from input waveguide to output waveguide. Next, two arms of the optimized half structure are merged in order to perform complete logic gates. To evaluate the performance of the suggested designs, ON to OFF logic level contrast ratio, the transmission and the response period have been calculated. All calculations in this letter were performed using improved complex envelope alternative direction implicit finite difference time domain method [14]. The suggested design for AND gate offers ON to OFF logic level contrast ratio of around 6 dB and the suggested design for OR gate offers transmitted power of not less than 0.5. On top of that, the proposed OR and AND logic gates can operate at bit rates of around 0.5 Tbits/s and 0.208 Tbits/s, respectively. As small as 13 μm in device length, being simple stems from total avoidance of nonlinear optics and ease of integration is quiet evident since, the input ports are straight PhC waveguide arms rendering easy coupling to input output circuits. It is expected that such designs have the potential to play an important role in the future of high speed optical communication systems based on photonic integrated circuits.

This letter is organized as follows. Following this introduction the description of used PhC platform is presented. Next, the suggested designs and the simulation results for the optical OR and AND gates have been introduced in sections III, IV, V and VI, respectively. Finally, the main conclusion of our study is presented in section VII.

II. Photonic Crystal Platform

The proposed 2D PhC platform shown in Fig. 1 consists of an array of size of 49×40 of silicon rods arranged on triangular lattice. The refractive index and the diameter of the silicon rod and the lattice constant are chosen to equal 3.59, 0.2 μm and 0.54, respectively. The PBG calculations depend on illuminating the 2D PhC structure with a

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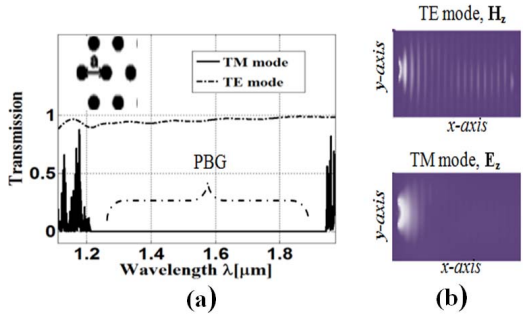

Fig. 1. PhC Structure: (a) Transmission spectra. (b) Field profiles.

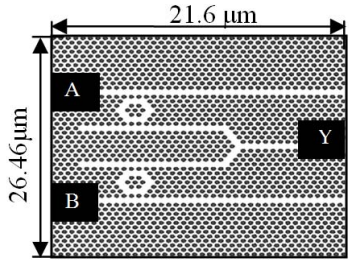

Fig. 2. The proposed optical OR gate structure.

Gaussian pulse from a homogeneous medium and investigating the propagation spectra around the 2D PhC structure [11]. Figure 1(a) shows the transmission spectra around the 2D PhC structure, for TM and TE polarization modes. This figure reveals that, the considered PhC platform has incomplete PBG which only exist over TM polarization mode and extending from 1.2165 μm to 1.9409 μm. In addition, Fig. 1(b) shows the steady state field profiles along the propagation *xy* plane at the $\lambda = 1.5$ μm for the TM and TE modes, respectively. The displayed field distributions clearly agree with the behavior of the transmission spectra where the light cannot pass for TM mode while the light can pass for TE mode through the PhC structure. To keep such PBG effect in the considered wavelength range of interest using 3D PhC structure, the height of the PhC rods should be carefully selected. As indicated by [8], the optimum rod height should be around half a wavelength relative to an averaged index that depends on the polarization.

III. Proposed OR Logic Gate

Figure 2 shows the schematic diagram of the proposed OR logic gate using the 2D PhC platform shown in Fig. 1(a). The proposed OR gate is formed by two line defects, two ring cavities and Y-branch waveguide. In Fig. 2, the input signals are coming from the left ports of the upper and lower waveguides called "A" and "B" respectively. Output signal is obtained from the right port of the middle waveguide called "Y". It is expected that the usage of ring cavity permits a signal with single peak to go from input port to output port. Our proposal is based on optimizing only the geometrical parameters of the upper half of the structure shown in Fig. 2 in order to achieve maximum transmission.

Next, simulating the complete design shown in Fig. 2 to mimic the truth table behavior of OR logic gate shown in Table I. It can be observed from the table that the output is logically "1" if any of the input values is one. As indicated from the Table I, the transmission of the logically "1" is defined by 0.5 or more.

TABLE I
TRUTH TABLE FOR OR LOGIC GATE

A	B	Logic output	Transmission$T=\lvert E_o/E_{in}\rvert^2$
0	0	0	0
0	1	1	≥ 0.5
1	0	1	≥ 0.5
1	1	1	≥ 0.5

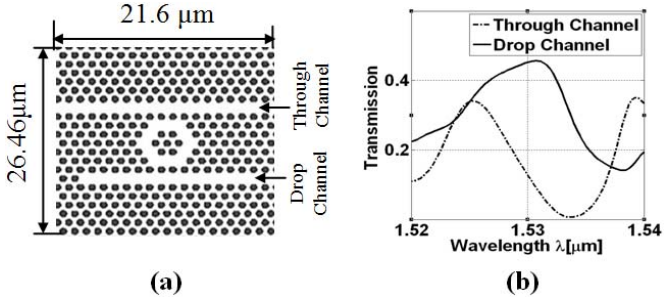

Fig. 3. Simulation of ring cavity: (a) Structure. (b) Transmission.

IV. Results and Discussion for OR Gate

To verify the proposition in the previous section, we use 2D FDTD simulator [14] to investigate and optimize the performance of the ring cavity and the Y-branch waveguide. Firstly, the spectral response of the proposed ring cavity is investigated as shown in Fig. 3. In Fig. 3(a), the input signal is coming from the left port of the upper waveguide called "Through channel". Output signal is obtained from the right port of the lower waveguide called "Drop channel". Figure 3(b) shows the transmittance with respect to the wavelength for TM mode. It can be found from the figure that one peak with about 40% of the input power will be transmitted to the drop channel. The value of the dropped power can be controlled and optimized by bending the drop channel and taking the output depending on different vertical length ζ as shown in Fig. 4. Figure 4(d) shows the calculated dropped power of the structures shown in Fig. 4(a)–(c) with ζ ranges from 3a to 6a. It can be observed from this figure that, the dropped power increases with the decrease of ζ and reaches its maximum value at ζ of *3a*.

Two arms of the optimized structure shown in Fig. 4(a) are merged in order to perform compact optical OR gate at the wavelength 1.529 μm as shown in Fig. 2. Figure 5(a) shows the steady state field profiles at 1.529 μm for the proposed OR gate for the last three cases shown in Table I. On top of that, Fig. 5(b) shows the spectral transmission of the proposed OR gate for TM like polarization of incident light from single input port and both input ports. The figures show that, when the signal at 1.529 μm is launched at port A, while the signal B is off it leads to the forward-dropping (logic 1) at the output port Y where the transmission reads 0.5. The same procedure happens when signal B is on, while the signal A is off.

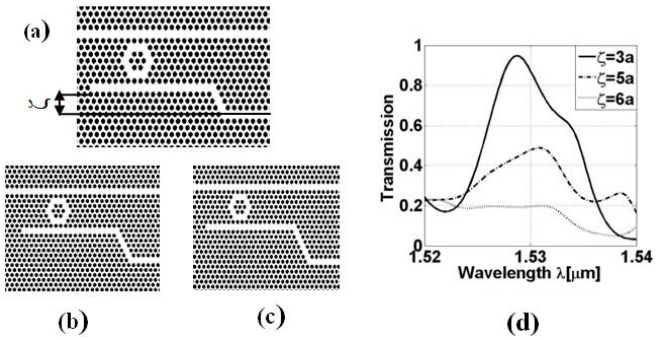

Fig. 4. Bend with different ζ, (a) ζ = 3a, (b) ζ = 5a, (c) ζ = 6a. (d) Transmission.

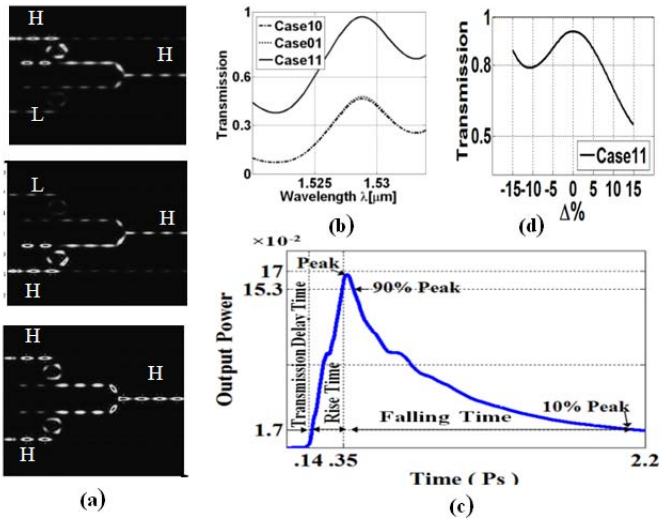

Fig. 5. Results of the proposed OR gate: (a) steady state field distribution, (b) transmission spectrum, (c) time evolving curve of the output power, (d) fabrication tolerance.

Moreover, the excitation of the two input ports by two identical input signals results into the forward-dropping (logic 1); the transmission reads 0.95. The bit rate (BR) of the proposed OR gate has been determined using the time evolving curve of the output power similar to [10]. Figure 5(c) shows that, the time of the output power consists of three parts; one of which is time due to transmission delay i.e. 0.14 ps and the other is the time for the power to climb from 0.1% peak to 90% peak is found to be 0.21 ps and the falling time from peak to 10% peak is approximately equal to 1.65 ps. Hence, the response period of the output power is equal to 2 ps and the proposed OR gate can operate at a BR of 0.5 Tbits/s. The tolerance with respect to the fabrication error has been evaluated. We have intentionally added $\pm\Delta\%$ tolerances in the central rods radii of ring cavities. As indicated in Fig. 5(d), the calculated fabrication tolerance of the suggested device found that the rods radii need to be controlled with no more than $\pm$10% fabrication error.

V. Proposed and Logic Gate

Figure 6 shows the schematic diagram of the proposed AND logic gate using the PhC platform shown in Fig. 1. The proposed AND gate is formed by two line defects, four ring cavities and Y-branch waveguide. In Fig. 6, the input

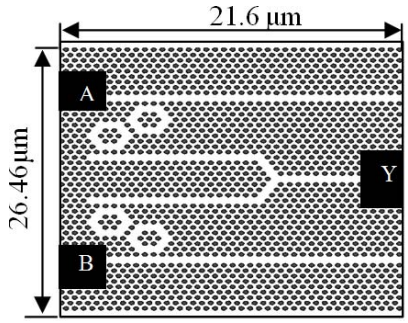

Fig. 6. The proposed optical AND gate structure.

TABLE II
Truth Table for AND Logic Gate

A	B	Logic output	$T=\lvert E_o/E_{in}\rvert^2$	Contrast ratio ≈6dB
0	0	0	0	
0	1	0	≤ 0.4	
1	0	0	≤ 0.4	
1	1	1	≥ 0.8	

signals are coming from the left ports of the upper and lower waveguides called "A" and "B" respectively. Output signal is obtained from the right port of the middle waveguide called "Y". By the same criteria, the upper half of the AND structure will be optimized to control the magnitude of the transmittance. It is expected that using two ring cavities will results in dropping signal with multiple peaks and multiple nulls. Hence, the position and the magnitude of the null can be controlled through optimizing the geometrical parameters of the ring cavities and the Y-branch line defect to mimic the truth table behavior of AND logic gate shown in Table II. It can be observed from the table that the output is logically "1" if only both of the input values are one.

VI. Results and Discussion for and Gate

Firstly, the spectral response of the proposed two coupled ring cavities is investigated using the 2D FDTD simulator as shown in Fig. 7. As shown in the Fig. 7(a), the input signal is coming from the left port of the upper waveguide called "Through channel". Output signal is obtained from the right port of the lower waveguide called "Drop channel". Figure 7(b) shows the transmittance with respect to the wavelength for TM mode. It can be found from the figure that the effect of two cavities results in transmission of multiple peaks and multiple nulls. The position of the null and its power magnitude can be controlled and optimized by bending the drop channel and taking the output depending on different vertical length ζ as shown in Fig. 8(a)–(c). Figure 8(d) shows the calculated dropped power for the structure shown in Fig. 8 with ζ ranges from 3a to 6a. The figure shows that, the positions of the nulls move to the left as well as its transmission value increases with the increase of ζ.

Compact optical AND gate can be obtained at wavelength 1.538 μm by merging two copies of the optimized structure shown in Fig. 8(a) as shown in Fig. 6. Figure 9(a) shows the steady state field distributions at 1.538 μm for the proposed AND gate for the last three cases shown in Table II. On top

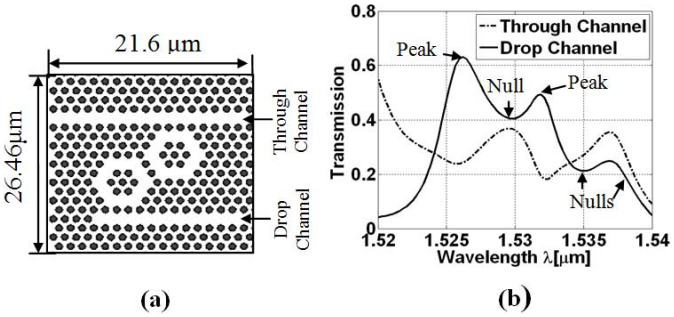

Fig. 7. Simulation of PhC resonator: (a) Structure. (b) Transmission.

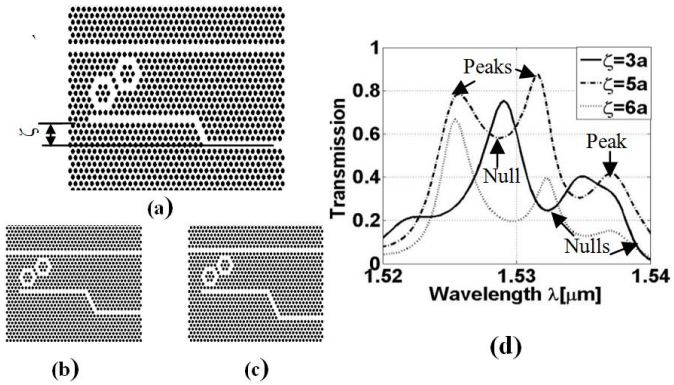

Fig. 8. Bend with different ζ, (a) $\zeta = 3a$, (b) $\zeta = 5a$, (c) $\zeta = 6a$. (d) Transmission spectrum.

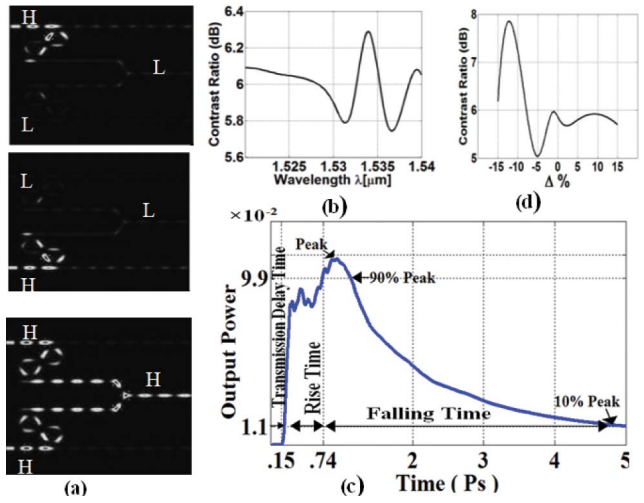

Fig. 9. Results of the proposed AND gate: (a) steady state field distribution, (b) contrast ratios, (c) time evolving curve of the output power, (d) fabrication tolerance.

of that, Fig. 9(b) shows the calculated contrast ratio of the proposed AND gate. The figures show that, when the signal at 1.538 μm is launched at port A, while the signal B is off it leads to the reverse-dropping (logic 0) at the output port C where the transmittance reads 0.4. The same procedure happens when signal B is on while the signal A is off. Moreover, the excitation of both ports A and B by two identical input signals results into the forward-dropping (logic 1); the transmittance reads 0.8. From Fig. 9(c), it has been concluded that, the response period of the output power is equal to 4.8 ps and the proposed AND logic gate can operate at a bit rate of 0.208 Tbits/s. The tolerance with respect to the error of fabrication has been evaluated. We have intentionally added $\pm\Delta\%$ tolerance in the central rods radii of ring cavities. As indicated in Fig. 9(d), that the optimized central rod radii of ring cavities need to be controlled with not more than $\pm 3\%$ fabrication error.

VII. Conclusion

In this letter, two compact designs for optical AND and OR gates using photonic crystal platform are proposed. The proposed devices are formed by the combination of the ring cavities and Y-shape line defect coupler placed between two waveguides. The proposed logic gates have been analyzed and numerically simulated using FDTD method. The suggested design for AND gate offers ON to OFF logic level contrast ratio of not less than 6dB and the suggested design for OR gate offers transmitted power of not less than 0.5. Moreover, the proposed OR and AND logic gates can operate at bit rates of around 0.5 Tbits/s and 0.208 Tbits/s, respectively. On top of that, we have also shown the fabrication tolerances of the suggested gates and found that the central rod radii of ring cavities need to be controlled with no more than $\pm 10\%$ and $\pm 3\%$ fabrication errors for optical OR and AND gates, respectively.

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