Design of Broadband Bandpass Cascaded Single-Stage Distributed Amplifier in 0.13 μm CMOS Technology for UWB Applications

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***Abstract*—This paper presents a broadband bandpass amplifier in CMOS technology based on the cascaded single-stage distributed amplifier (CSSDA) technique. In this design, the conventional lowpass LC filter structure of the CMOS CSSDA is replaced by a bandpass LC filter structure lines. The CSSDA has a nearly constant gain, linear phase response, and acceptable return loss in the passband. Simulation results clearly indicate that the proposed circuit topology can be used as a broadband bandpass amplifier for UWB applications.**

I. INTRODUCTION

Broadband amplifiers are the vital building blocks of broadband wireline/wireless receivers and transmitters. They are used in many radio frequency and high-data rate communication systems including satellite transceivers, pulsed radar systems, optical receivers, etc[1]. Deep submicron CMOS technology provides the high-speed active devices along with on-chip passive components required for implementation of the broadband amplifiers. Submicron CMOS technology is a low-cost technology compared with other high-speed semiconductor technologies (GaAs, SiGe, InP, GaN, others) [2,3]. Cascaded single-stage distributed amplifiers (CSSDA) are ideal candidates for enhancing bandwidth because the input and output artificial transmission lines have high cut-off frequencies.

CSSDAs considered as a major technique for broadband amplification. With the increasing applications of Ultra Wideband (UWB) technology, there is a new need for the design of a low noise broadband amplifier to boost received signals to a detectable level for analog to digital converter to produce the corresponding digital signal. A block diagram of a UWB receiver is shown in Fig. 1

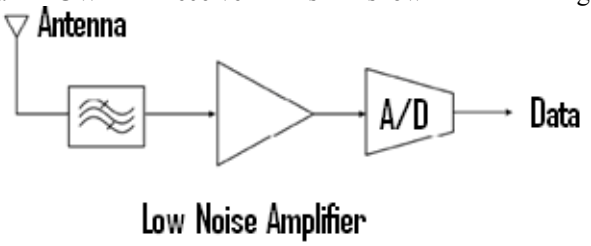

Fig. 1: A typical block diagram that is used in UWB receivers

The current UWB systems operate in the frequency band between 3 GHz and 10 GHz , and have a stringent limit on their signal power level as shown in Fig 2.[4]

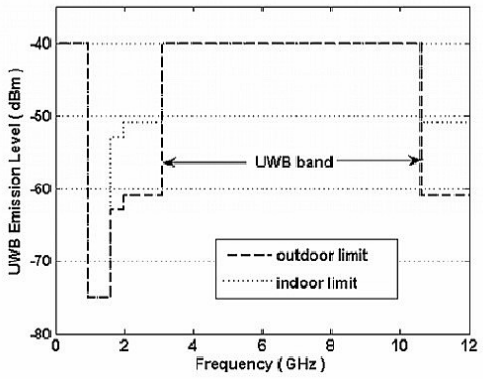

Fig. 2: FCC's UWB emission mask.

Therefore, the amplifier should reject the signal outside this frequency band to avoid interference from other wireless systems as well as to reduce the input noise as much as possible. In CMOS technology, since the interconnects with lengths up to 100 micrometers do not exhibit the transmission lines behavior at frequencies up to 30 GHz , the transmission

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lines are artificially constructed as a ladder network of inductors and capacitors.

In this topology, the inductors and capacitors are placed in the transmission lines as in the conventional lowpass LC filters [5]. Several successful implementations of CMOS CSSDAs are reported in the literature [6-10]. Design of the CSSDA is extensively discussed in microwave engineering texts [6-15].

In this paper, a novel bandpass CSSDA is designed based on a conventional lowpass CSSDA, where the lowpass transmission lines are replaced by bandpass LC transmission lines.

A CSSDA is presented in a standard 0.13 μm CMOS process. The organization of this paper is as follows. Section II describes the principle theory of CSSDA. The design of the proposed circuit is presented in Section III. The simulation results are shown in Section IV, and a conclusion is given in Section V.

II. THEORY OF CONVENTIONAL LOWPASS CSSDA

In this part, the CSSDA is designed as a conventional lowpass CSSDA. The schematic diagram of a conventional lowpass CSSDA is shown in Fig 3. The CSSDA topology shown in Fig 4 uses the simplified small-signal equivalent model of the CMOS. A signal generator connected at the input of this network will result in a voltage swing across the input gate capacitor C_{gs} at the first stage.

The signal is amplified via the CMOS's transconductance to produce a current flow at its drain port, which is terminated by the interstage impedance Z_{int}.

This current will in turn develop a voltage at the gate of the next stage to be amplified by the corresponding CMOS, producing a current at its drain port. Thus, the signal will be amplified by the gain of the successive stages.

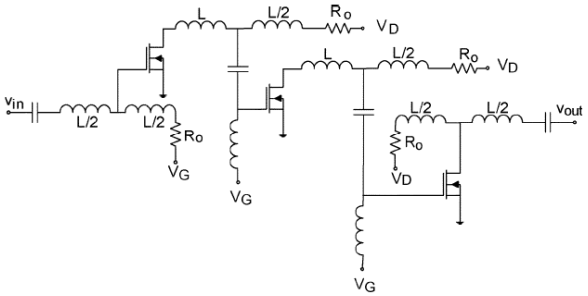

Fig. 3: Schematic diagram of a conventional lowpass CSSDA

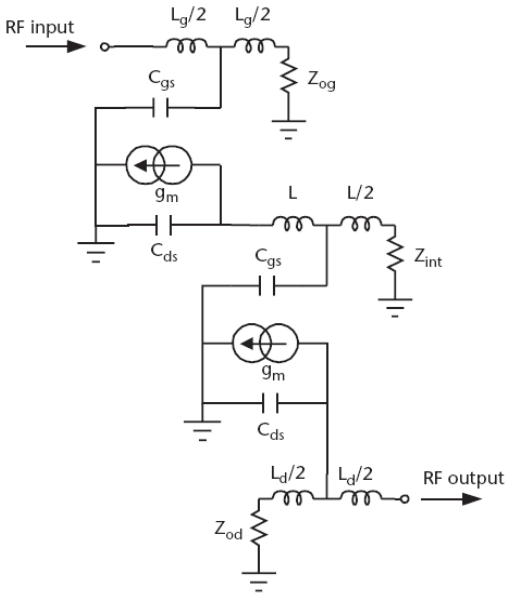

Fig. 4: Small-signal model of a general CMOS CSSDA amplifier

The available power gain of *n*-stage cascaded distributed amplifier is:[12,13]

$$G_{cssda} = g_m^{\,2n} Z_{\text{int}}^{2(n-1)} Z_{od} Z_{og} / 4 \qquad (1)$$

Where Z_{og} and Z_{od} are the characteristic impedances of the gate and drain lines respectively, g_m is the transconductance of the transistors.

III. DESIGN OF BANDPASS CSSDA

To convert the lowpass operation of the conventional circuit to that of a bandpass amplifier , it is first necessary to replace the lowpass filter topology with a conventional bandpass LC filter circuit for transmission lines. For a typical bandpass filter frequency response and corresponding bandpass LC filter circuit shown respectively in Fig 5a and 5b, the following simple relationships are derived.

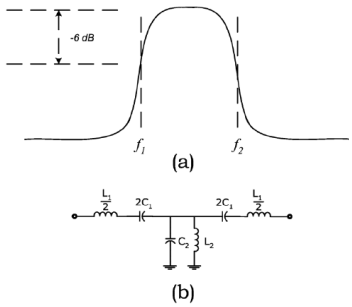

Fig. 5: a) Typical frequency response of bandpass LC filter, and b) its corresponding LC filter topology (singlestage)

The nominal characteristic impedance of the artificial transmission line is equal to[16,17]

$$Z_o = \sqrt{\frac{L_1}{C_2}} = \sqrt{\frac{L_2}{C_1}} \qquad (2)$$

The values of LC components are given by

$$L_1 = \frac{Z_o}{\pi(f_2 - f_1)} \qquad (3)$$

$$L_2 = \frac{(f_2 - f_1)Z_o}{4\pi(f_2 \times f_1)} \qquad (4)$$

$$C_1 = \frac{(f_2 - f_1)}{4\pi(f_2 \times f_1)Z_o} = \frac{L_2}{Z_o^{\,2}} \qquad (5)$$

$$C_2 = \frac{1}{\pi(f_2 \times f_1)Z_o} = \frac{L_1}{Z_o^{\,2}} \qquad (6)$$

Where:

f_1 and f_2 are the lower and upper cutoff frequencies of the bandpass LC filter as depicted in Fig.5(a), respectively. The above formulas are used for the design of the transmission lines of a bandpass CSSDA.

IV. SIMULATION RESULTS

The proposed broadband bandpass CSSDA is designed in 0.13 µm CMOS technology. The transistor sizes are selected for high g_m and high gain to meet the requirement of the UWB systems. The design is based on simplified models of the transistors and passive components to examine the functionality of the proposed circuit topology. The simulations are carried out using ADS software [18].

Fig.6 gives the schematic diagram of the proposed bandpass CSSDA amplifier and Fig. 7 shows the complete layout of the CSSDA.

The total layout area is 1.931mm by 1.046mm or $2.021\,mm^2$. In this figure the input RF pads are located at the left side of the layout and the output RF pads are at the right side.

Figs. 8 to 10. show the measured S-parameters from 0 to 14 GHz. Other simulation results are given in Figures 11 to 15.

V. CONCLUSION

A novel circuit topology for broadband bandpass CSSDAs is presented in this paper. Using a standard 0.13 µm CMOS process, a CSSDA is designed and simulated for demonstration. The design steps of the proposed amplifier are presented. Simulation results have shown that the proposed method for the design of broadband bandpass CMOS CSSDAs can be successfully used for UWB applications.

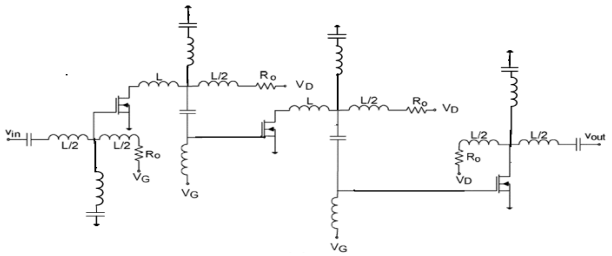

Fig. 6: Schematic diagram of the proposed bandpass CSSDA amplifier

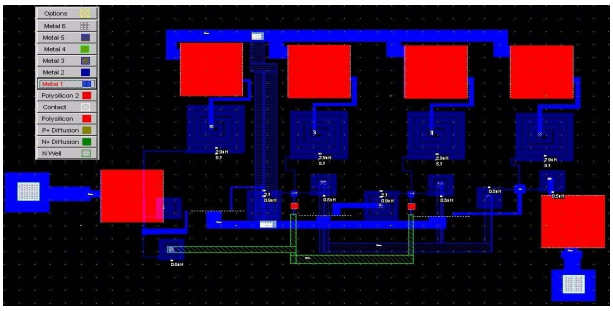

Fig.7: Layout of the proposed Broadband Bandpass CSSDA Amplifier. The RF input is on the left, the output on the right side. The layout area is $2.021\,mm^2$.

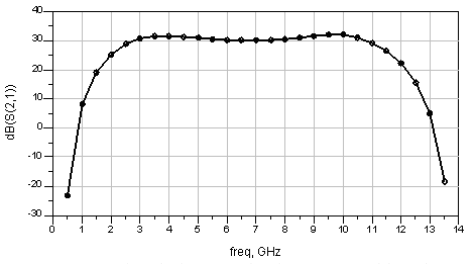

Fig. 8: S_{21} parameter simulation results for proposed bandpass CSSDA amplifier

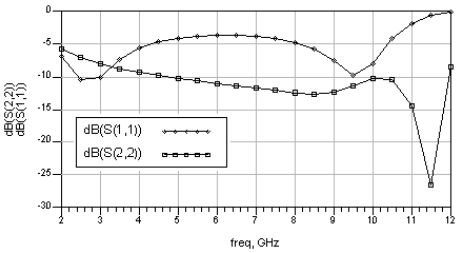

Fig. 9: Return loss simulation results for proposed bandpass CSSDA amplifier

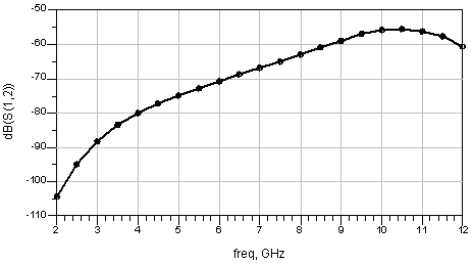

Fig. 10: S_{12} parameter simulation results for proposed bandpass CSSDA amplifier

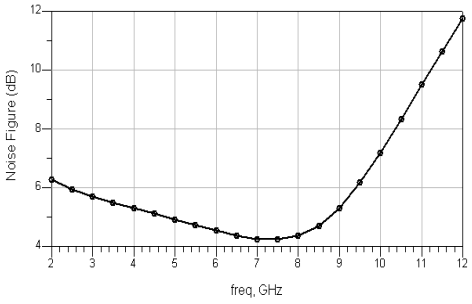

Fig.11: Simulated noise figure

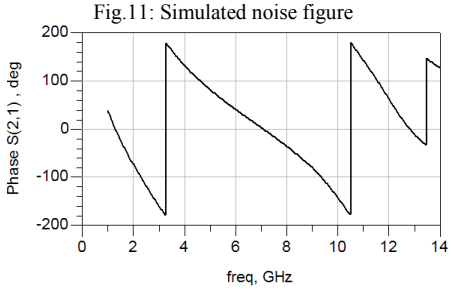

Fig .12: Simulated phase shift vs frequency

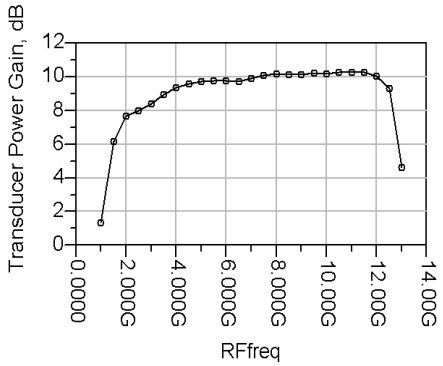

Fig.13: Simulated Transducer power gain vs frequency

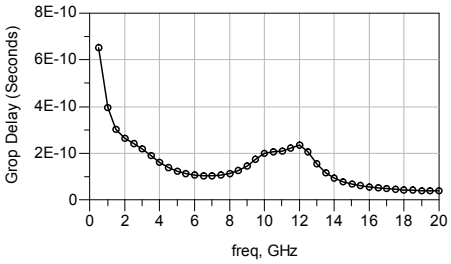

Fig.14: Simulated Group delay vs frequency

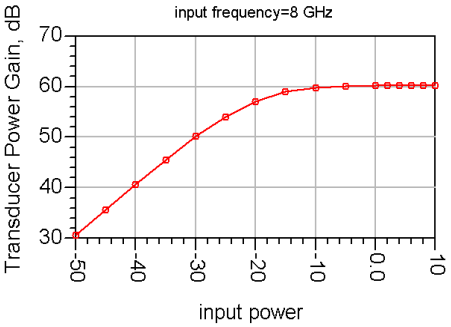

Fig.15: simulated Transducer power gain vs input power

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