Appl. Phys. A
DOI 10.1007/s00339-014-8935-9

Applied Physics A
Materials Science & Processing

Leakage current reduction in junctionless tunnel FET using a lightly doped source

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Received: 17 August 2014 / Accepted: 11 December 2014

Abstract In this paper, we explain the problem of dramatic OFF-state leakage in junctionless tunnel field effect transistor (JLTFET) for a channel thickness greater than 10 nm. In JLTFET, with channel width greater than 10 nm, the depletion region primarily remains confined below the dielectric–semiconductor interface. Hence, we tend to incur significant leakage through the center of the device. With the help of 2D device simulations, we demonstrate that the cause of the leakage current is predominantly due to thermal injection in the source region and is concentrated through the center of the device. We suggest a technique of using a lightly doped source region, below the p-gate to increase the barrier and prevent any leakage. The proposed alteration records an improved I_{ON}/I_{OFF} ratio for JLTFET for a channel of width 20 nm.

1 Introduction

Recently, tunnel FETs are being regarded as promising candidates for supply voltage scaling because of their remarkable subthreshold swing. Carrier transport in tunnel FET is determined by band-to-band tunneling, unlike carrier transport due to injection in MOSFET which limits the subthreshold swing to 60 mV/dec [1–3]. Therefore, tunnel FET offers steeper switching, which makes it an attractive candidate for low power applications. Use of narrow bandgap materials and vertical structures in the source side has led to further improvement in characteristics, compared to all silicon tunnel FET [4–17].

To make the fabrication process easier, a novel structure named junctionless tunnel FET (JLTEFT) has been reported which suggests the use of a secondary gate (p-gate) to form the source region [18–22]. The key advantage of the JLTFET structure is that there is no stringent requirement to control a precise and steep p-n junction. However, the ON-current is low compared to MOSFET in Si JLTFET, ranging from 10 μA/μm to 0.1 mA/μm. Recent studies have shown excellent performance of JLTFET with III–V materials [23–25]. In most of the JLTFET simulations, the use of a thin body of the order close to 5 nm has been reported. The dimensions of the device, as reported, confirms the scalable nature of the device. We try to explore the performance of silicon JLTFET device for a thicker body, close to 20 nm. The purpose of this investigation is to propose a feasible JLTFET configuration, which would be suitable for use in bulk applications like silicon-on-insulator (SOI) [26, 27] and FinFET [28] structure.

Leakage current due to thermal injection is observed in the source side, for a body thickness of 20 nm. This results in higher I_{OFF} in thicker body JLTFETs, which leads to significant OFF-state power dissipation. In this paper, we propose a structure of n-type silicon JLTFET with lightly doped source region and explain how it helps in significant reduction of leakage through the device. The improvement in the device performance in terms of I_{ON}/I_{OFF} ratio is discussed. We also propose that a laterally graded Gaussian doping profile is suitable, and the device does not require an abrupt doping junction.

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Published online: 18 December 2014

1.1 Device structure and simulation parameters

Figure 1. shows the structure of the proposed Si JLTFET. For a fair comparison, we have tried to keep the structure of the JLTFET identical to the structure published in [19, 23]. The control gate modulates the tunneling barrier for electrons tunneling from source to drain, similar to uniformly doped n-type Si JLTFET. A fixed gate also called the p-gate is used to deplete the region below it and raise the energy bands so that it acts similar to a p-type source [19]. To operate the device, the p-gate is grounded and a positive voltage of magnitude 1 V is applied to the drain. High-κ dielectric hafnium oxide ($\varepsilon = 25$) is used as a dielectric for the control gate and p-gate.

In our simulation study, we have neglected the formation of native oxide between the dielectric–semiconductor interface and considered a physical oxide thickness of 2 nm. The device is designed with both control gate (L_g) and p-gate (L_p) measuring 20 nm each. The separation between the two adjacent gates are kept 2 nm (t_{SP}), and high-κ dielectric HfO_2 ($\varepsilon = 25$) of physical thickness 2 nm is used as the insulator for both the gates. A uniform n-type doping of 10^{19} cm^{-3} is used in the drain region and for the region below the control gate. We have introduced a lightly doped source region below the p-gate with a doping concentration of 10^{15} cm^{-3}. The work function of the control gate and the p-gate were chosen to be 4.3 and 5.9 eV, respectively. We have used an abrupt n^+-n junction in the simulations to understand the physics of the device clearly. In the end, we have proposed a laterally graded JLTFET structure which is free from any abrupt p-n junction and adheres to the term junctionless.

All simulations were performed in Silvaco Atlas, version 5.16.3.R [29], using a nonlocal band-to-band tunneling model. The nonlocal band-to-band tunneling model takes into account the spatial variation of the energy bands without the assumption that the generation/recombination of opposite carrier types is spatially coincident. The Fermi–Dirac statistics and Shockley–Read–Hall (SRH) recombination model were included for the calculation of transport characteristics. The band gap narrowing model was also included assuming a highly doped channel. Direct gate tunneling was neglected, with the assumption of high-κ dielectric in the simulation. Presence of traps greatly influence the OFF-current in tunnel FET. In order to include the effect of traps, model for trap-assisted tunneling by Schenk [29, 30] was included in our simulation.

2 Results and discussions

The OFF-state band structure of a uniformly doped Si JLTFET with body thickness (t_B) of 20 nm (along $y = 0$)is shown in Fig. 2. We can clearly see that the band structure closely resembles the p-i-n configuration. In the OFF state, the energy width for tunneling (t_w) is much wider. This prevents band-to-band tunneling of electrons from the source side (valence band) to the region below the control gate (conduction band). As a positive gate voltage is applied, the tunneling barrier (t_w) gets narrowed and the energy range for tunneling is widened, allowing tunneling current to flow through the device. The above band structure is consistent with the JLTFET of 5 nm body width reported in the literature [19]. However, if we analyze the OFF band structure of a 20 nm JLTFET along the center of the body, we tend to find an abnormality. Figure 3 compares the band structure along x through the center of the device (cutline 2 in Fig. 2) for a body thickness of 5 and 20 nm, respectively. In case of the 5 nm (t_B) device, the OFF-state band structure is found to be as expected and no significant current flows through the device. However, for the 20 nm (t_B) device, we observe that the bands are not

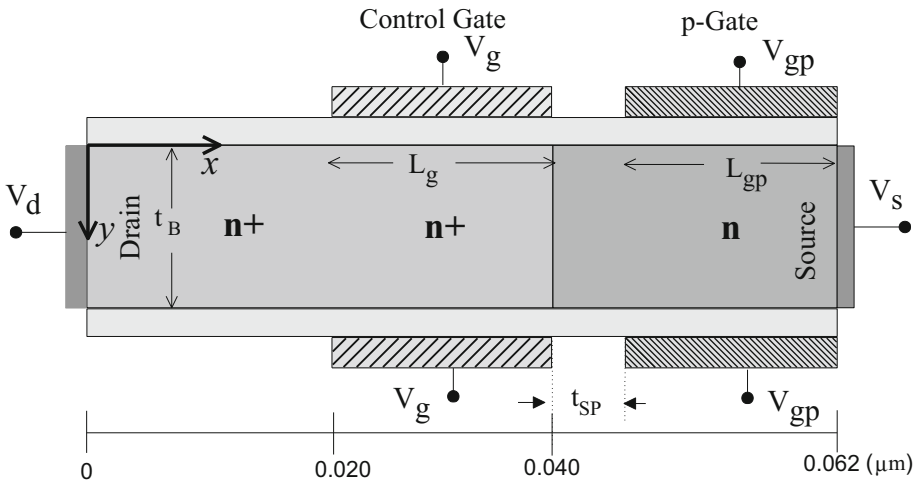


Fig. 1 Schematic of the proposed n-type Si JLTFET with lightly doped source

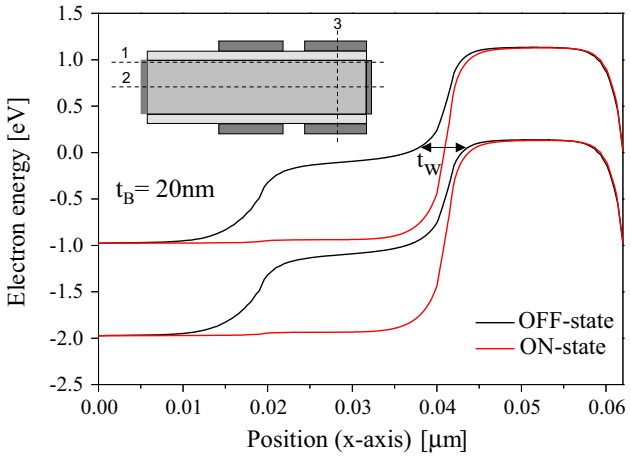


Fig. 2 OFF state and ON state band diagram of a uniformly doped JLTFET with body thickness of 20 nm (along x) and just below the dielectric (cutline 1).$V_d = 1$ V and $V_g = 0$ V for the OFF state and $V_d = 1$ V and $V_g = 1$ V for ON state. The *inset* of the figure shows the JLTFET with two cutline 1,2 along $y = 0$ and along the center of the device, respectively

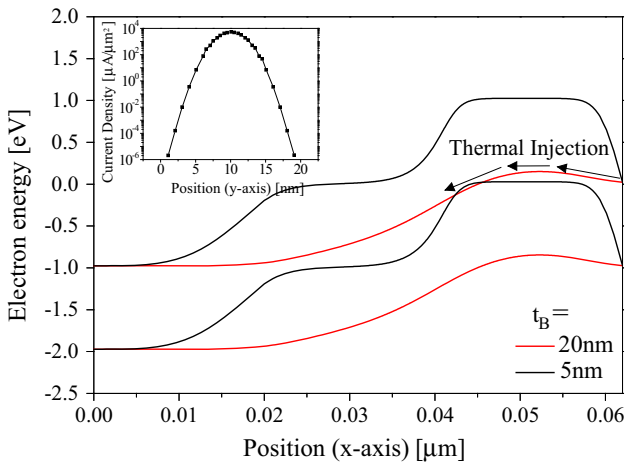


Fig. 3 OFF state ($V_d = 1$ V and $V_g = 0$ V) band diagram of a uniformly doped JLTFET with body thickness of 5 and 20 nm, respectively, parallel to x-axis through the center (cutline 2 [Fig. 2]) of the device body. *Inset*: current density through the body of the device in the source region parallel to y-axis (cutline 3 [Fig. 2])

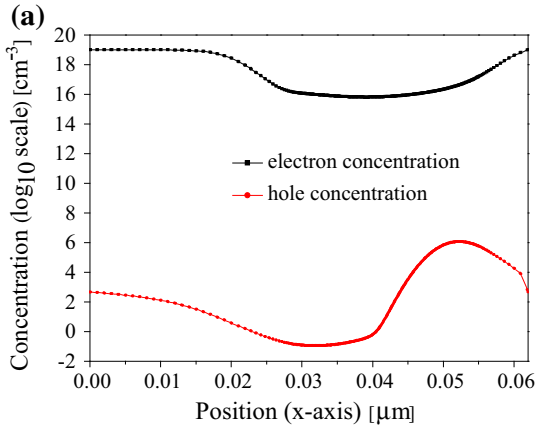
lifted as expected. For a JLTFET device with a thicker body, the depletion region is confined to the surface of the device and fails to extend to the center of the device. This inherent problem is due to the use of a highly doped (10^{19} cm^{-3}) channel region below the gates [31]. The inset of Fig. 3. shows the exponential nature of current density along the *y*-axis of device (for $t_B = 20$ nm). Therefore, the figure confirms the possibility of serious leakage through the center of the device which is maximum through the center of the device.

Since, the depletion region is not extended to the bulk of the device, the control of the gate on the bulk of the device is lost. The width of the energy barrier (t_w) is wider than 20 nm which is sufficiently large to prevent band-to-band tunneling. Therefore, it is clear from Fig. 3 that the OFF-state leakage is predominantly due to electrons from the source surmounting the barrier (classically) below the p-gate by the process of thermal injection.

The electron and hole concentration in a uniformly doped JLTFET of body thickness 20 nm is shown in Fig. 4a. It is clear from the figure that the electron concentration below the source is high (10^{16} cm^{-3}) which signifies that the device is not completely turned OFF, and there is significant current through the device. In order to behave like a p$^+$-i-n$^+$ tunnel FET, the electron concentration must be close to zero and the hole concentration must be as high as possible below the p-gate (source region) [17, 19]. We propose a structure where we use a lightly doped source (Fig. 1), in order to increase the depletion width below the gates. The electron and hole concentration of the JLTFET with lightly doped source is shown in Fig. 4b. Interestingly, with the use of lightly doped source, the depletion region is extended to the center of the device. Consequently, a substantial reduction in the electron concentration and increase in hole concentration is observed. The concentration profile seems analogous to a p$^+$-i-n$^+$ tunnel FET, and the leakage current in the OFF state is expected to reduce. Figure 5 compares the band structure (along cutline 2 [Fig. 2]) of the JLTFET with lightly doped source with a uniformly doped JLTFET. It is clearly evident that the barrier for carrier injection below the p-gate is raised which prohibits further leakage. Furthermore, the energy barrier width for tunneling (t_w) is greater than 10 nm which prevents significant leakage due to band-to-band tunneling.

Figure 6a and b shows the I_d–V_g characteristics of the uniformly doped JLTFET and the proposed JLTFET structure (with lightly doped source), respectively. From the Fig. 6a, it is observed that the OFF-current starts to degrade for a body thickness greater than 10 nm in a uniformly doped JLTFET. For a body thickness of 20 nm, the device encounters a serious leakage current of the order of 10 μA/μm. This is because the electron injection current dominates over the band-to-band tunneling current. We show in Fig. 6b that the leakage current due to thermal injection through the center of the device is completely reduced by using a doping of lower concentration in the source region. For the JLTFET with body thickness of 20 nm, the leakage current is found to reduce by ~8 orders of magnitude, which supports what we wanted to see from Fig. 5.

For a uniformly doped JLTFET, as we can see in Fig. 7, I_{OFF} increases exponentially with increase in body thickness (t_B) for $t_B > 10$ nm. This is because the probability of carrier injection is exponentially dependent on the barrier



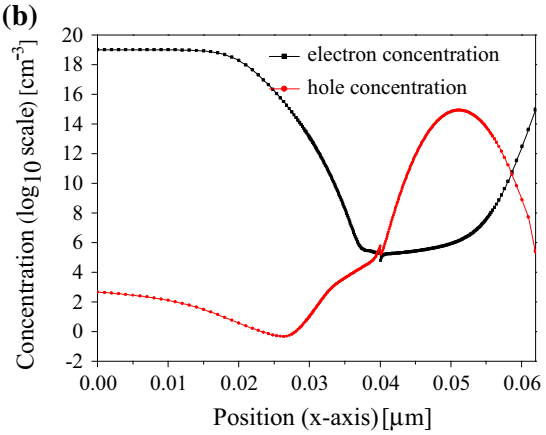


Fig. 4 **a** OFF state ($V_d = 1$ V and $V_g = 0$ V) electron and hole concentration of a uniformly doped JLTFET ($t_B = 20$ nm) along a cutline parallel to x-axis through the center of the device. **b** OFF state electron and hole concentration of a JLTFET ($t_B = 20$ nm) with lightly doped source [Fig. 1] along a cutline parallel to x-axis and passing through the center (cutline 2 [Fig. 2]) of the device

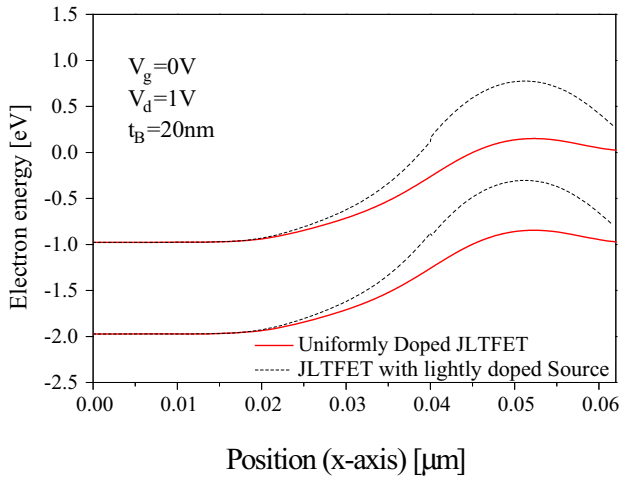


Fig. 5 OFF state ($V_d = 1$ V and $V_g = 0$ V) band diagram of a uniformly doped JLTFET and the JLTFET with lightly doped source for $t_B = 20$ nm, along a cutline parallel to x-axis through the center of the device (cutline 2 [Fig. 2])

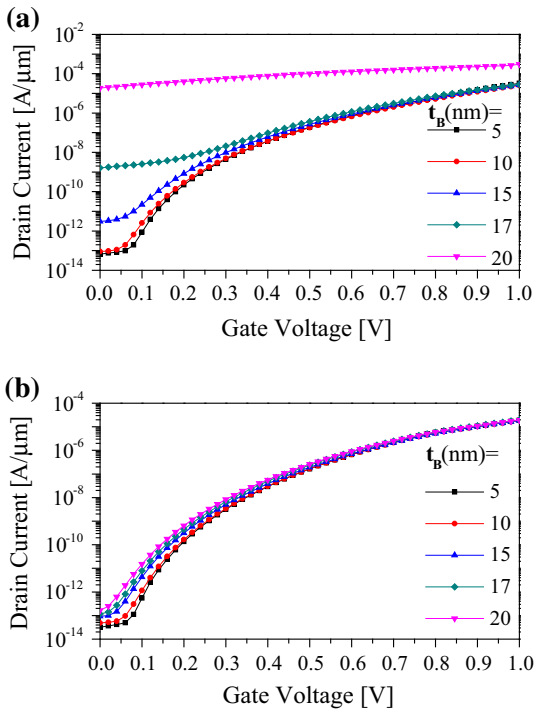


Fig. 6 **a** Simulated I_d–V_g characteristics of Si JLTFET for different body thickness (t_B), showing significant leakage for body thickness >10 nm. **b** I_d–V_g characteristics of Si JLTFET with lightly doped source for different body thickness showing reduced leakage current

height [32–34]. With increase in body thickness, the barrier below the p-gate gets lowered which increases the magnitude of current through the device in its OFF state. This unwanted leakage results in unacceptable static power dissipation and poor I_{ON}/I_{OFF} ratio. With the introduction of the lightly doped source region, $I_{OFF}$is not found to increase much with the increase in body thickness. Figure 7 portrays an increase in I_{OFF} from 3×10^{-14} to 1.5×10^{-13} A/μm for JLTFET with lightly doped source for a body thickness of 5 and 20 nm, respectively. The I_{ON} of both the structures is almost independent of the body thickness. However, for a uniformly doped JLTFET with $t_B = 20$ nm, the component of the I_{ON} due to thermal injection exceeds the current component due to band-to-band tunneling current, which results in higher I_{ON} than expected. The slight decrease in the drive current for the JLTFET with lightly doped source is probably due to reduced doping concentration. Figure 8 shows the I_{ON}/I_{OFF} ratio for both devices. The remarkable improvement in the I_{ON}/I_{OFF} ratio is clearly visible from Fig. 8. The I_{ON}/I_{OFF} ratio is maintained greater than 10^8 for the body thickness ranging from 5 to 20 nm.

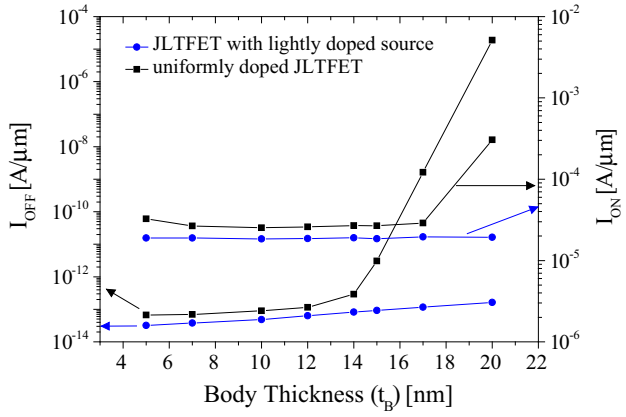


Fig. 7 Comparison of OFF-current and ON-current between uniformly doped JLTFET and JLTFET with lightly doped source

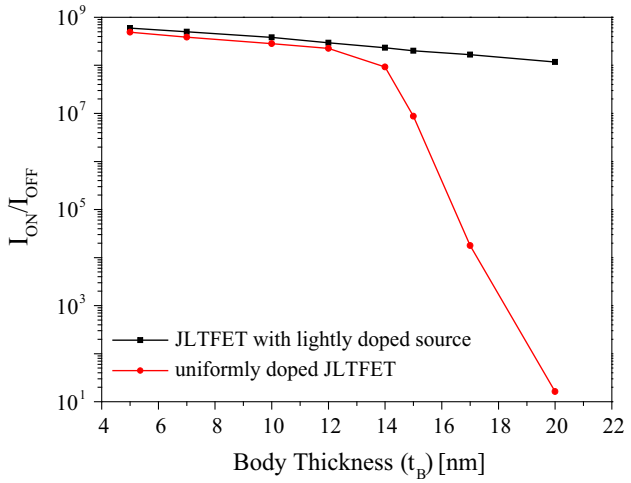


Fig. 8 Comparison of the I_{ON}/I_{OFF} ratio between a uniformly doped JLTFET and JLTFET with lightly doped source

In order to study the variation in the device characteristics with change in the position of the n^+-n junction, we show the transfer characteristics of the device for different positions of the junction in Fig. 9. From the figure, it is clear that for the same device with unchanged work function of the gate metals, the device gives best results when the junction is close to the spacing between the control gate and p-gate. This is not a stringent requirement as we can see that the I_{ON}/I_{OFF} is not greatly affected by the position of the junction. Moreover, we can adjust the work function of the control gate to lower the V_T, which will adjust the I_{ON}/I_{OFF} ratio. Thus, we can infer that the position of the junction can be flexibly optimized without affecting the device performance significantly.

Since the aim of our work is to propose a junctionless tunnel device with low leakage current, we should be avoiding an abrupt junction. All the analysis that is presented gives us a physical understanding of how the

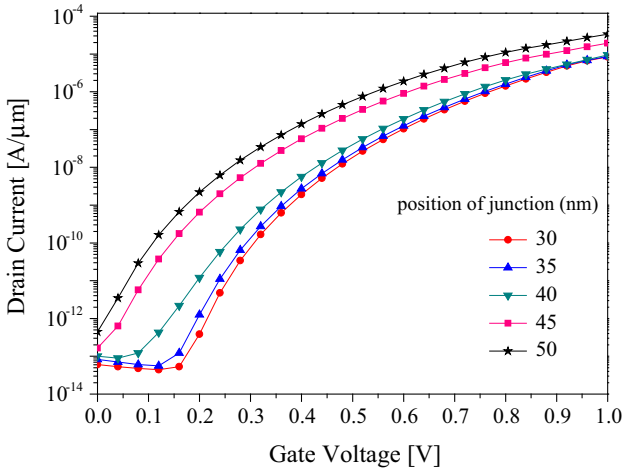


Fig. 9 Simulated I_d–V_g characteristics of Si JLTFET with lightly doped source for different positions of the n^+-n junction for a body thickness of 20 nm

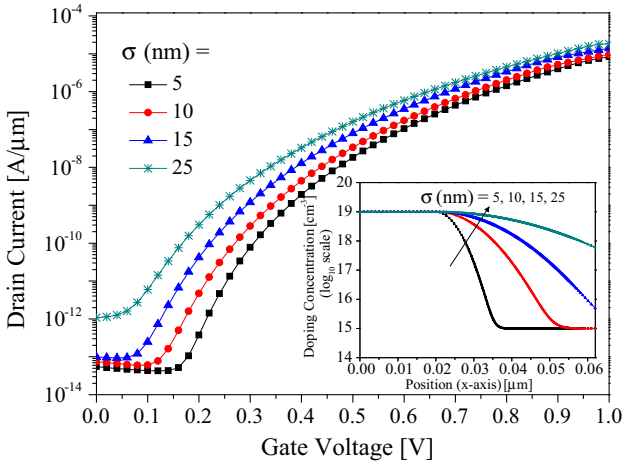


Fig. 10 I_d–V_g characteristics of Si JLTFET with lightly doped source for different values of σ (standard deviation) for a body thickness of 20 nm. The inset of the figure shows the lateral doping profile (along x) of the JLTFET body

leakage can be avoided using a lightly doped source. Now, we propose an alternative Gaussian distributed doping profile in the body which can be used instead of an abrupt n^+-n junction. The non-uniform doping profile is modeled using Gaussian distribution as found in ion-implanted devices. The doping profile follows a relation as given in (1).

$$N_d(x,y) = N_p \exp\left(-\frac{x^2}{2\sigma^2}\right) \quad (1)$$

The doping profiles used in our simulations are shown in the inset of Fig. 10. The doping concentration is allowed to vary laterally with x. The doping concentration starts to fall from its peak concentration of 10^{19} cm^{-3} (N_d) at

$x = 0.020$ μm (which is the edge of the control gate). Figure 10 portrays the change in device characteristics for different values of standard deviation (σ) used in the doping profile. For high values of σ, the doping concentration below the p-gate remains high. Thus, the depletion below the p-gate (at the center of the device) is weaker compared to a higher value of σ. As a result, the energy bands for high values of σ are not lifted as much as for lower values of σ. Therefore, the energy range for band-to-band tunneling in ON state is less for low values of σ, which leads to slightly reduced I_{ON} and increased V_T. However, the I_{ON} and V_T can be optimized by changing the control gate metal work function. The increase in I_{OFF} for higher values of σ is also due to the increase in leakage because of higher doping below the p-gate.

3 Conclusion

Firstly, we report the problem of excessive leakage through the center of the device for Si JLTFETs with body thickness wider than 10 nm. The reason for the leakage is mainly due to carrier injection in the source region. To extend the depletion region below the p-gate, we introduce a concept of lightly doped source. The leakage current was successfully reduced by eight orders of magnitude for a JLTFET of body thickness of 20 nm. The variability in the transfer characteristics of the device for different positions of the n^+-n junction is studied. It is found that the position of the junction can be flexibly adjusted without any significant change in the device performance. In order to avoid any abrupt junction, we propose the JLTFET with lateral non-uniform doping following the Gaussian profile. The device shows improved results comparable to abrupt junction JLTFET. Thus, we can avoid the problem of leakage in JLTFET by using the non-uniformly doped architecture. Using the non-uniformly doped structure, we can try to implement bulk JLTFET structures in SOI or FInFET configurations.

References

1. H. Riel, A.M. Ionescu, Tunnel field-effect transistors as energy-efficient electronic switches. Nature **479**(7373), 329–337 (2011)
2. K. Boucart, A.M. Ionescu, Double-gate tunnel FET with high- κ gate dielectric. IEEE Trans. Electron Devices **54**(7), 1725–1733 (2007)
3. K.K. Bhuwalka, S. Sedlmaier, A.K. Ludsteck, C. Tolksdorf, J. Schulze, I. Eisele, Vertical tunnel field-effect transistor. IEEE Trans. Electron Devices **51**(2), 279–282 (2004)
4. K.E. Moselund, H. Schmid, C. Bessire, M.T. Bjork, H. Ghoneim, H. Riel, InAs-Si nanowire heterojunction tunnel FETs. IEEE Electron Device Lett. **33**(10), 1453–1455 (2012)
5. K. Tomioka, T. Fukui, Tunnel field-effect transistor using InAs nanowire/Si heterojunction. Appl. Phys. Lett. **98**(8), 083114–083114–3 (2011)
6. S. Mookerjea, D. Mohata, T. Mayer, V. Narayanan, S. Datta, Temperature-dependent I–V characteristics of a vertical in 0.53 Ga 0.47 as tunnel FET. IEEE Electron Device Lett. **31**(6), 564–566566 (2010)
7. N. Patel, A. Ramesha, S. Mahapatra, Drive current boosting of n-type tunnel FET with strained SiGe layer at source. Microelectronics J. **39**(12), 1671–1677 (2008)
8. H. Riel, K.E. Moselund, C. Bessire, M.T. Bjork, A. Schenk, and H. Ghoneim, "InAs-Si heterojunction nanowire tunnel diodes and tunnel FETs." in Electron Devices Meeting (IEDM), IEEE International, 16 (2012)
9. K.K. Bhuwalka, J. Schulze, I. Eisele, Performance enhancement of vertical tunnel field-effect transistor with SiGe in the δp + layer. Jpn. J. Appl. Phys. **43**(7R), 4073–4078 (2004)
10. S. Mookerjea, S. Datta, "Comparative study of Si, Ge and in as based steep subthreshold slope tunnel transistors for 0.25 V supply voltage logic applications, 2008 device res. conf., pp. 47–48 (2008)
11. A. Schenk, R. Rhyner, M. Luisier, and C. Bessire, Analysis of Si, InAs, and Si-InAs tunnel diodes and tunnel FETs using different transport models, 2011 Int. Conf. Simul. Semicond. Process. Devices 263–266 (2011)
12. T. Krishnamohan, D.K.D. Kim, S. Raghunathan, K. Saraswat, Double-gate strained-ge heterostructure tunneling FET (TFET) With record high drive currents and ≪60 mV/dec subthreshold slope, 2008 IEEE Int. Electron Devices Meet., pp. 1–3 (2008)
13. L. Lattanzio, L. De Michielis, A.M. Ionescu, Electron-hole bilayer tunnel FET for steep subthreshold swing and improved ON current, in Solid-State Device Research Conference (ESSDERC). Proceedings of the European **2011**, 259–262 (2011)
14. C. Shih, N.D. Chien, Sub-10-nm tunnel field-effect transistor with graded Si/Ge heterojunction. Electron Device Lett. IEEE **32**(11), 1498–1500 (2011)
15. S.H. Kim, S. Agarwal, Z.A. Jacobson, P. Matheu, C. Hu, T.-J. Liu, Tunnel field effect transistor with raised germanium source. IEEE Electron Device Lett. **31**(10), 1107–1109 (2010)
16. K. Ganapathi, S. Salahuddin, Heterojunction vertical band-to-band tunneling transistors for steep subthreshold swing and high on current. IEEE Electron Device Lett. **32**(5), 689–691 (2011)
17. K. Rok, Y. Jun, S. Cho, J. Hwa, J. Lee, J. Bae, E. Cho, I. Man, InGaAs/InPheterojunction-channel tunneling field-effect transistor for ultra-low operating and standby power application below supply voltage of 0.5 V. Curr. Appl. Phys. **13**(9), 2051–2054 (2013)
18. B. Ghosh, P. Bal, P. Mondal, A junctionless tunnel field effect transistor with low subthreshold slope. J. Comput. Electron. **12**(3), 428–436 (2013)
19. B. Ghosh, M.W. Akram, Junctionless tunnel field effect transistor. IEEE Electron Device Lett. **34**(5), 584–586 (2013)
20. P. Bal, M.W. Akram, P. Mondal, B. Ghosh, Performance estimation of sub-30 nm junctionless tunnel FET (JLTFET). J. Comput. Electron. **12**(4), 782–789 (2013)
21. P. Bal, B. Ghosh, P. Mondal, B.M.M. Tripathi, Dual material gate junctionless tunnel field effect transistor. J. Comput. Electron. **13**(1), 230–234 (2014)
22. M.W. Akram, B. Ghosh, P. Bal, P. Mondal, P-type double gate junctionless tunnel field effect transistor. J. Semicond. **35**(1), 14002 (2014)
23. P.K. Asthana, B. Ghosh, Y. Goswami, B.M.M. Tripathi, High-Speed and Low-Power Ultradeep-Submicrometer III–V Heterojunctionless. IEEE Trans. Electron Devices **61**(2), 479–486 (2014)