Phase-Locked Loop Based on Selective Harmonics Elimination for Utility Applications

Naji Rajai Nasri Ama, Fernando Ortiz Martinz, Lourenço Matakas, Jr., and Fuad Kassab Junior, *Member, IEEE*

***Abstract*—Phase-locked loops (PLL) are widely used in power electronics equipment connected to the mains. The use of a square wave voltage-controlled oscillator instead of a sinusoidal one eliminates one multiplier, resulting in a simple PLL algorithm, suitable for low-cost processors. In spite of its simplicity, distorted grid voltages cause steady-state phase error. This paper proposes the use of a modified square waveform obtained by the selective harmonics elimination (SHE) method to solve the phase error problem. Simulation and experimental results for the steady state and the transient tests are presented to validate the proposed single-phase and three-phase SHE-PLL methods. The tests using a field-programmable gate array show that the dynamic response of the proposed method is similar to that of classical PLL, with a simpler implementation.**

***Index Terms*—Field-programmable gate arrays (FPGA), phase-locked loops (PLL), power electronics.**

I. Introduction

PHASE-LOCKED loops (PLLs) are widely used in communication, control, automation, and instrumentation systems to achieve signal synchronization. Recently, PLLs have found many applications in grid-connected power electronic devices: 1) to synchronize thyristor firing circuits [1]; 2) to transform variables between stationary and synchronous rotating reference frames [2], [3]; 3) to compute power system disturbances in power quality monitoring systems [4], [5]; and 4) to calculate reference signals for the internal control loops in uninterruptible power supplies [6], dynamic voltage restorers [2], [5], active filters [5], and power converters used in distributed energy systems [3], [7], including wind and photovoltaic systems [8]. In these applications, the PLL detects the phase angle and frequency of the grid fundamental voltage. On the other hand, three-phase PLLs detect the positive sequence component, even for distorted and unbalanced grids [3], [9]–[20].

The typical PLL [21], [22] is composed of a phase detector (PD), a loop filter (LF), and a voltage-controlled oscillator (VCO) (see Fig. 1).

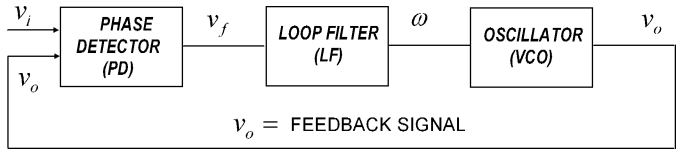

Fig. 1. PLL—general structure.

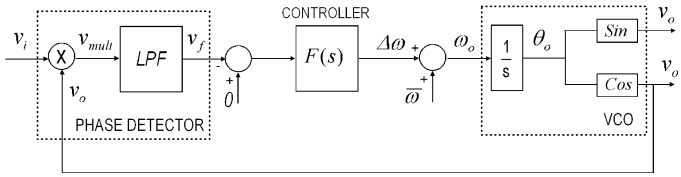

Fig. 2. Classical single-phase PLL.

The PD compares the reference signal v_i with the feedback signal v_o, producing a signal v_f that depends on the phase error between v_i and v_o. All the cases discussed in this paper use the linearized multiplier type PD [20]–[22] followed by a low-pass filter (LPF). The LF attenuates the oscillating terms of the error signal v_f. The VCO generates an output signal v_o with frequency ω. The complete system produces an output signal v_o, synchronized in phase and frequency with the reference signal v_i.

Often the feedback signal v_o is a unit amplitude sinusoidal signal [1]–[11], [23], [24]. This strategy is defined in this paper as a classical PLL.

In [21] and [22], the sinusoidal VCO was replaced by a square wave VCO for analog implementation. This method does not need an analog multiplier in the PD block and is suitable for hardware implementations with pure sinusoidal input. The product of v_i by a two-level (± 1) signal v_o was accomplished by mixed analog/digital circuitry. Nowadays, the square wave strategy can be useful for PLLs implemented in microcontrollers, DSPs, and field-programmable gate arrays (FPGA). In this paper, the PD in Fig. 2 that computes the product $v_{\rm mult} = v_o \cdot v_i$ in the classical PLL is replaced by the operation $v_{\rm mult} = {\rm sign}(v_o)$, eliminating one multiplier. Another advantage compared to the classical PLL is to reduce memory usage associated with long lookup tables required to store the sinusoidal waveforms with reasonable accuracy.

According to [22], the square wave PLL is not applicable to input signals with harmonics, because the steady-state phase error is not null. We propose an improvement on the square wave PLL which consists in substituting the original square wave by the selective harmonics elimination (SHE) waveform, thus minimizing the PLL phase angle error.

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The authors are with the Polytechnic School of the University of São Paulo, 05508-900 São Paulo, Brazil (e-mail; naji@usp.br; fernando_martinz@yahoo.com; matakas@pea.usp.br; fuad@lac.usp.br).

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This paper is organized as follows. Section II reviews the operation of the classical PLL, emphasizing that it synchronizes with the fundamental component of the input signal v_i. Section III describes the square wave PLL. Section IV discusses the operation of the square wave PLL, explaining why the phase error increases with distorted input signals.

The PLL phase error is computed as a function of the spectrum of the grid voltage. Section V discusses the requirements for the pulsewidth modulated squared SHE waveform and the evaluation of its switching angles. Section VI presents simulation and experimental results for both steady state and transient tests of a single-phase PLL, validating the proposed SHE-PLL method. The tests were carried out using an FPGA. The three-phase SHE-PLL is analyzed in Section VII, where experimental results are shown. The square wave PLL and the SHE-PLL algorithms present a dynamic response similar to the classical PLL. Notwithstanding, they are implemented in a simpler way. Section VIII concludes this paper.

II. Classical Single-Phase PLL

Fig. 2 shows the topology of the classical single-phase PLL, using a multiplier type PD.

Let the input voltage be represented by

$$v_i = A_1 \sin(\omega_1 t + \phi_1) + A_2 \sin(2\omega_1 t + \phi_2) + \ldots = \sum_{k=1}^{\infty} A_k \sin(k\omega_1 t + \phi_k) \quad (1)$$

where A_1 is the fundamental peak value, ω_1 is the fundamental angular velocity (frequency), $\overline{\omega}$ is the grid nominal frequency, and ϕ_1 is the fundamental phase angle. The feedback signal v_o, which is the PLL output with unit amplitude, is a sinusoidal voltage represented by

$$v_o = \cos(\omega_o t + \phi_o) = \cos\theta_o. \quad (2)$$

The signal v_{mult} is computed in the Appendix by calculating the multiplier output $v_{\text{mult}} = v_o \cdot v_i$ in (A.1) and by considering that v_o tracks v_i, i.e.,$(\omega_o = \omega_1)$ in (A.2). The signal v_{mult} presents a dc and oscillating components. Keeping in mind that v_i contains odd and even harmonics, the oscillating terms of v_{mult} are thus multiples of the mains fundamental frequency ω_1.

The LPF block is designed to guarantee that the high frequency components of v_{mult} are attenuated; thus, the steady-state filtered output v_f can be described by

$$v_f = \frac{A_1}{2} \cdot \sin\phi_d. \quad (3)$$

In this paper, the LPF block in Fig. 2 is implemented using a moving average filter (MAV) [5], [14], [18]–[20]. The MAV filter with a window length *T*, corresponding to the fundamental frequency period, eliminates all the oscillating terms of v_{mult} that are multiples of the fundamental frequency ω_1. According to (A.2), if v_i contains only odd harmonics, the oscillating terms of v_{mult} are multiple of $2\omega_1$. In this case, a MAV with a window length of *T*/2 can be used, resulting in lower memory usage and faster LPF response [14].

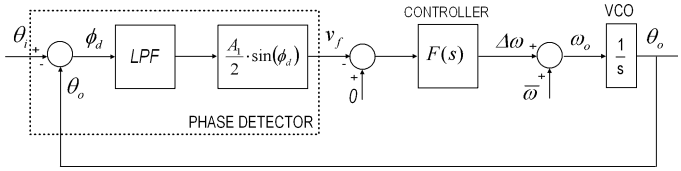

Fig. 3. Nonlinear single-phase PLL dynamic model.

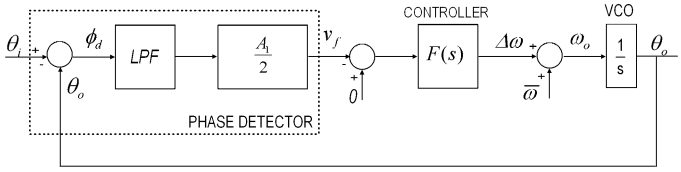

Fig. 4. Linearized single-phase PLL model.

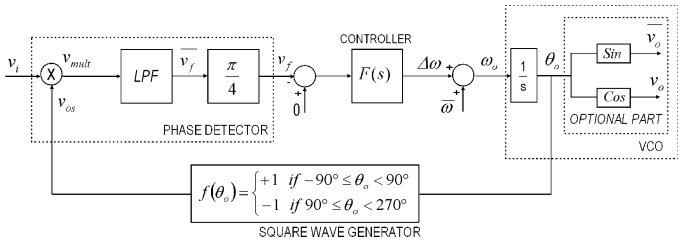

Fig. 5. Square wave feedback signal PLL.

Equation (3) leads to the nonlinear model shown in Fig. 3. The phase error is $\phi_d = \theta_i - \theta_o$. Considering $\theta_i = \omega_1 t + \phi_1$ and $\theta_o = \omega_o t + \phi_o$, when $\omega_1 = \omega_o$, the phase error is equal to $\phi_d = \phi_1 - \phi_o$.

If ϕ_d is very small, then $\sin(\phi_d) \cong \phi_d$ and the linearized model in Fig. 4 is obtained.

Note that the closed-loop gain of this PLL is highly dependent on the peak amplitude of the fundamental voltage A_1, as seen in (3). Normalization of the input voltage has been suggested in [9] to minimize the effects of grid voltage variations on the PLL dynamic response.

For the stable steady-state operation point, $\phi_d = 0$, $v_f = 0$ and v_o are in quadrature with the input voltage v_i. The signal $\overline{v_o}$ in Fig. 2 is in phase with the input voltage v_i.

III. Square Wave Feedback Signal PLL

The single-phase square wave PLL, shown in Fig. 5, has the same structure of the classical PLL in Fig. 2. However, it uses the square wave v_{os} (see Fig. 6) instead of using the output voltage $v_o = \cos(\omega_o t + \phi_o) = \cos\theta_o$ as feedback signal to the PD. The signal v_{os} is obtained at the output of the square wave generator and depends on the phase angle θ_o according to the function $f(\theta_o)$ defined in Fig. 5.

The first component of the Fourier series expansion of v_{os} is proportional to the sinusoidal signal v_o, suggesting that the behavior of the square wave PLL is similar to the classical PLL. The gain $\pi/4$, which is added to keep the closed-loop gain constant for all presented PLLs algorithms, will be derived in Section IV-A. Performance loss due to the harmonic components of v_{os} will be discussed in Section IV-B. One advantage of a

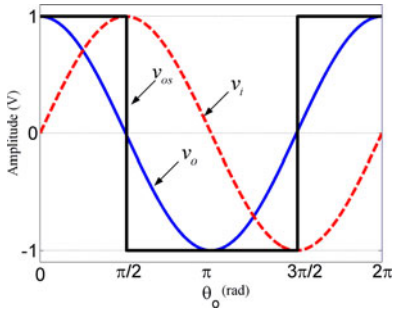

Fig. 6. Square wave v_{os} and PLL output v_o voltage.

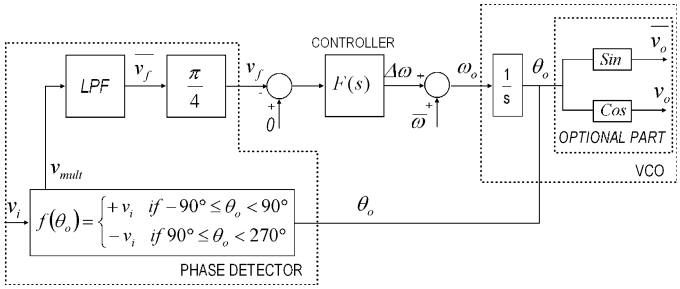

Fig. 7. Square wave feedback signal PLL.

square wave VCO is that the PD becomes a simple "multiply by one" operation which can be implemented as shown in Fig. 7. The signal $v_{\rm mult}$ corresponds to the input signal v_i, affected only by the signal of v_{os}. It is a promising alternative for low-cost converter systems based on microprocessors, DSPs, or FPGAs.

A second feature is that the evaluation of the sin and cos functions is computed outside the PLL loop, and does not influence its performance. The sin (or cos) generators (see Fig. 7) can be omitted in some applications that include the control of thyristor converters [1]. In this case, only θ_o is required.

IV. Analysis of the Square Wave Feedback Signal PLL

Using Fourier series, v_{os} can be expressed as

$$v_{os} = \frac{4}{\pi}\cdot\left\{\cos(\omega_o t+\phi_o) - \frac{1}{3}\cos(3\,\omega_o t+3\phi_o)+\ldots\right\}$$
$$= -\frac{4}{\pi}\cdot\sum_{j=1}^{\infty}(-1)^j\cdot\frac{\cos\left[(2j-1)\,\omega_o t+(2j-1)\,\phi_o\right]}{2j-1}. \quad (4)$$

The aforementioned equation confirms that v_{os} contains a scaled copy of the output voltage v_o. The input signal v_i is described by (1). Equation (A.3), in the appendix computes $v_{\rm mult} = v_{os}\cdot v_i$. If v_o tracks v_i, i.e., $(\omega_o = \omega_1)$, $v_{\rm mult}$ is described by (A.4).

A. Pure Fundamental Sinusoidal Input Voltage

Let the input voltage be represented by $v_i = A_1\sin(\omega_1 t+\phi_1)$. The output of the multiplier $v_{\rm mult}$ (A.5) presents a dc component and oscillating terms.

Using the assumption that the oscillatory terms of $v_{\rm mult}$ are sufficiently attenuated by the LPF, the filtered signal $\overline{v_f}$ is similar to the one obtained in (3), except for a $4/\pi$ gain, i.e.,

$$\overline{v_f} = \frac{4}{\pi}\cdot\frac{A_1}{2}\sin\phi_d. \quad (5)$$

For small values of ϕ_d, $\sin(\phi_d)\cong\phi_d$ and consequently

$$\overline{v_f} = \frac{4}{\pi}\cdot\frac{A_1}{2}\cdot\phi_d. \quad (6)$$

The square wave PLL and the modified square wave PLL (depicted in Figs. 5 and 7) preserve the LPF and the controller $F(s)$ but include the gain $\pi/4$ to achieve the same dynamical performance of the classical PLL.

B. Distorted Input Voltage

A more realistic input voltage is analyzed in this section, considering harmonic distortion at the grid voltages, according to (1). The output of the multiplier $v_{\rm mult}$ (A.4), presents a dc component and oscillating terms.

The LPF attenuates the high-order frequency terms of $v_{\rm mult}$ (A.4); thus, the PD output $\overline{v_f}$ is

$$\overline{v_f} = \frac{2}{\pi}\cdot\left[\begin{array}{c} A_1\sin\phi_d - \dfrac{A_3}{3}\sin(\phi_3-3\phi_o)+\ldots \\ -\dfrac{(-1)^j\,A_k}{2j-1}\sin\left[\phi_{2j-1}-(2j-1)\cdot\phi_o\right]\end{array}\right]$$
$$j=1,\ldots,\infty. \quad (7)$$

Compared to (6), (7) shows that the inclusion of harmonics in v_i results in new dc component terms. Harmonics of v_i and v_{os} with the same order contribute to $\overline{v_f}$. The controller forces v_f and $\overline{v_f}$ to zero; nonetheless, according to (7), the inclusion of harmonics in v_i may lead to $\phi_d\neq 0$ even if $\overline{v_f}=0$. This explains the phase error for the square PLL operating with distorted v_i.

For example, suppose v_i includes a third harmonic with amplitude $A_3 = 0.3A_1$, and consider the worst case when $\sin(\phi_3-3\phi_o)=\pm1$. This results in $\overline{v_f} = \frac{2}{\pi}\cdot\left[A_1\sin\phi_d \mp \frac{0.3}{3}\cdot A_1\cdot 1\right]$. When the PLL is locked, then $\overline{v_f}=0$, which results in a phase error equal to $\phi_d = \sin^{-1}(\pm 0.3/3) = \pm 5.73°$. The solution for this problem is presented in the next section.

V. SHE-PLL

As discussed in Section IV-B, if v_i and v_{os} have harmonics of the same order, they contribute to the dc component of $v_{\rm mult}$ resulting in phase error. One solution for this problem consists of eliminating all the relevant harmonics that exist in the input voltage v_i from the VCO signal v_{os}. This new signal is called $v_{o\rm SHE}$ and is obtained by means of the SHE algorithm.

The SHE waveform $v_{o\rm SHE}$ is shown in Fig. 8, for $N=5$ switching angles $(\alpha_1,\alpha_2,\alpha_3,\alpha_4,\alpha_5)$ per quarter of VCO period T. The remaining switching instants are calculated by using the quarter- and half-wave symmetry of $v_{o\rm SHE}$ shown in Fig. 8.

The SHE waveform can be represented by a Fourier series according to

$$v_{o\rm SHE} = \frac{a_0}{2}+\sum_{n=1}^{\infty}a_n\cos(n\omega_o t)+b_n\sin(n\omega_o t). \quad (8)$$

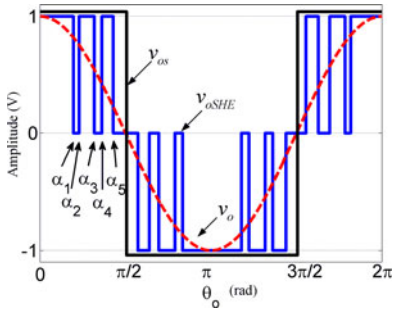

Fig. 8. SHE proposed feedback signal, for $N = 5$.

For the three-level $v_{o\mathrm{SHE}}$ waveform in Fig. 8, see the following.

1) The half-wave symmetry property results in $a_0 = 0$*:*

The quarter-wave symmetry property results in

$$a_n = \begin{cases} \dfrac{8}{T} \cdot \displaystyle\int_0^{T/4} v_{o\mathrm{SHE}} \cos n\omega_o t \, dt, & n \text{ is odd} \\ 0, & n \text{ is even.} \end{cases} \tag{9}$$

2) The even-wave symmetry property of $v_{o\mathrm{SHE}}$ *results in* $b_n = 0$ *for all* n*:*

According to [25], the quarter-wave coefficients are determined by

$$a_n = \frac{8}{2\pi} \cdot \left[\int_0^{\alpha_1} \cos n\theta_o \, d\theta_o + \int_{\alpha_2}^{\alpha_3} \cos n\theta_o \, d\theta_o + \int_{\alpha_4}^{\alpha_5} \cos n\theta_o \, d\theta_o \right] \tag{10}$$

$$a_n = \frac{4}{n\pi} \cdot (\sin n\alpha_1 - \sin n\alpha_2 + \sin n\alpha_3 - \sin n\alpha_4 + \sin n\alpha_5). \tag{11}$$

In this paper, the values of $(\alpha_1, \alpha_2, \alpha_3, \alpha_4, \alpha_5)$ are calculated by imposing $a_1 = 1$, and $a_3 = a_5 = a_7 = a_9 = 0$ in (11), resulting in

$$a_1 = \frac{4}{\pi} \cdot (\sin\alpha_1 - \sin\alpha_2 + \sin\alpha_3 - \sin\alpha_4 + \sin\alpha_5) = 1 \tag{12}$$

$$a_3 = \frac{4}{3\pi} \cdot (\sin 3\alpha_1 - \sin 3\alpha_2 + \sin 3\alpha_3 - \sin 3\alpha_4 + \sin 3\alpha_5) = 0 \tag{13}$$

$$a_5 = \frac{4}{5\pi} \cdot (\sin 5\alpha_1 - \sin 5\alpha_2 + \sin 5\alpha_3 - \sin 5\alpha_4 + \sin 5\alpha_5) = 0 \tag{14}$$

$$a_7 = \frac{4}{7\pi} \cdot (\sin 7\alpha_1 - \sin 7\alpha_2 + \sin 7\alpha_3 - \sin 7\alpha_4 + \sin 7\alpha_5) = 0 \tag{15}$$

$$a_9 = \frac{4}{9\pi} \cdot (\sin 9\alpha_1 - \sin 9\alpha_2 + \sin 9\alpha_3 - \sin 9\alpha_4 + \sin 9\alpha_5) = 0. \tag{16}$$

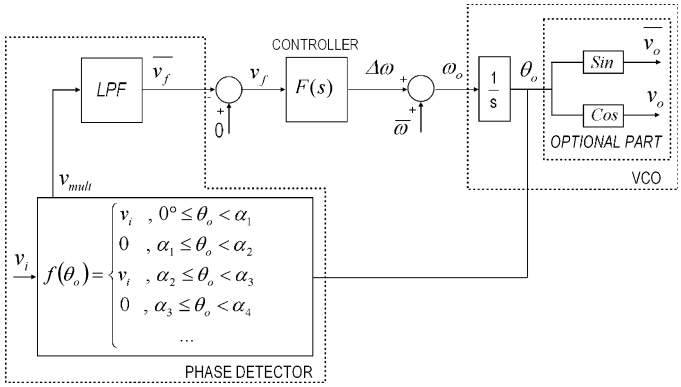

Fig. 9. SHE-PLL.

The numerical solution for the system of five nonlinear (12)–(16) is obtained using the Newton–Raphson method as presented in [25]. The starting point for the algorithm is obtained using the method presented in [26], resulting in $\alpha_1 = 25.58°$, $\alpha_2 = 28.48°$, $\alpha_3 = 48.49°$, $\alpha_4 = 58.87°$, and $\alpha_5 = 69.65°$.

The block diagram of the proposed SHE-PLL (see Fig. 9) is similar to that of the square wave feedback (see Fig. 7). A slightly bigger lookup table compared to the square PLL is now required, since additional switching angles must be included. However, the SHE-PLL table will still be substantially smaller than what is required for generating a sinusoidal waveform.

VI. Simulation and Experimental Results

To validate the SHE-PLL, we performed simulations using MATLAB/Simulink and experiments using system generator from Xilinx. The experimental setup was implemented using the Spartan-3E FPGA starter kit board. For both cases, we adopted a sampling frequency of $f_S = 12$ kHz and a fundamental frequency of $f_1 = 60$ Hz. The square wave feedback signal PLL (see Fig. 7) and the SHE-PLL (see Fig. 9) performances were analyzed with respect to the classical PLL in Fig. 2.

The input waveform was generated by an external programmable signal generator (Agilent 332201 A) and injected in the FPGA A/D converter. The system runs in real time. The measured signals were periodically stored in the FPGA memory and sent to the PC using the ChipScope software from Xilinx. All tests were performed with unit amplitude voltages.

The PLL closed-loop natural frequency was chosen to be $\omega_n = 25$ rad/s and the damping factor equal to $\zeta = 0.7$. The use of the tuning method presented in [27] for continuous time proportional-integral (PI) controllers and considering the gain of (3) result in a proportional gain $k_P = 70\ \mathrm{V} \cdot \mathrm{s}^{-1}$ and an integral gain $k_i = 1250\ \mathrm{s}^{-1}$. The discrete-time PI transfer function was obtained by the backward Euler method as follows:

$$F(z) = \frac{70.1042 - 70 \cdot z^{-1}}{1 - z^{-1}}. \tag{17}$$

In this paper, v_i is assumed to contain only odd harmonics, so that the MAV should cancel the even harmonics of v_f. According to [19], the MAV with window length $T/2$ must contain $N2 = f_s/(2f_1) = 100$ samples/fundamental half-period. $N2$ is

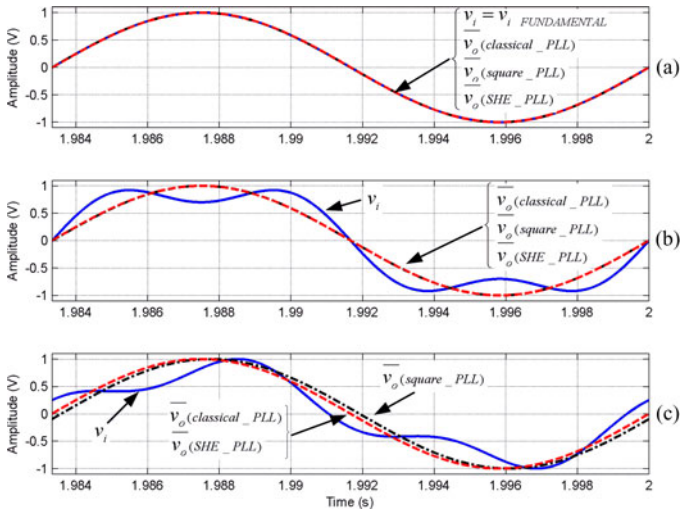

Fig. 10. Simulation results. (a) Sinusoidal input voltage. (b) Input voltage with fundamental plus in phase 30% third harmonic. (c) Input voltage with fundamental plus 90° displaced 30% third harmonic. Input voltage (solid line), classical PLL (dotted line), square PLL (dash-dotted line), and SHE-PLL (dashed line).

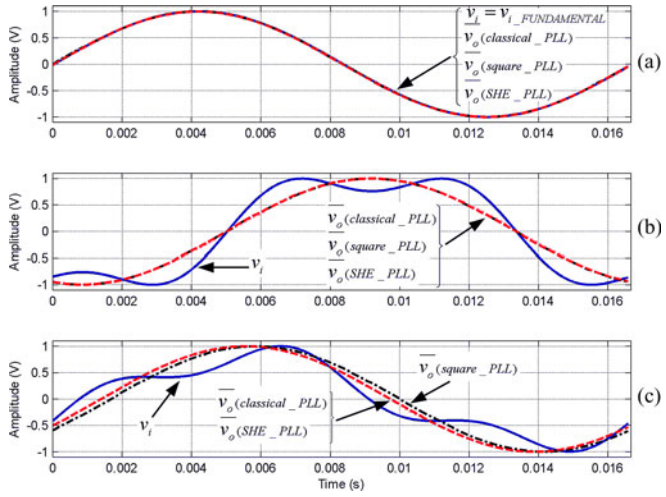

Fig. 11. Experimental results. (a) Sinusoidal input voltage. (b) Input voltage with fundamental plus in phase 30% third harmonic (c) Input voltage with fundamental plus 90° displaced 30% third harmonic. Input voltage (solid line), classical PLL (dotted line), square PLL (dash-dotted line), and SHE-PLL (dashed line).

an integer number that defines the order of the MAV. The discrete transfer function of the MAV is

$$\mathrm{LPF}\,(z) = \frac{1}{100} \cdot \frac{1 - z^{-100}}{1 - z^{-1}}. \tag{18}$$

A. Steady-State Tests

Fig. 10 shows the simulated waveforms for the input signal v_i and the output signal v_o, for the classical, square wave, and SHE PLLs. Fig. 11 presents the corresponding experimental waveforms. The ideal case, in which the input signal is a sinusoidal voltage with zero phase angle, is shown in Figs. 10(a) and 11(a). As expected from (3) and (5), the results for the three PLL methods are equal, with zero steady-state phase error between v_o and v_i.

Figs. 10(b) and 11(b) show the effect of injecting a third harmonic component with amplitude equal to $A_3 = 0.3$, in phase with the fundamental component. Again, zero steady-state error is achieved for the classical PLL, as expected from (3). For the square wave and SHE PLLs, the steady-state error is also null, since from (7) $\overline{v_f} = 0.5 \cdot [1 \cdot \sin(0-0) - (0.3/3) \cdot \sin(0 - 3 \cdot 0)] = 0$.

Now consider that the third harmonic component of v_i lags the fundamental voltage by 90°. As seen in Figs. 10(c) and 11(c), the classical PLL achieves zero steady-state error, as expected from (3). However, the square wave PLL presents the steady-state error calculated in Section IV-B, i.e., $\phi_d = -5.73°$ (0.265 ms), where the negative angle means a lag fundamental voltage. In this case, when the SHE method is implemented, the steady-state error is null, as shown in Figs. 10(c) and 11(c), because $v_{o\mathrm{SHE}}$ has no third harmonic. In other words, in the absence of low-order harmonics in $v_{o\mathrm{SHE}}$, these low-order harmonics of v_i will not add to the output of the PD (7). Only harmonics of order higher or equal to $2N + 1 = 11$ will cause phase error. The SHE-PLL is a good solution because high-order, high amplitude harmonics are not expected on the grid voltages.

If the grid distortion is low, the designer can choose $v_{o\mathrm{SHE}}$ to have a lower number of switching angles N. If v_i is sinusoidal, then even the square wave PLL (corresponding to the SHE-PLL with $N = 2$) has a good performance.

B. Transient Tests

In order to evaluate the PLL transient response to grid faults, an input signal with a 50% voltage sag and a 45° phase jump was applied to the three PLLs. Simulation and experimental results are, respectively, shown in Figs. 12 and 13. All the PLLs present the same behavior because they have the same closed-loop gain. Transient response is slower after the voltage sag, and faster when v_i restores to unit amplitude because as discussed in previous sections, the amplitude of the fundamental of v_i affects the closed-loop gain. In steady state, the PD output v_f approaches zero. The signal v_f is proportional to $\sin(\phi_d)$, so that $v_f = 0$ corresponds to zero phase error ($\phi_d = 0$).

Fig. 14 presents experimental results for the SHE-PLL during a severe fault, where v_i goes to zero for a period of 0.4 s and recovers to the unit amplitude. In these tests, the PI output is limited to ±37.7 rad/s (±10 Hz). Even if the PI integrator drifts while $v_i = 0$, the sinusoidal VCO output $\overline{v_o}$ continues operating (although at a wrong frequency). As soon as v_i recovers, the PLL tracks correctly again.

In order to evaluate the transient response and the robustness to frequency variation of the three PLL methods, a frequency step from 60 to 66 Hz is applied at the input voltage v_i at $t =$ 0.055 s, as shown in Fig. 15 (experimental). The input voltage is a unit amplitude fundamental component. The parameters of the PI controller and of the MAV filter are the same for the three PLLs, assuring identical dynamic responses for the three cases as can be seen in Fig. 15.

Since the frequency response of the MAV filter depends on the grid fundamental frequency, the oscillating terms of v_{mult} will not be completely canceled when operating far from the

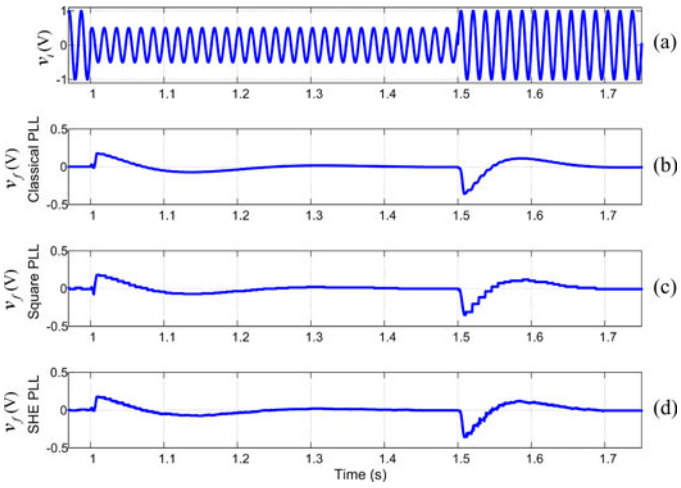

Fig. 12. Simulated results. (a) Input v_i with 50% voltage sag and $+45^\circ$ phase jump. PD output v_f for the (b) classical PLL, (c) square wave PLL, and (d) SHE-PLL.

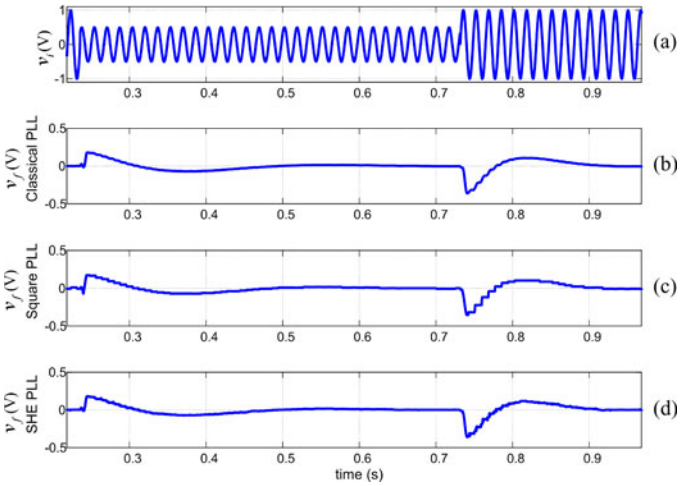

Fig. 13. Experimental results. (a) Input v_i with 50% voltage sag and $+45^\circ$ phase jump. PD output v_f for the (b) classical PLL, (c) square wave PLL, and (d) SHE-PLL.

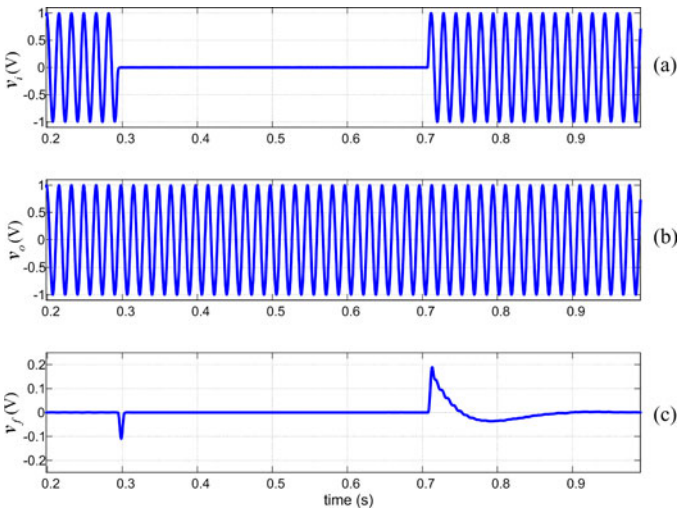

Fig. 14. Experimental results (SHE-PLL): (a) input voltage, (b) sinusoidal output $\overline{v_o}$, and (c) v_f.

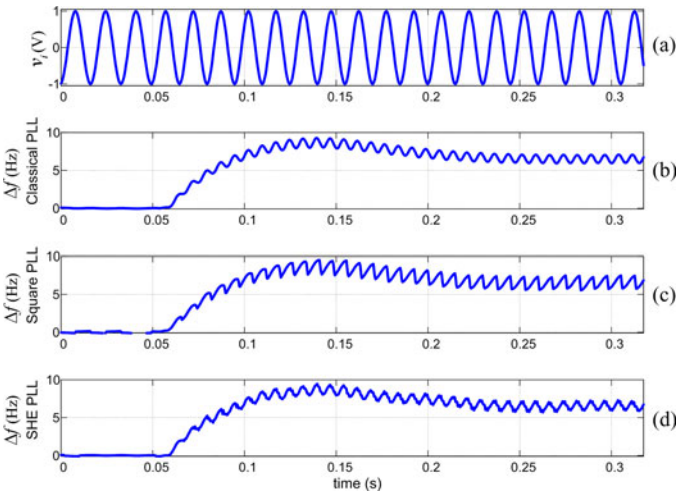

Fig. 15. Experimental results—frequency jump from 60 to 66 Hz. (a) Input signal. (b) Δf-classical PLL. (c) Δf-square wave PLL. (d) Δf-SHE-PLL.

MAV filter nominal frequency $\overline{\omega}$. They will appear in v_f and on $\Delta\omega$ (Δf) when the frequency of v_i is not exactly 60 Hz. After the transient, Δf will settle at 66 Hz.

In applications where this ripple is not acceptable, an adaptive window for the MAV may be used [5]. However, since for interconnected and for distributed generation (DG) power systems the permissible fundamental frequency variation is small, the square wave PLL and the SHE-PLL with MAV still guarantee very good harmonics attenuation on v_f. For instance, the work in [28] limits this variation up to $\pm 1\%$ of nominal frequency for 99.5% of week in interconnected power systems. Additionally, it is established in [29] that for DG systems, no reconnection can be made if the power system frequency is in the range of 59.3 to 60.5 Hz for a stabilization period of up to 5 min (60 Hz nominal frequency).

VII. Three-Phase SHE-PLL

The synchronous reference frame PLL (SRF-PLL) is shown in Fig. 16 and is well described in the literature [3], [9], [10], [12]–[16], and [20]. It tracks the positive sequence components (at fundamental frequency) of the three input signals v_{ia}, v_{ib}, and v_{ic}. The three input signals (v_{ia}, v_{ib}, v_{ic}) are converted to the *dq* rotating frame (v_d, v_q), in the *abc*/*dq* block by using the Park transformation [30]. The signal v_d is equivalent to the signal v_{mult} in Figs. 2, 5, and 9, and is used as the unfiltered measurement of the phase error. The VCO in Fig. 16 generates three-phase balanced signals $(\overline{v_{oa}}, \overline{v_{ob}}, \overline{v_{oc}})$ in phase with the positive sequence of the input signals. It also generates the other three-phase signals (v_{oa}, v_{ob}, v_{oc}) in quadrature with $(\overline{v_{oa}}, \overline{v_{ob}}, \overline{v_{oc}})$.

The *abc*/*dq* block of SRF-PLLs can be done in two steps [9], [12], [13], [15], [16], or directly [20]. The first approach sequentially processes the input signals from the *abc* to the $\alpha\beta$ reference frame applying Clarke transformation [31] and then from the $\alpha\beta$ to the *dq* reference frame by using Park transformation [30]. The second approach [20] proposes the use of the direct calculation of the *dq* components. This can be

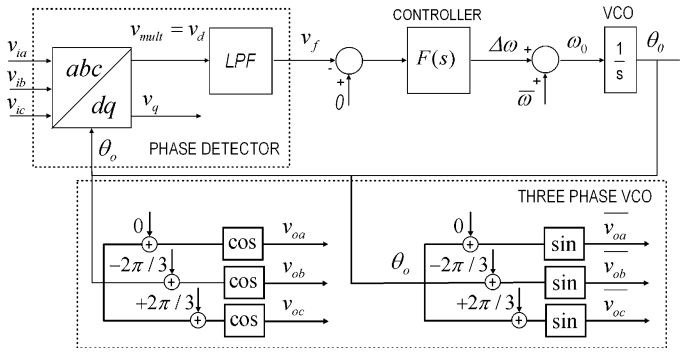

Fig. 16. SRF-PLL block diagram.

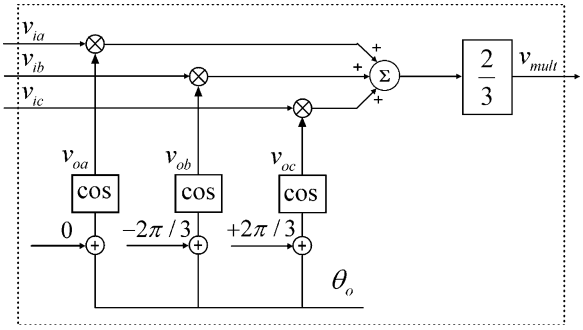

Fig. 17. PD obtained by the direct *abc*/*dq* (Park) transformation.

accomplished by

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos\theta_o & \cos(\theta_o - 2\pi/3) & \cos(\theta_o + 2\pi/3) \\ -\sin\theta_o & -\sin(\theta_o - 2\pi/3) & -\sin(\theta_o + 2\pi/3) \end{bmatrix} \times \begin{bmatrix} v_{ia} \\ v_{ib} \\ v_{ic} \end{bmatrix}. \quad (19)$$

Some minor variations of the SRF-PLLs found in the literature, and discussed in [10], include the following. 1) The use of v_q instead of v_d; 2) the use of positive feedback instead of negative feedback; and 3) the use of modified versions of the Park transformation [20]. These choices only affect the displacement angle between the input and output signals, by multiples of 90° and have no influence on the PLL dynamical performance.

Fig. 17 details the *abc*/*dq* block using (19). The signal $v_d = v_{\rm mult}$ is the sum of three parts. The first one $(^2/_3 v_{ia}\cos\theta_o)$ is identical to the $v_{\rm mult}$ signal for the classical PLL, except for the 2/3 gain. Phases *b* and *c* contribute with $^2/_3 v_{ib}\cos(\theta_o - 2\pi/3)$ and $^2/_3 v_{ic}\cos(\theta_o + 2\pi/3)$, respectively. The previous proposal of using a SHE waveform in Fig. 9 to avoid one multiplier in the classical PLL can be easily extended to the SRF-PLL. That is, a three-phase SHE-PLL is obtained if the three cosine functions are substituted by three SHE waveforms displaced by 120°. This eliminates three multipliers when compared to the SRF-PLL.

Fig. 18 shows the experimental results for the three-phase SHE-PLL under the joint occurrence of a 50% balanced voltage sag and a +45° phase jump with duration of five grid cycles. The three input waveforms were generated by three external programmable signal generators (Agilent 332201 A) and

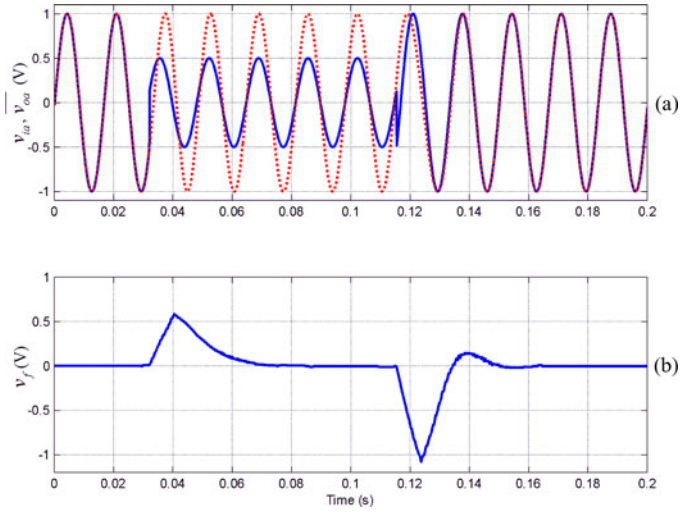

Fig. 18. Experimental results, three-phase SHE-PLL, and transient test. Balanced 50% sag plus +45° phase jump grid voltages. (a) Phase *a* input v_{ia} (solid line) and output $\overline{v_{oa}}$ (dotted line) voltages. (b) PD output v_f.

TABLE I
PHASORS OF THE FUNDAMENTAL COMPONENTS

PHASE	INPUT VOLTAGES (PEAK VALUE - V)	OUTPUT VOLTAGES (PEAK VALUE - V)
A	0.50∠11.54°	0.99∠11.66°
B	1.00∠−108.46°	1.00∠−108.31°
C	1.00∠131.54°	1.00∠131.63°

injected in the FPGA by means of three external A/D converters. The PI controller was discretized by using a backward Euler method and adjusted to achieve a fast dynamic response, according to the MAV-PLL in [20]. The phase margin was chosen to be 56°, for a crossover frequency $\omega_c = 141$ rad/s. This result in $k_P = 150\ \text{V}\cdot\ \text{s}^{-1}$ and $k_i = 70\ \text{s}^{-1}$.

Fig. 18(a) shows the input (v_{ia}) and output (v_{oa}) signals for phase *a*. The PLL locks to the positive sequence in about two cycles as shown in Fig. 18(a) and (b), when $v_f = 0$. The transient after the end of the voltage sag has low damping due to the increase of the closed-loop gain, caused by the variation of positive sequence amplitude from 0.5 to 1.0 V.

Steady-state experimental results in Fig. 19(b) show that the three-phase SHE-PLL locks at the positive sequence of the fundamental component when the grid presents distorted and unbalanced input voltages [see Fig. 19(a)]. The input signals v_{ia}, v_{ib}, and v_{ic} in Fig. 19(a) have equally displaced fundamental components, with amplitudes of 0.5, 1.0, and 1.0 V, respectively. The input signals [see Fig. 19(a)] also include a fifth harmonic component with amplitude of 0.2 V.

Table I shows the calculated phasors (peak values) of the fundamental components of the voltages in Fig. 19(a) and (b). These results confirm that the fundamental components of the PLL output voltages have unit amplitude, and are equally displaced.

The evaluation of the positive, negative, and zero sequence components of voltages in Table I results in Table II. The analysis shows that only unit amplitude, positive sequence appears at the output. Moreover, its phase angle is identical to the input

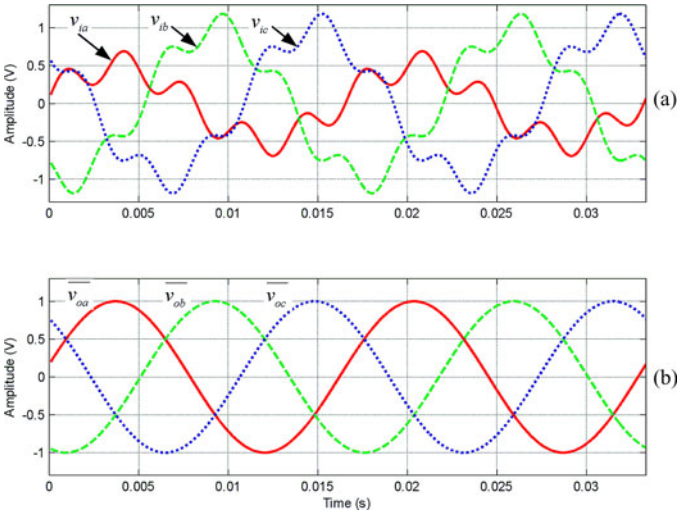

Fig. 19. Experimental results, three-phase SHE-PLL, and steady-state test. Grid with 0.2 V of fifth harmonic in all phases plus unbalanced fundamental voltages. (a) Input voltages $v_{ia} = 0.5$ V (solid line), $v_{ib} = 1$ V (dashed line), and $v_{ic} = 1$ V (dotted line). (b) PLL output voltages $\overline{v_{oa}}$ (solid line), $\overline{v_{ob}}$ (dashed line), and $\overline{v_{oc}}$ (dotted line).

TABLE II
PHASORS OF THE FUNDAMENTAL SYMMETRICAL COMPONENTS

SEQUENCE	INPUT VOLTAGES (PEAK VALUE - V)	OUTPUT VOLTAGES (PEAK VALUE - V)
POSITIVE	$0.83\angle 11.54°$	$1.00\angle 11.66$
NEGATIVE	$0.17\angle -168.44°$	$6\cdot10^{-4}\angle$-169.71
ZERO	$0.17\angle -168.44°$	$1\cdot10^{-4}\angle 63.43°$

TABLE III
THDV

THDV	INPUT VOLTAGES	OUTPUT VOLTAGES
A	40%	0.1607%
B	20%	0.0895%
C	20%	0.1280%

one, confirming that the three-phase SHE-PLL tracks the fundamental positive sequence of the input signal. The fundamental zero and negative sequences are canceled.

Table III presents the voltage total harmonic distortion (THDV) for the waveforms shown in Fig. 19(a) and (b), confirming that the harmonic distortion of the output voltages is low.

VIII. CONCLUSION

This paper presented an implementation of a single-phase PLL based on a square wave feedback signal with SHE, suitable for power system applications. The use of a squared wave VCO simplifies the implementation of PLLs in FPGAs, DSPs, or microcontrollers, because the number of multiplications is reduced and the sine and cosine calculations may be eliminated for some applications. The SHE-PLL also eliminates the steady-state phase error inherent to the square wave PLL when the input signal contains harmonics.

The classical, square wave, and SHE PLLs were simulated and implemented in an FPGA to generate experimental results which were compared. Steady state and transient tests for distorted grid voltages, voltage sags, outages and phase jumps, and frequency variation were performed to validate the algorithm. Tests have demonstrated that the dynamic response of the SHE-PLL and square wave PLL is similar to the classical PLL. Moreover, the simulation and experimental results have shown that the SHE-PLL with fixed window MAV filter is robust to grid faults including voltage sag with phase jump and frequency variation up to 6 Hz of nominal frequency.

The single-phase SHE-PLL was then extended to the three-phase case. The three-phase SHE-PLL substitutes the *abc*/$\alpha\beta$ block (Park transformation) of the well-known SRF-PLL by the sum of the products of the input voltages and their corresponding displaced SHE waveforms. Each of the three partial products is evaluated in the same way as proposed for the single-phase SHE-PLL, avoiding three multipliers. Experimental results have shown that the three-phase SHE-PLL tracks the fundamental positive sequence components of the input signal, with the advantage of reducing the complexity and the computational effort of the implementation.

APPENDIX

This appendix computes the output of the multiplier block $v_{\text{mult}} = v_o \cdot v_i$ for the classical and square wave PLLs.

A. Classical PLL

For v_i and v_o defined by (1) and (2), $v_{\text{mult}} = v_o \cdot v_i$ is given by (A.1) as shown at the bottom of the page.

Assuming $\omega_o \cong \omega_1$, the aforementioned equation can be simplified to (A.2) as shown at the top of the next page, where $\phi_d = \phi_1 - \phi_o$.

B. Square Wave PLL

For v_i and v_{os} defined by (1) and (4), $v_{\text{mult}} = v_{os} \cdot v_i$ is given by (A.3) as shown at the top of the next page.

Assuming that the PLL is locked, $\omega_o \cong \omega_1$, the aforementioned equation can be simplified to (A.4) as shown at top of the next page.

For a sinusoidal $v_i = A_1 \sin(\omega_1 t + \phi_1)$, (A.4) is rewritten as (A.5) as shown at the top of the next page.

$$v_{\text{mult}} = \frac{1}{2} \cdot \left\{ \begin{array}{l} A_1 \sin\left[(\omega_1 - \omega_o)\cdot t + \phi_1 - \phi_o\right] + A_1 \sin\left[(\omega_1 + \omega_o)\cdot t + \phi_1 + \phi_o\right] + \\ + A_2 \sin\left[(2\omega_1 - \omega_o)\cdot t + \phi_2 - \phi_o\right] + A_2 \sin\left[(2\omega_1 + \omega_o)\cdot t + \phi_2 + \phi_o\right] + \\ + A_3 \sin\left[(3\omega_1 - \omega_o)\cdot t + \phi_3 - \phi_o\right] + A_3 \sin\left[(3\omega_1 + \omega_o)\cdot t + \phi_3 + \phi_o\right] + \cdots \\ + A_k \sin\left[(k\omega_k - \omega_o)\cdot t + \phi_k - \phi_o\right] + A_k \sin\left[(k\omega_k + \omega_o)\cdot t + \phi_k - \phi_o\right] \end{array} \right\} \tag{A.1}$$

$$v_{\text{mult}} = \frac{1}{2} \cdot \left\{ \begin{array}{l} A_1 \sin\phi_d + A_1 \sin\left(2\omega_1 t + \phi_1 + \phi_o\right) + \\ + A_2 \sin\left(\omega_1 t + \phi_2 - \phi_o\right) + A_2 \sin\left(3\omega_1 t + \phi_2 + \phi_o\right) + \\ + A_3 \sin\left(2\omega_1 t + \phi_3 - \phi_o\right) + A_3 \sin\left(4\omega_1 t + \phi_3 + \phi_o\right) + \cdots \\ + A_k \sin\left[\left(k-1\right)\omega_1 t + \phi_k - \phi_o\right] + A_k \sin\left[\left(k+1\right)\omega_1 t + \phi_k + \phi_o\right] \end{array} \right\} \tag{A.2}$$

$$v_{\text{mult}} = \frac{2}{\pi} \cdot \left\{ \begin{array}{l} A_1 \sin\left[\left(\omega_1 - \omega_o\right) \cdot t + \phi_1 - \phi_o\right] + A_1 \sin\left[\left(\omega_1 + \omega_o\right) \cdot t + \phi_1 + \phi_o\right] + \\ + A_2 \sin\left[\left(2\omega_1 - \omega_o\right) \cdot t + \phi_2 - \phi_o\right] + A_2 \sin\left[\left(2\omega_1 + \omega_o\right) \cdot t + \phi_2 + \phi_o\right] + \\ + A_3 \sin\left[\left(3\omega_1 - \omega_o\right) \cdot t + \phi_3 - \phi_o\right] + A_3 \sin\left[\left(3\omega_1 + \omega_o\right) \cdot t + \phi_3 + \phi_o\right] + \\ - \dfrac{A_3}{3} \sin\left[\left(3\omega_1 - 3\omega_o\right) \cdot t + \phi_3 - 3\phi_o\right] - \\ \dfrac{A_1}{3} \sin\left[\left(3\omega_1 + 3\omega_o\right) \cdot t + \phi_3 + 3\phi_o\right] + \cdots \end{array} \right\}$$

$$v_{\text{mult}} = -\frac{2}{\pi} \cdot \left\{ \sum_{k=1}^{\infty} \sum_{j=1}^{\infty} \frac{(-1)^j A_k}{2j-1} \cdot \left\{ \begin{array}{l} \sin\left[k\omega_1 \cdot t - \left(2j-1\right)\omega_o t + \phi_k - \left(2j-1\right)\phi_o\right] + \\ + \sin\left[k\omega_1 \cdot t + \left(2j-1\right)\omega_o t + \phi_k + \left(2j-1\right)\phi_o\right] + \end{array} \right\} \right\} \tag{A.3}$$

$$v_{\text{mult}} = \frac{2}{\pi} \cdot \left\{ \begin{array}{l} A_1 \sin\phi_d + A_1 \sin\left(2\omega_1 t + \phi_1 + \phi_o\right) + \\ + A_2 \sin\left(\omega_1 t + \phi_2 - \phi_o\right) + A_2 \sin\left(3\omega_1 t + \phi_2 + \phi_o\right) + \\ + A_3 \sin\left(2\omega_1 t + \phi_3 - \phi_o\right) + A_3 \sin\left(4\omega_1 t + \phi_3 + \phi_o\right) + \\ - \dfrac{A_3}{3} \sin\left(\phi_3 - 3\phi_o\right) - \dfrac{A_1}{3} \sin\left(6\omega_1 t + \phi_3 + \phi_o\right) + \cdots \end{array} \right\}$$

$$v_{\text{mult}} = -\frac{2}{\pi} \cdot \left\{ \sum_{k=1}^{\infty} \sum_{j=1}^{\infty} \frac{(-1)^j A_k}{2j-1} \cdot \left\{ \begin{array}{l} \sin\left[\left(k-2j+1\right)\omega_1 t + \phi_k - \left(2j-1\right)\phi_o\right] + \\ + \sin\left[\left(k+2j-1\right)\omega_1 t + \phi_k + \left(2j-1\right)\phi_o\right] + \end{array} \right\} \right\} \tag{A.4}$$

$$v_{\text{mult}} = \frac{2}{\pi} \cdot \left\{ \begin{array}{l} A_1 \sin\phi_d + A_1 \sin\left(2\omega_1 t + \phi_1 + \phi_o\right) + \\ - \dfrac{A_1}{3} \sin\left(-2\omega_1 t + \phi_1 - 3\phi_o\right) - \dfrac{A_1}{3} \sin\left(4\omega_1 t + \phi_1 + 3\phi_o\right) + \cdots \end{array} \right\}$$

$$v_{\text{mult}} = -\frac{2}{\pi} \cdot \left\{ \sum_{j=1}^{\infty} \frac{(-1)^j A_1}{2j-1} \cdot \left\{ \begin{array}{l} \sin\left[\left(2-2j\right)\omega_1 \cdot t + \phi_1 - \left(2j-1\right)\phi_o\right] + \\ + \sin\left[2j\omega_1 \cdot t + \phi_1 + \left(2j-1\right)\phi_o\right] + \end{array} \right\} \right\} \tag{A.5}$$

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Naji Rajai Nasri Ama received the B.S. and the M.S. degrees in electrical engineering from the University of Technology, Baghdad, Iraq, in 2000 and 2003, respectively. He is currently working toward the Ph.D. degree at the Polytechnic School of the University of São Paulo, São Paulo, Brazil.

His research interests include grid synchronization methods, power electronics, digital signal processing, control systems, and grid-connected power converters.

Fernando Ortiz Martinz was born in São Paulo, Brazil. He received the B.S. degree in electrical engineering from the State University of Campinas, São Paulo, in 2003, and the M.S. degree from the Polytechnic School of the University of São Paulo (EPUSP), São Paulo, in 2007, where he is currently working toward the Ph.D. degree.

From 2003 to 2006, he was a Development Engineer with Dynamic Voltage Restorer and Flexible AC Transmission Systems His interests include modeling, control, and synchronization in power electronics, power quality, and grid-connected power converters.

Mr. Martinz is a member of the Brazilian Power Electronics Society.

Lourenço Matakas, Jr. received the B.S., M.S., and Ph.D. degrees in electrical engineering from the Escola Politécnica da Universidade de São Paulo, São Paulo, Brazil, in 1984, 1989, and 1998, respectively.

From 1984 to 1989, he was a Development Engineer with the Foundation of Engineering and Technology, University of São Paulo, São Paulo. From 1993 to 1995, he was a Research Assistant with the Department of Electrical Engineering, The University of Tokyo, Tokyo, Japan. In 1996, he joined the Pontifical Catholic University of São Paulo, São Paulo, leaving in 2011 as an Associate Professor. In 1996, he joined the Escola Politécnica da Universidade de São Paulo, where he is currently an Assistant Professor of power electronics. His research interests focus on static converters applied to grid and control of converters, phase-locked loops, and pulsewidth modulation strategies.

Dr. Matakas is a member of the Brazilian Power Electronics Society.

Fuad Kassab Junior (M'96) received the B.S., M.S., and Ph.D. degrees in electrical engineering from the Escola Politécnica da Universidade de São Paulo, São Paulo, Brazil, in 1985, 1989, and 1995, respectively, and the B.S. degree in physics from the Instituto de Física da Universidade de São Paulo, São Paulo, in 1985.

Since 1986, he has been a Consultant in industrial processes. In 1988, he joined the EscolaPolitécnica da Universidade de São Paulo, where he is currently an Assistant Professor in the Department of Telecommunication and Control Engineering. His research interests include control theory, modeling, and simulation of dynamic systems and optimization.