# Low-Power Adiabatic Sequential Circuits with Complementary Pass-Transistor Logic

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***Abstract*—This paper presents low-power complementary pass-transistor adiabatic logic (CPAL) using two-phase power-clocks instead of four-phase ones. The two-phase CPAL uses complementary pass-transistor logic for evaluation and transmission gates for energy-recovery. It is more suitable for design of flip-flops and sequential circuits, as it uses fewer transistors than conventional CMOS transmission gate-based implementations and other adiabatic logic circuits such as 2N-2N2P. Adiabatic flip-flops (*D*, *T* and *JK*) based on the two-phase CPAL are introduced. A practical sequential system realized with the proposed adiabatic flip-flops is demonstrated. SPICE simulations show that the two-phase CPAL flip-flops consume less power than 2N-2N2P and CMOS implementation.**

## I. INTRODUCTION

The classical approaches to achieve low-power design are to reduce the supply voltage, the loading capacitances of gates, and the switching activity. However, adiabatic logic, which utilizes ac power supplies to recycle the energy of node capacitances, is an attractive approach to obtain low power which conventional CMOS circuit can't reach [1-8]. Over the past decade, several adiabatic logic families were proposed and achieved considerable energy savings over conventional CMOS [1-4]. The previously proposed adiabatic circuits focused mainly on combination logic [3, 5]. In digital systems, however, flip-flops and sequential circuits cannot be also neglected [6].

Recently, we proposed the CPAL (complementary pass-transistor adiabatic logic) using four-phase power-clocks [7, 8]. CPAL circuits have more efficient energy transfer and recovery, because the non-adiabatic energy loss of output loads has been completely eliminated by using complementary pass-transistor logic for evaluation and transmission gates for energy-recovery. In this paper, we present the CPAL using two-phase power-clocks instead of four-phase power-clocks. The two-phase CPAL is more suitable for design of flip-flops and sequential circuits, because they use fewer transistors than conventional CMOS transmission gate-based implementations and other adiabatic logic circuits such as 2N-2N2P and PAL-2N [1, 6].

## II. TWO-PHASE CPAL

The basic structure of the CPAL buffer (inverter) is shown in Fig. 1, and its structure is the same as the four-phase CPAL [7, 8]. It is composed of two main parts: the logic function circuit and the load driven circuit. The logic circuit consists of four NMOS transistors (N1-N4) with complementary pass-transistor logic (CPL) that was proposed by K. Yano at al. [9]. The load driven circuit consists of a pair of cross-coupled CMOS transmission gates (N5, P1 and N6, P2). The CPAL gate is supplied by a single-phase power-clock. In this paper, cascaded CPAL gates are driven by two-phase power-clocks, as shown in Fig. 2.

The simulation waveforms of the CPAL buffer are illustrated in Fig. 3. By referring the schematic shown in Fig. 1 and the waveforms in Fig. 3, the operation of the two-phase CPAL buffer can be summarized as follows.

During the time interval $T_1$ and $T_2$, the voltage of the input INb is low and the voltage of the input IN goes high. Therefore, N1 and N3 are turned on. As the voltage of the input IN goes up, the voltage of the node X is charged to about $V_{DD} - V_{TN}$, where $V_{TN}$ is the threshold voltage of the NMOS transistor, while the node Y is clamped to ground.

During the time interval $T_3$ and $T_4$, as the voltage of the input IN falls, N1 and N2 are turned off. Thus, the voltage of the node X will keep its state because the node X is isolated.

During the period $T_5$, as the voltage of the clock $\phi$ goes up, the voltage of the node OUT begins to go high via N5. When the voltage of the OUT rises above $V_{TN}$, N8 will be turned on, and OUTb will be clamped to ground. When the voltage of the clock $\phi$ rises above $V_{TP}$, where $V_{TP}$ is the threshold voltage of the PMOS transistor, P1 will be turned on, so the node OUT is charged through transmission gate (N5, P1) without non-adiabatic loss.

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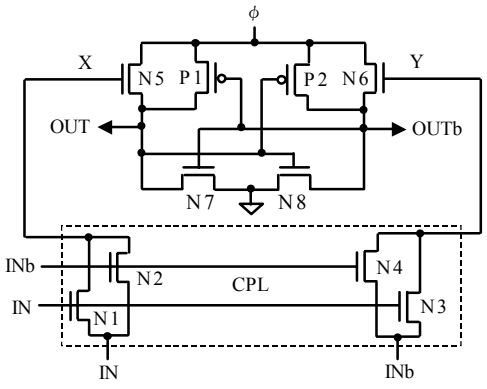


Figure 1. Schematic of CPAL buffer.

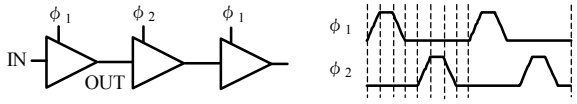


Figure 2. CPAL buffer chain and its two-phase power clock.

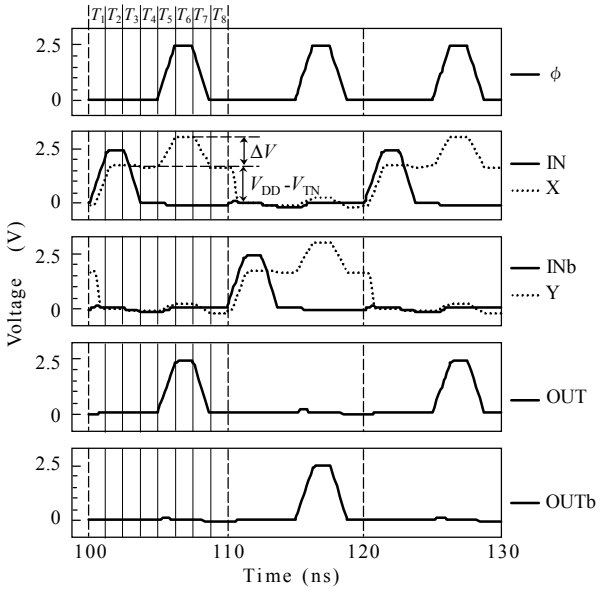


Figure 3. Simulation waveforms of the two-phase CPAL buffer.

During $T_6$, the voltage of the node OUT is the same as the clock $\phi$, while the node OUTb is still at ground. During $T_7$, as the voltage of the clock falls from $V_{DD}$ to ground, the charge on the node OUT is recovered through N5 and P1.

During the time interval $T_5$ - $T_7$, because N1 and N2 are turned off, the node X is in the high-impedance state. Therefore, the voltage of the node X can be bootstrapped to a higher level than $V_{DD} - V_{TN}$ due to the gate-to-channel capacitance of N5, as shown Fig. 3 [4, 7]. When $\phi$ rises from 0V to $V_{DD}$, the voltage of the node X is increased by $\Delta V$, which is expressed as

$$\Delta V = \frac{C_G}{C_{D1} + C_{D2} + C_W + C_G} V_{DD}, \quad (1)$$

where $C_G$=$WLC_{OX}$ is the gate-to-channel capacitance of N5 (or N6), $W$ and $L$ are the channel width and length of N5 (or N6), $C_{OX}$ is the gate-to-channel capacitance per unit area, $C_{D1}$ and $C_{D2}$ is the diffusion capacitance of N1 and N2, respectively, and $C_W$ represents the wiring capacitance. According to (1), when the channel width of N5 and N6 increases, the $\Delta V$ will be raised. High voltage $\Delta V$ can reduce the adiabatic loss because the turn-on resistances of the NMOS transistors (N5 and N6) are reduced [8, 10].

Energy dissipation of the two-phase CPAL circuits includes mainly two terms: full-adiabatic energy loss on output nodes and non-adiabatic energy loss on internal nodes, which is similar as the fore-phase CPAL [8]. The energy dissipation per cycle of the internal nodes X (or Y) can be written as

$$E_X = C_X(V_{DD} - V_{TN})V_{TN} + \tfrac{1}{2}C_X(V_{DD} - V_{TN})^2, \quad (2)$$

where $C_X$= $C_{D1}$+$C_{D2}$+$C_{G7}$ +$WLC_{OX}$ is the capacitance of the node X, and $W$ and $L$ are the channel width and length of N5 (or N6). Full-adiabatic energy loss on output nodes can be represented as

$$E_{output} = 2(\frac{RC_L}{T})C_L V_{DD}^2, \quad (3)$$

where $C_L$ is the load capacitance of the CPAL buffer, $T$ is the transition time of the power-clock, and $R$ is the turn-on resistance of the transmission gate.

Fig. 4 shows the energy consumption comparison of the 2N-2N2P [1] and CPAL buffer using 0.25μm TSMC process. We used the sizes of $W/L$=1.08μm/0.24μm for PMOS transistors and $W/L$=0.36μm/0.24μm for NMOS transistors in all circuits, except for N5 and N6 in the CPAL, the size of which is 1.08μm/0.24μm. Compared to 2N-2N2P, CPAL dissipates less energy and is insensitive to load capacitance, because the capacitance of the internal nodes is much smaller than that of output nodes. The simulations also show that the energy loss of CPAL is much lower than 2N-2N2P at all operation frequencies, because the turn-on resistance of the transmission gates of CPAL is smaller than that of the PMOS transistors of 2N-2N2P. Because of shorter transition time, the energy loss of the two-phase CPAL is slightly larger than the four-phase CPAL [7, 8].

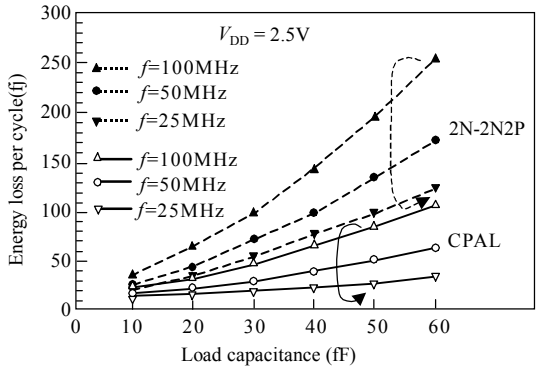


Figure 4. Energy consumption of the CPAL and 2N-2N2P buffers.

## III. ADIABATIC FLIP-FLOPS & SEQUENTIAL CIRCUITS

In adiabatic circuits, the output signal of the buffer (inverter) is set to 0V, when the power-clock falls from the peak voltage to ground. In this way, a signal can never be stored. Therefore, adiabatic flip-flops can't be built by simply using conventional methods. The adiabatic flip-flop can be structured using a cascaded buffer chain [6]. The adiabatic *D* flip-flop based on the two-phase CPAL is shown in Fig. 5(a). Because of the fact that the output of the two-phase CPAL buffer follows the input with a 180° phase lag, the input *D* is just shifted to the output terminal *Q* through the two-stage CPAL buffer chain by one clock period. Thus, the function of Fig. 5(a) is corresponding to a traditional *D* flip-flop.

Assume that the present state of flip-flops is *Q*. Then, next state $Q^+$ of the *T* and *JK* flip-flops can be written as $Q^+ = T \oplus Q$ and $Q^+ = J\overline{Q} + \overline{K}Q$, respectively. Therefore, the *T* and *JK* flip-flops can be realized by using the XOR and multiplexer to replace the first-stage CPAL buffer in the adiabatic *D* flip-flop, respectively, as shown in Fig. 5(b) and Fig. 5(c) [10].

The CPAL logic gates can be easily implemented by using the complementary pass-transistor logic (CPL) to replace the transistors (N1-N4) of the CPAL buffer [9, 10]. Fig. 6 shows the AND/NAND gate, OR/NOR gate, XOR/XNOR gate, and multiplexer with CPAL circuit topology. In Fig. 6, only the N-logic input blocks are shown and the other transistors (P1, P2, and N5-N8) are omitted for simplicity. All basic gates, such as inverter, AND, OR, multiplexer, and XOR, use the same topology, and only inputs are permutated. Therefore, the design is very modular and simple [9].

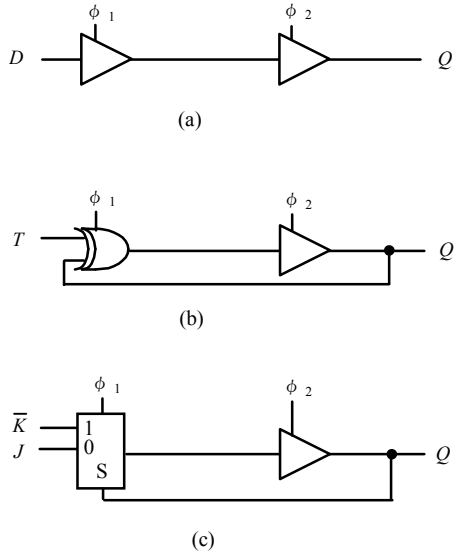


Figure 5. Adiabatic flip-flops based on two-phase CPAL: (a) *D* flip-flop, (b) *T* flip-flop, and (c) *JK* flip-flop.

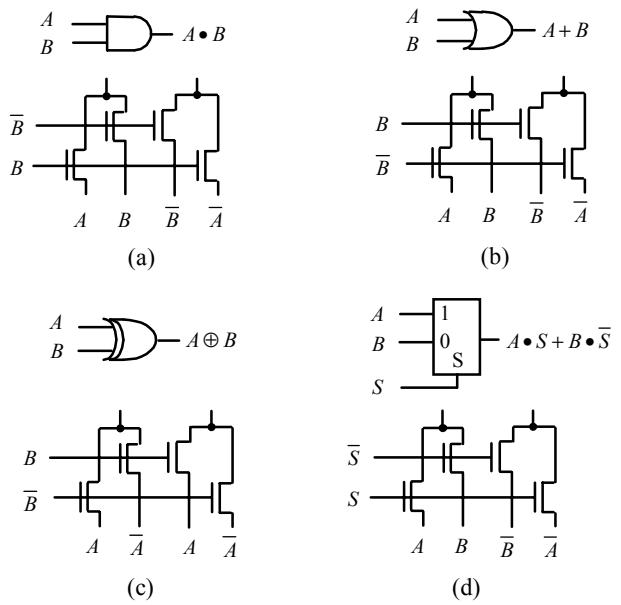


Figure 6. CPAL gates: (a) AND, (b) OR, (c) XOR, and (d) multiplexer.

The trapezoidal power-clock is easy to analyze but difficult to generate. As general *LC* circuits can produce sinusoidal power-clocks, it has more practical significance. Simulated waveforms of the CPAL *J-K* flip-flop are showed in Fig. 7 using two-phase non-overlap sinusoidal power-clocks [11-12]. It is seen that its logic function is corresponding to a traditional *J-K* flip-flop. It should be pointed that the two-phase power-clocks must be almost-non-overlap for proper operation of two-phase CPAL.

Complex sequential circuits can be realized using the proposed two-phase CPAL gates and flip-flops. An adiabatic BCD code up-counter is shown in Fig. 8, which consists of four flip-flops and a carry circuit. Each flip-flop consists of two-stage CPAL circuits, and some of them are used to realize the combinatorial logic function. The transition function of each flip-flop can be expressed as: $Q_3^+ = (Q_1 \cdot Q_2)Q_0 + Q_3\overline{Q}_0$, $Q_2^+ = (Q_0 \cdot Q_1) \oplus Q_2$, $Q_1^+ = (Q_0 \oplus Q_1)\overline{Q}_3$, and $Q_0^+ = \overline{Q}_0$ [10]. Therefore, this is an 8421 BCD code up-counter.

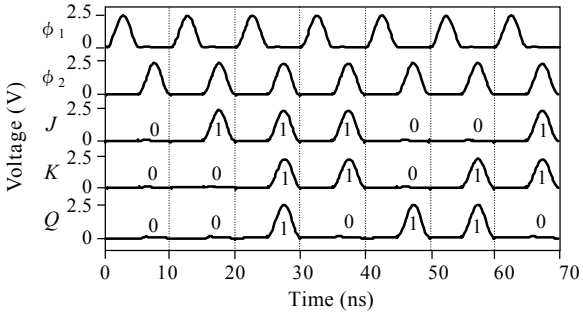


Figure 7. Simulated waveforms of the *J-K* flip-flop

The SPICE simulation is also carried out for the adiabatic counter, and its waveforms are showed in Fig. 9. For comparison, the two other adiabatic *D* flip-flops based on PAL-2N [6] and 2N-2N2P are simulated using the same process parameter. The simulation results show that the proposed CPAL D flip-flop consumes only 35% of the dissipated energy of the 2N-2N2P one and attains energy savings of 42% as compared to PAL-2N implementation at 100MHz. The conventional CMOS transmission gate-based D flip-flop adopting DC power supply, which consists of four CMOS transmission gates and four CMOS inverters, is also simulated [13]. The two-phase CPAL *D* flip-flop is about 3 to 6 times less dissipative than the static CMOS flip-flop from 50 to 200Mhz.

The transistor count of the two-phase CPAL flip-flops and counters is compared against PAL-2N, 2N-2N2P, and conventional CMOS transmission gate-based (CMOS TG) circuits [1, 6, 13], and is tabulated in Table 1.

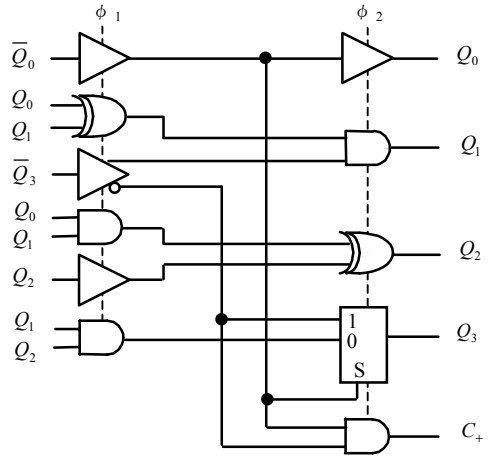


Figure 8. Adiabatic 8421 BCD code up-counter.

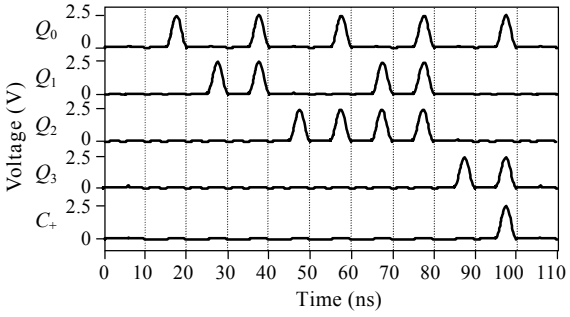


Figure 9. Simulated waveforms of the adiabatic counter

TABLE I. COMPARISON OF TRANSISTOR COUNT

| | ***D* flip-flop** | ***J-K* flip-flop** | **Decimal counter** |
|---|---|---|---|
| **Two-phase CPAL** | 20 | 20 | 110 |
| **PAL-2N/2N-2N2P** | 24 | 28 | 140 |
| **CMOS TG** | 16 | 28 | 124 |

## IV. CONCLUSIONS

This paper presents CPAL circuits using two-phase AC power supply. Moreover, this paper also explores the design of adiabatic sequential circuits. The energy dissipation of the adiabatic flip-flops based on the two-phase CPAL is very low. Because of two-phase clock scheme, the proposed CPAL counter uses fewer transistors than the other adiabatic logic and conventional CMOS transmission gate-based implementations. It should be pointed that the two-phase power-clocks must be non-overlap for proper operation of two-phase CPAL. Although the CPAL circuits are used for the design of an 8421 BCD code up-counter here, the other adiabatic sequential circuits can be also realized.

## ACKNOWLEDGMENT

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