Carbon Nanotube Field-Effect Transistors for High-Performance Digital Circuits—DC Analysis and Modeling Toward Optimum Transistor Structure

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***Abstract*—Scaling of silicon technology continues while a research has started in other novel materials for future technology generations beyond year 2015. Carbon nanotubes (CNTs) with their excellent carrier mobility are a promising candidate. The authors investigated different CNT-based field effect transistors (CNFETs) for an optimal switch. Schottky-barrier (SB) CNFETs, MOS CNFETs, and state-of-the-art Si MOSFETs were systematically compared from a circuit/system design perspective. The authors have performed a dc analysis and determined how noise margin and voltage swing vary as a function of tube diameter and power-supply voltage. The dc analysis of single-tube SB CNFET transistors revealed that the optimum CNT diameter for achieving the best $I_{\rm ON}$-to-$I_{\rm OFF}$ ratio while maintaining a good noise margin is about 1 to 1.5 nm. Despite several serious technological barriers and challenges, CNTs show a potential for future high-performance devices as they are being researched.**

***Index Terms*—Carbon nanotube field effect transistors (CNFETs), dc analysis, high-performance-circuits, modeling, noise margin, voltage swing.**

I. Introduction

TECHNOLOGYscaling of the bulk Si transistor over the last three decades has not only produced ultrahigh-performance digital circuits but has also sustained Moore's Law. However, ramifications of "short channel effects" such as exponential increase in leakage current and large parameter variations [1] have created challenges in design [2] as well as testing [3] of ICs and have rendered scaling of silicon more difficult and expensive than ever before. In spite of all the problems, scaling of silicon technology is expected to continue while researchers are investigating nonplanar transistor structures such as FinFETs [4] and Trigates [5] and looking at means to improve mobility by strain [6] or compound semiconductors [7]. More futuristic research has also started in earnest to consider alternative devices and circuit architecture in a sub-10-nm transistor era in approximately a post-2015 timeframe. Several futuristic (and revolutionary) devices such as carbon nanotube field effect transistors (CNFETs), molecular diodes,

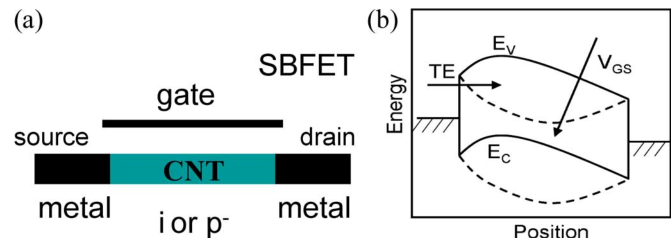

Fig. 1. SB CNFET showing (a) the schematic and (b) the energy band diagram.

and quantum cellular automata have caught the attention of device/circuit and system engineers worldwide. While the evolutionary devices such as nonplanar Si technology and trigate transistors as well as straining promise to mitigate some of the problems associated with bulk Si MOSFETs, the quest for new material continues in order to realize faster binary switches. Of all the different materials that are being investigated, CNTs [8], [9] appear to be the most promising in their high intrinsic carrier mobility despite numerous material research questions and yield concerns.

CNTs are sheets of graphene rolled into tubes. Depending on their chirality (i.e., the direction in which the graphene sheet is rolled), the single-walled CNTs can either be metallic or semiconducting. Semiconducting nanotubes have attracted widespread attention of electron device and circuit designers as possible channel material for high-performance transistors [9], [10]. The performance of CNFETs is advancing rapidly. Simple circuit applications such as inverter, basic logic gates, and simple ring oscillators [11] have already been demonstrated by several groups [12] as a starting point, and research in circuit applications, modeling, and design optimizations continues.

Let us discuss the different types of CNT devices and transistors that are being currently studied. One of the devices is a tunneling device that works on the principle of direct tunneling through a Schottky barrier (SB) at the source-channel junction [13]. This transistor is shown in Fig. 1, and we refer to it as SB CNFET. The barrier width is modulated by the application of gate voltage, and thus, the transconductance of the device is dependent on the gate voltage [14]–[17]. These devices are fabricated using direct contact of the metal with the semiconducting nanotube, and consequently, they have an SB at the metal nanotube junction [16], [17]. Two important aspects of these nanotube transistors are worth mentioning. First, the energy barrier at the SB severely limits the transconductance of the nanotube transistors in the ON-state and reduces the current delivery

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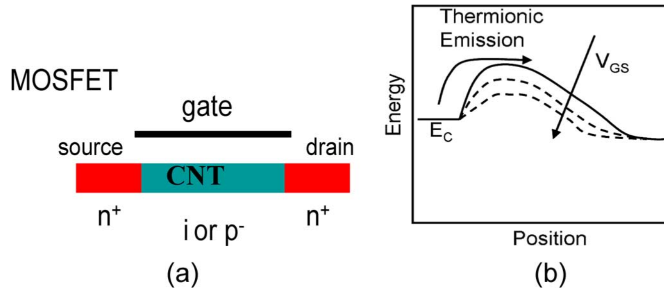


Fig. 2. MOS CNFET showing (a) the schematic and (b) the energy band diagram.

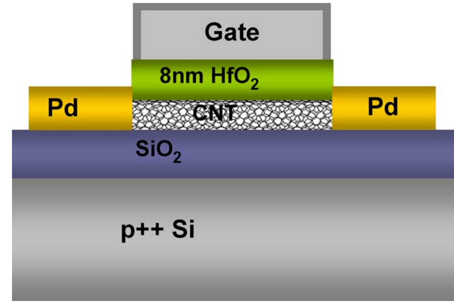


Fig. 3. Schematic diagram of the top-gated SB CNFET with self-aligned gate structure. This device has been reported in [17].

capability (transistor $I_{\rm ON}$)—a key metric to transistor performance. Second, SB CNFETs exhibit strong ambipolar characteristics in their current–voltage (I–V) behavior, and this constraints the use of these transistors in conventional CMOS logic families.

To overcome these handicaps associated with the SB CNFETs, there have been attempts to develop CNFETs which would behave like normal MOSFETs [18]–[20]. Potassium-doped source and drain regions have recently been demonstrated, and the field-effect behavior has been experimentally shown [19]. More recently, a tunable CNFET with electrostatic doping (also referred to as electrical doping) has been demonstrated in [20]. This MOSFET-like CNFET (Fig. 2) operates on the principle of barrier-height modulation by application of the gate potential. Guo *et al.* [21] have presented numerical studies on such MOS CNFETs that show: 1) The MOSFET-like CNFETs have unipolar characteristics unlike SB CNFETs' ambipolar conduction. 2) The absence of SB reduces the OFF-leakage current. 3) They are more scalable compared to their SB counterparts. 4) In the ON-state, the source-to-channel junction has no SB, and hence, the device demonstrates significantly higher "ON" current.

A third variety of CNFETs, namely, the band-to-band tunneling FETs (BTBT CNFETs) have also been demonstrated both experimentally [22] and in theory [23]. These devices have super cutoff characteristics (subthreshold slopes less than 60 mV/dec), but they suffer from low ON-currents. They can potentially be used for ultralow power applications. Since we are interested in high-performance devices, we will not discuss the BTBT devices here in this paper.

Although MOS CNFETs should ideally be the best devices to work with and researchers are trying to realize them [19], [20], the experimentally demonstrated devices suffer from air instability (due to Potassium K-doping [19]) and lower ON-currents (compared to the SB FETs). Nevertheless, recently published results [19], [20] do show the possibility of realizing higher performance MOS CNFETs in future. On the other hand, SB CNFETs with well-defined geometries, self-aligned gate stacks, and currents as high as 25-μA per nanotube [17] have already been reported. This "state-of-the-art" high-performance SB CNFET (Fig. 3) has high current per tube that makes it interesting to assess the performance of CNFET-based digital circuits.

In this paper, the following will be addressed.

1) Motivate our research by performing a simple calculation to determine why a CNFET technology can potentially improve upon the performance of a scaled silicon technology.
2) We briefly discuss our simulation methodology and environment incorporating an atomistic device description and a lookup-table-based circuit solver.
3) We study transistor parameters and device $I_{\rm ON}$ versus $I_{\rm OFF}$ characteristics to point toward an optimum transistor structure fabricated on this new material system.
4) Finally, we integrate the role of circuits and systems into our analysis by performing dc circuit simulations to identify desired tube diameters and operating power-supply voltages for our CNT-based circuits.
5) We will cover ac transient analysis, performance versus power tradeoffs, and scalability issues in details in the second part of this paper [35].

The challenges in designing an optimal SB CNFET are different from that of a Si transistor. The design of SB CNFETs needs special attention due to the ambipolar nature of conduction. Although the focus of this paper will be on SB CNFETs, we will discuss MOS CNFETs as and when necessary for comparison.

II. Potential of CNFETs: Implications for Technology Scaling

Before going into the details of CNFET technology and its possible optimization for digital circuits, it will be worthwhile to carry out a simple calculation to determine why a CNFET technology can potentially improve upon the performance of a scaled silicon technology. Being a quasi-one-dimensional (1-D) conductor, a CNT channel resistance is limited by the fundamental quantum resistance (R_Q) of 6.5-KΩ per tube [8]. If we could deliver to this quantum resistance (ignoring metallic versus semiconducting behavior for the moment) at 1-V operating voltage, we should get about 150 μA/nanotube. With all its nonidealities like poor contacts, scattering as well as existence of tunneling barriers, the state-of-the-art CNFETs can deliver $\sim$20 μA/nanotube at $\sim$1 V [17]. Consider a transistor total width of 1 μm and assume we are packing nanotubes in an array with spacing of one diameter apart. With this internanotube spacing of $2d$ (pitch of $2d$), where d is the diameter of CNT, we can pack as many as 500 nanotubes (of $d = 1$ nm) provided the technology, which allows us to make such a well-defined array of tubes (no such array has been experimentally demonstrated yet). This corresponds to a current of $\sim$10 mA/μm which is almost 10$\times$ higher than the corresponding silicon transistor

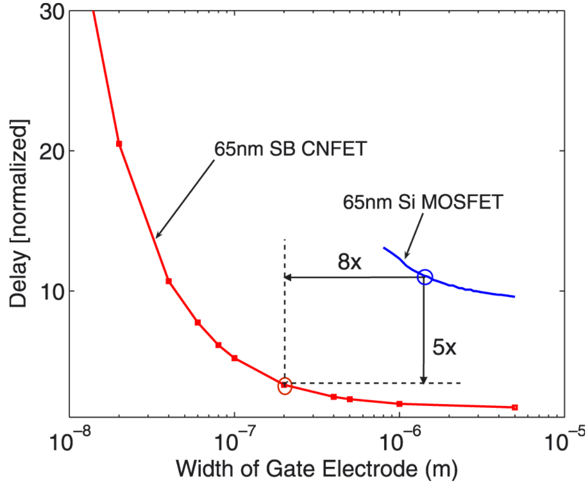


Fig. 4. Normalized delay versus size of a ring oscillator for a 65-nm bulk Si transistor. Using the same interconnect parasitics, a 65-nm CNT transistor has also been simulated. Note that due to the higher current density, a smaller size (for iso-delay) or smaller delay (for iso-size) can be achieved. For typical sizing, 8× area improvement and 5× delay reduction are obtained.

(assuming that Si gives us about 1 mA/μm, although we know that utilizing strain Si can improve this value). The capacitance per nanotube is ∼2–5 aF, which corresponds to ∼1 fF/μm (which is in the same order as a silicon transistor). This means that the 1-D CNT technologies can potentially deliver a much higher current in the same area and for identical gate capacitance. The increase in current density leads to lower delay and higher integration density. Consider a ring oscillator where an inverter is driving an identical inverter. Fig. 4 illustrates how the delay changes with the gate electrode width of the transistor. For CNFETs, we have packed CNTs in parallel with internanotube spacing of 2 nm (i.e., pitch is twice the diameter). The parasitic capacitances corresponding to the 65-nm technology node have been estimated and used in Fig. 4. Note that the use of CNTs as channel materials leads to higher current density which in turn leads to smaller widths (for a fixed iso-delay) and smaller delays (for a fixed width). From Fig. 4, consider the points on the two curves (denoted by circles). These points represent effective tradeoffs between the area and delay and hence can be considered as an optimal width and an optimal delay for the given technology. We can either realize a 5× improvement in delay or an 8× improvement in area in case of CNT technology as compared to the 65-nm Si technology. This simple calculation motivates the fact that the use of such 1-D conductor can potentially increase both the frequency of operation as well as allow higher integration density. In the second part of this paper [35], we will discuss the implications for Moore's Law and scalability in more details.

III. Simulation Strategy

Transistor device simulations of both the MOS CNFETs as well as the SB CNFETs have been carried out in a manner described by Guo *et al.* in [24] and [25]. We have considered three-dimensional (3-D) electrostatics in this paper. The accuracy of the device-simulation methodology has been verified by the authors in [24] through a comparison with the experimental data obtained from [17]. The close match between the theory and experiments makes it possible to use the same device strategy to make further estimations and predictions regarding circuit/system level performance of scaled CNFETs.

The detailed principle of the device simulation for the CNFETs can be found in [24] and will be mentioned here briefly for the convenience of the readers. The studied CNFETs have a self-aligned top-gate structure (Fig. 3). CNFETs are simulated by solving the Schrödinger equation using the nonequilibrium Green's function (NEGF) formalism [24], [27], self-consistently with the Poisson equation (3-D electrostatics). Ballistic transport in the CNT channel has been assumed [25]. An atomistic description of the nanotube using a tight binding Hamiltonian with an atomistic (p_z orbital) basis was employed [24]. The charge density was computed by integrating the local density of states (LDOS) over energy [25]

$$\begin{aligned} Q(z) = (-e)\int_{-\infty}^{+\infty} dE \cdot \operatorname{sgn}\left[E - E_N(z)\right] \\ \times \Big\{ D_S(E,z) f(\operatorname{sgn}[E - E_N(z)](E - E_{\rm FS})) \\ + D_D(E,z) f(\operatorname{sgn}\left[E - E_N(z)\right] \\ \times (E - E_{\rm FD})) \Big\}. \end{aligned} \tag{1}$$

Here, e is the electron charge, $\operatorname{sgn}(E)$ is the sign function, $E_{{\rm FS},D}$ is the source (drain) Fermi level, $E_N(z)$ is the charge neutrality level, and $D_{S,D}(E,z)$ is the LDOS due to the source (drain) contact, $D_{S,D} = G\Gamma_{S,D}G^+$, where $G = [(E + i0^+)I - H - \Sigma_S - \Sigma_D]^{-1}$ is the retarded Green's function, H is the device Hamiltonian, $\Sigma_{S,D}$ is the source/drain self-energy, and $\Gamma_{S,D} = i(\Sigma_{S,D} - \Sigma_{S,D}^+)$ is the source/drain broadening function [26], [27].

Along with the NEGF transport equation, we iteratively solve a 3-D Poisson equation to obtain the self-consistent electrostatic potential [27]. Once the self-consistent potential profile is obtained, the source–drain current was computed by Landauer's equation:

$$I = \frac{4e}{h}\int dE \cdot T(E)\left[f(E - E_{\rm FS}) - f(E - E_{\rm FD})\right] \tag{2}$$

where $T(E) = \operatorname{trace}(\Gamma_S G \Gamma_D G^+)$ is the source–drain transmission [27], [28].

The difference in the simulation strategy between the MOS and SB CNFETs lies in the treatment of the source–drain regions. For SB CNFETs (with metallic source/drain), a phenomenological treatment of the metal contact is used with the metal-CNT SB height [29]. A coupling parameter which controls the metal-induced gap states is an input parameter [25]. The simulation methodology for MOS CNFETs is in essence similar to that of SB CNFETs. The self-energies of the source and the drain are derived from the real-space Hamiltonian of the doped CNT in a manner described in [24].

Note that since the electron-hole recombination length is about 2 μm [30] and much longer than the channel length, electron-hole recombination is not a concern. The modeled CNFETs deliver a near ballistic dc ON-current [31] with essentially no phonon scattering in the channels.

In this paper, we are interested in the circuit behavior of the scaled SB CNFETs. For the rest of this paper, we have used a 2-nm thick HfO_2 high-K dielectric ($K = 16$) while we investigated CNTs with the following chiral vectors (8,0), (13,0), (20,0), and (26,0). All of them are semiconducting and have the following diameters (d) and bandgaps: 1) 0.6 nm (referred to as narrow) and 1.4 eV; 2) 1.0 nm and 0.84 eV; 3) 1.56 nm and 0.54 eV; and 4) 2 nm (referred to as wide) and 0.42 eV. The transistor channel length is assumed to be 20 nm, unless otherwise mentioned.

The device data (I–V and C–V) have been tabulated and used in a circuit-simulation environment to simulate circuits and systems. Hence, the numerical study presented in this paper involves a detailed atomistic description of the device and circuit-simulation tools to estimate the performance of different flavors of CNFETs.

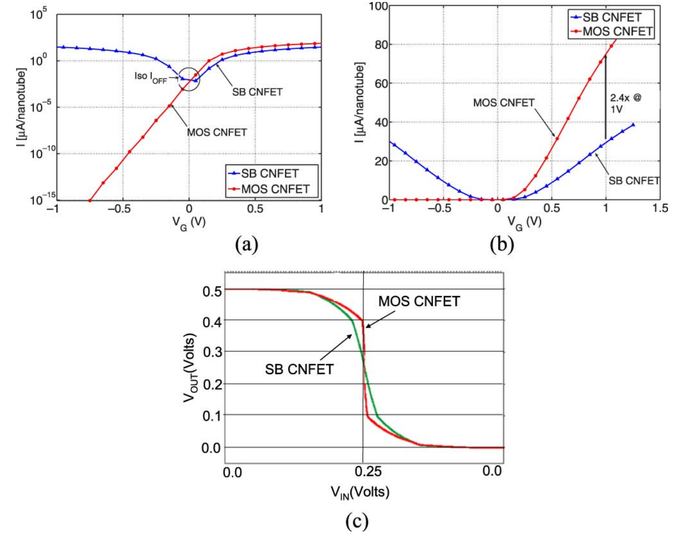


Fig. 5. (a) and (b) Comparison of the I–V characteristics of an SB CNFET and a MOS CNFET. (c) VTC of an SB and MOS CNFET, showing that the MOS CNFET has a sharper VTC.

IV. Toward an Optimal CNFET—DC Simulations, Noise Margin, and Voltage Swing

The challenges in designing an optimal SB CNFET are different from that of a Si transistor. The design of SB CNFETs needs special attention due to the ambipolar nature of conduction [31], [32]. SB CNFETs show strong ambipolar conduction due mainly to the fact that: 1) The tunneling barrier is very thin after the gate oxide thickness is reduced. (An electrostatic calculation shows that the SB thickness is roughly proportional to the gate oxide thickness [21].) 2) The holes at the valence band edge have strong wave behavior due to the small effective mass [25]. The minimal leakage current is achieved when the electron and hole currents are equal in SB CNFETs.

The most important thing to note here is that a zero bias at the gate of the SB CNFET ($V_{\mathrm{GS}} = 0$) would not turn the transistor off as it is shown by the I_D–V_G characteristics of the devices. Similarly a high potential at the gate of the P-type SB CNFET would be as ineffective in turning the transistor OFF. The problem of ambipolar conduction has been addressed in [16] and discussed in [33]. As a result, normal operation of digital gates, say, a simple inverter would require a change in the flatband voltage of the SB CNFETs, such that the minimum leakage point corresponds to the zero-bias condition ($V_{\mathrm{GS}} = 0$). Hence, for a midgap material for the source and the drain, where $\phi_p = \phi_n = eV_D/2$, the flatband voltage has to be $V_{\mathrm{DD}}/2$, where V_{DD} is the power-supply voltage. It has been proposed in [14] that a good SB pMOS should have a source/drain material whose Fermi level is aligned to the valence band (E_V). Similarly, a good SB nMOS should have a source/drain material aligned to conduction band (E_c). This indeed suppresses the ambipolar conduction and makes hole (pMOS) or electron (nMOS) conduction more favorable. Nevertheless, the device still shows a considerable ambipolar conduction, and care should be taken to design the flatband condition, such that the point of current minima coincides with $V_{\mathrm{GS}} = 0$ (@$V_{\mathrm{DS}} = V_{\mathrm{DD}}$). In the rest of this paper, we have ensured that the V_{FB} is such that $I_{\mathrm{DS}} = I_{\mathrm{MIN}}$ @$V_{\mathrm{GS}} = 0$ and $V_{\mathrm{DS}} = V_{\mathrm{DD}}$. In MOS CNFETs, however, the conduction is unipolar and the design of flatband voltage is similar to that of a Si MOSFET. To summarize, the flatband voltage (or, the corresponding threshold voltage) has to be determined in the following manner.

1) For MOS CNFETs, the V_{FB} can be fixed for a target ON-current or a target OFF-current (as in silicon MOSFETs).
2) For SB CNFETs, the V_{FB} has to be chosen such that the current minimum occurs at $V_{\mathrm{GS}} = 0$ and $V_{\mathrm{DS}} = V_{\mathrm{DD}}$. This current minimum is the OFF-current of the device. Thus, separate control of ON-current or the threshold voltage is not possible.

Midgap SB CNFETs have been demonstrated in [30] and they show strong ambipolar conduction. It can be noted that such a device benefits from the fact that the same material can be used as the source/drain material for both the pMOS and the nMOS. However, to improve the performance of SB CNFETs, p-FETs with the source/drain Fermi level aligned to E_V have also been investigated [14]. In our numerical study, we will assume that an nMOS counterpart of the p-type SB CNFET is achievable by using a suitable source/drain material. We will refer to these two types of CNFETs as midgap SB CNFETs and band-edge SB CNFETs, respectively. However, unless otherwise mentioned, by SB CNFETs, we will mean midgap SB CNFETs.

At this point, we will compare the dc characteristics of a MOS CNFET and an SB CNFET. Fig. 5 illustrates the I–V characteristics of an SB CNFET and MOS CNFET. Both devices have a CNT diameter of 1 nm and a top gate with 2-nm HfO_2 dielectric thickness. The SB CNFET has metallic source drain with midgap work functions. The V_{FB} of the MOS CNFET has been adjusted for identical OFF-currents. Note that the ON-current of the MOS CNFET is 2.4× higher than the SB CNFET. Fig. 5(c) illustrates the voltage transfer characteristics (VTC) of an inverter made with MOS CNFETs and SB CNFETs. Owing to the higher transconductance gain of MOS CNFETs, we observe a sharper VTC for MOS CNFETs.

The diameter (since, it is inversely proportional to the bandgap) plays a major role in determining the SB height. The I_{ON} and the I_{OFF} are intrinsically tied to the SB height and

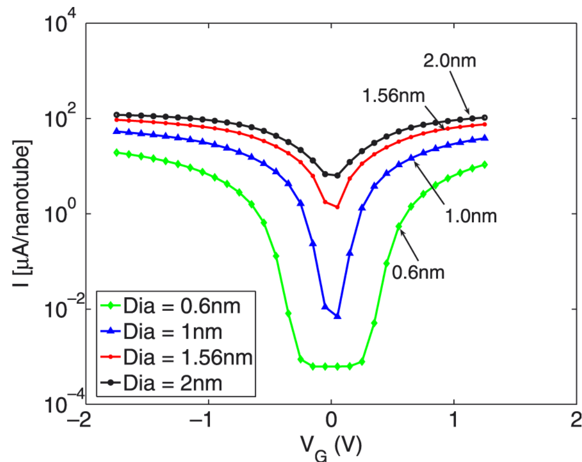
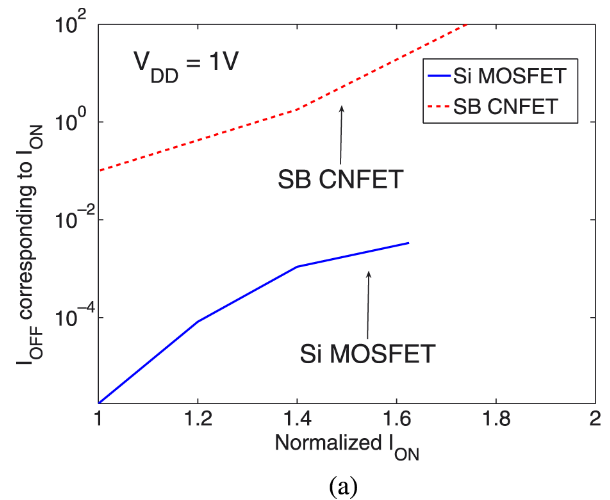


Fig. 6. I_{DS}–V_{GS} characteristics of an SB CNFET with varying CNT diameters. Note that $V_{DD} = 1.0$ V and the gate dielectric is 2 nm of HfO_2. It can be noted that the I_{OFF} increases exponentially and the I_{ON} increases linearly with diameter.

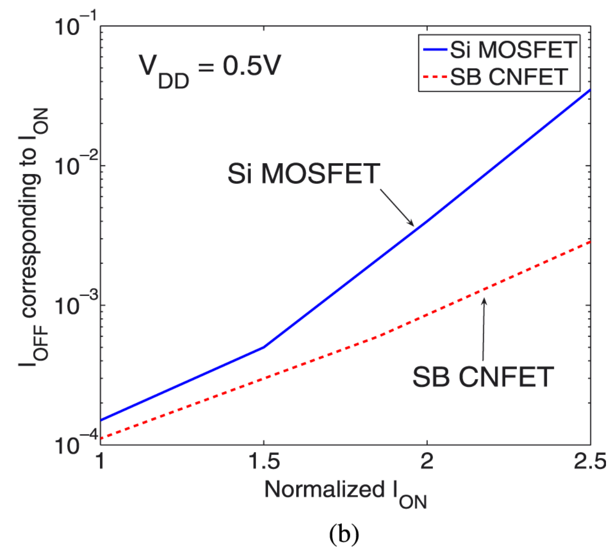
hence to the diameter. Fig. 6 illustrates the I_{DS}–V_{GS} characteristics of several SB CNFETs with varying diameters. It can be noted that a narrow diameter (a higher band-gap) produces a higher SB, resulting in an exponentially lower I_{ON} and also lower I_{OFF}. The wider diameter-SB CNFETs (∼2 nm) have significantly higher I_{ON} at the cost of very high I_{OFF} and poor I_{ON}–I_{OFF} ratio. The role of V_{DD} on the I_{OFF} is significant. In nanoscale MOSFETs, the power supply affects the I_{OFF} through drain-induced barrier lowering and hence has a second-order effect. In SB CNFETs, the OFF-current is exponentially proportional to the V_{DD} through 1-D electrostatics.

In this context, it is worthwhile to investigate the relationship between I_{ON} and I_{OFF} of an SB CNFET and compare it to Si MOSFET. The I_{ON}–I_{OFF} relationship is critical in device engineering and development of FET technologies. The slope determines how one can trade off leakage for performance and I_{ON}. Also, we can compare various technology options' performance by comparing I_{ON} at iso-I_{OFF}. In our study, the I_{OFF} corresponding to a normalized value of I_{ON} has been illustrated in Fig. 7. The different values of I_{ON} and I_{OFF} for the SB CNFET are obtained by varying the CNFET diameter, while for the MOSFET, the channel doping has been changed. The data in Fig. 7(a) show that SB transistors are not suited for operating at large supply voltages. The leakage is very high and it even prevents us from comparing I_{ON} at iso-I_{OFF}. However, it can be noted that for iso-I_{ON} conditions, the OFF-current in SB CNFETs is prohibitively large at high V_{DD} (= 1 V, in our simulations). On the contrary, for low supply bias conditions, i.e. $V_{DD} = 0.5$ V, SB CNFETs show lower I_{OFF} for iso-I_{ON} conditions. In addition, they provide higher performance at iso-I_{OFF}. The slope of Fig. 7(b) shows that SB CNFETs have very favorable tradeoff in I_{ON}–I_{OFF}. This makes it apparent that the true potential of SB CNFETs would be in low V_{DD} applications. Note further that the slope of the I_{ON}–I_{OFF} curve is different for the SB CNFETs, although it also gives an exponential rise in OFF-current for a linear increase in ON-current (like Si MOSFETs).

Hence, both diameter and V_{DD} play a role on the dc voltage swing and noise margin [34] of an inverter made of SB CNFETs. Fig. 8(a) illustrates the output voltage swing of an inverter for different V_{DD}s and varying diameters. Since the voltage swing depends on the ratio of I_{ON} and I_{OFF}, we observe that the voltage swing degrades at high V_{DD}s (> 700 mV) and also with larger CNT diameter. Fig. 8(b) shows the variation of noise margin of the inverter with V_{DD} and diameter. An ideal inverter should have a noise margin of 0.5 V_{DD}. However, larger CNT diameters and high V_{DD}s result in poor noise margins (as low as 0.2 V_{DD}). From the dc simulations, it becomes clear that large CNT diameters (i.e., low SB) and high V_{DD}s have prohibitively large leakage, resulting in low noise margins and voltage swings. Hence, for SB CNFET-based digital circuit design, large diameters or high V_{DD}s are not desirable. MOS CNFETs, on the contrary, do not show ambipolar conduction, and we do not observe a first-order V_{DD} dependence of I_{OFF}. By properly choosing the flatband voltage, MOS CNFETs can be designed to have rail-to-rail voltage swing and noise margins as high as 0.4 V_{DD}. Thus, we only need to worry about flatband and threshold-voltage settings.



(a)



(b)

Fig. 7. I_{ON} versus I_{OFF} of a Si MOSFET and an SB CNFET (for the 45-nm technology node, with an effective channel length of ∼20 nm) for (a) $V_{DD} = 1$ V and (b) $V_{DD} = 0.5$ V. The different I_{ON} and I_{OFF} values are obtained by changing the doping concentration in case of Si MOSFETs and by changing the nanotube diameter in case of SB CNFETs.

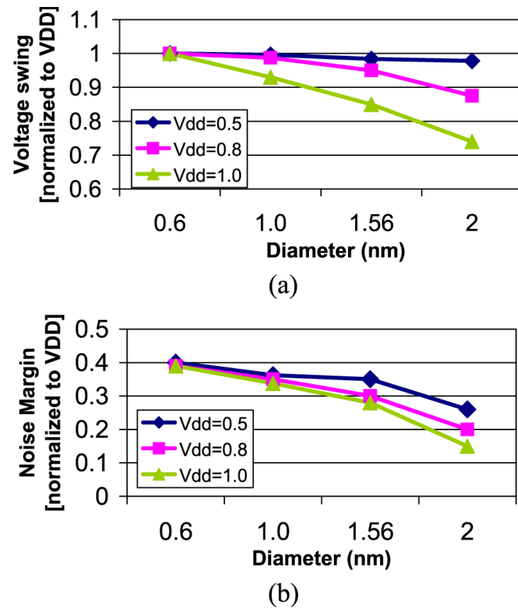


Fig. 8. Role of diameter and V_{DD} on normalized voltage swing and normalized noise margin of an SB CNFET-based inverter. Note how a larger diameter or a higher V_{DD} reduces both the voltage swing and the noise margin.

Finally, our data have narrowed down the choice of power-supply voltages and CNT diameters for circuit operation based on our dc analysis that will be summarized in the conclusion section.

V. Conclusion

In this paper, we have analyzed the promise that CNT-based electronics hold for digital circuit design. We investigated different CNFETs for an optimal switch. SB CNFETs, MOS CNFETs, and state-of-the-art Si MOSFETs were systematically compared from a circuit/system design perspective. Transistor I_{ON} versus I_{OFF} data show that SB CNFETs outperform Si MOSFETs at low supply voltages, while at higher supply voltages, the situation is reversed. A simulation environment incorporating an atomistic device description and a lookup-table-based circuit solver has been used. DC analysis determined how noise margin and voltage swing vary as a function of tube diameter and power-supply voltage. Our data suggest that we should operate at lower than 1-V supply voltages with tube diameter of around 1 nm. Our analysis of high-performing single-tube SB CNFET transistor structures revealed that 1 to 1.5 nm is the optimum CNT diameter for high-speed digital applications. Despite several serious technological barriers, CNTs with their high-current capability show a potential for performance improvement. However, further research is required on material quality of the CNTs, on improving the yield of semiconducting tubes, and on the growth of the nanotubes in a predetermined direction with good control of diameter thickness (for control of variation).

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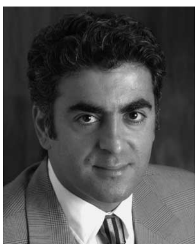

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