Advances in Computational Modeling of Electronic Devices Based on Graphene

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***Abstract*—Nowadays electronic devices such as $p-n$ diodes, field-effect transistors, logic gates, mixers, ring oscillators, and memories have been designed based on single, bi and/or multi-layer graphene. However, a lot of effort must be developed to integrate mathematical models into new simulators for electronic devices based on nanomaterials such as those based on carbon nanotubes, fullerenes, and graphene. Main contributions with respect to modeling and simulation of electronic devices based on graphene and developed in the ultimate years are analyzed here. In addition, future perspectives related with mathematical modeling of electronic devices based on graphene are discussed.**

***Index Terms*—Carbon nanotubes, field-effect transistors, graphene, logic gates, nanoelectronics, nanomaterials.**

I. Introduction

THE GRAPHENE can be considered as the most important material at the beginning of the 21st century, from that Novoselov and Geim announced the achievement of graphene sheets in 2004 [1]. It is 2-D crystalline allotrope of carbon which is strong, light, and nearly transparent, as well as an excellent thermal and electrical conductor. Its electrical properties are a combination of semiconducting behavior (zero density of states) and a metallic behavior (lack of bandgaps) [2]. In addition, its electronic flow is ordered and do not exists interaction among electrical carriers. These properties can be adjusted by means of electrical and magnetic fields, rise of layers, change of geometry, and chemical modification.

Graphene continues being subject of intense research and debate with respect to its electrical properties. Technical issues such as the interaction among electronic carriers and how it modifies its physical properties are still being exhaustively researched for numerous groups around the world. Therefore, the computational modeling represents an excellent tool to forecast electrical behavior of electronic devices based on graphene, where different phenomena found in them can be incorporated before of being physically implemented.

This paper has been divided as follows. In Section II basic concepts related with types and electrical properties of graphene are given. Next, the main contributions that have been developed for modeling electrical properties of electronic devices based on graphene are analyzed in Section III. In Section IV, future perspectives that must be developed with respect to simulation of electronic devices based on graphene, and which must be achieved in the next years are described. Finally, conclusions of this paper are given in Section V.

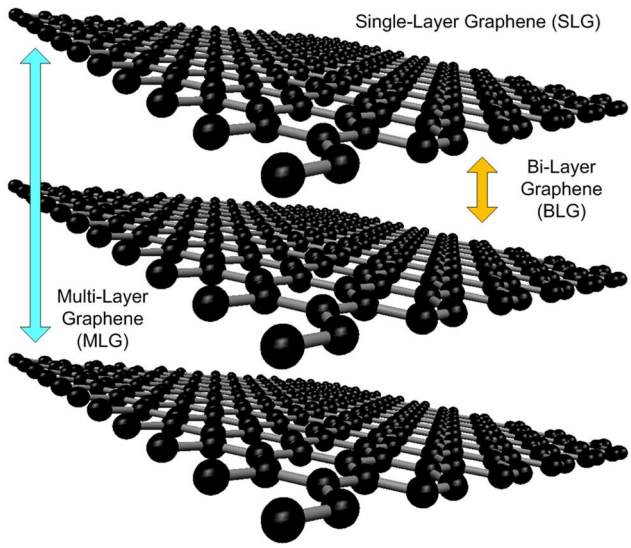

Fig. 1. Structure of the different types of graphene: SLG, BLG, and MLG.

II. Basic Concepts of Grapheme

There are several allotropes of carbon of which the most interesting in nowadays is called graphene, which is a 2-D, crystalline allotrope, where carbon atoms are densely packed in a sp^2-bonded atomic-scale hexagonal pattern. Graphene can be wrapped up into 0-D fullerenes, rolled into 1-D nanotubes or stacked into 3-D graphite [3]. In Section II-A types of graphene in accordance with their electrical properties are described. Main electrical phenomena found in graphene are described in Section II-B.

A. Types of Graphene

Graphene can be classified in accordance with the number of graphene sheets as: single-layer graphene (SLG) or mono-layer graphene, bi-layer graphene (BLG), and multi-layer graphene (MLG), as depicted in Fig. 1. Strips of graphene with ultra-thin width (< 50 nm) are known as graphene nanoribbons (GNRs).

Graphene sheet can be enrolled at specific and discrete chiral vectors named n and m, and thus, it can be called as armchair graphene if $n = m$, if $n \neq m$ is called chiral graphene, or

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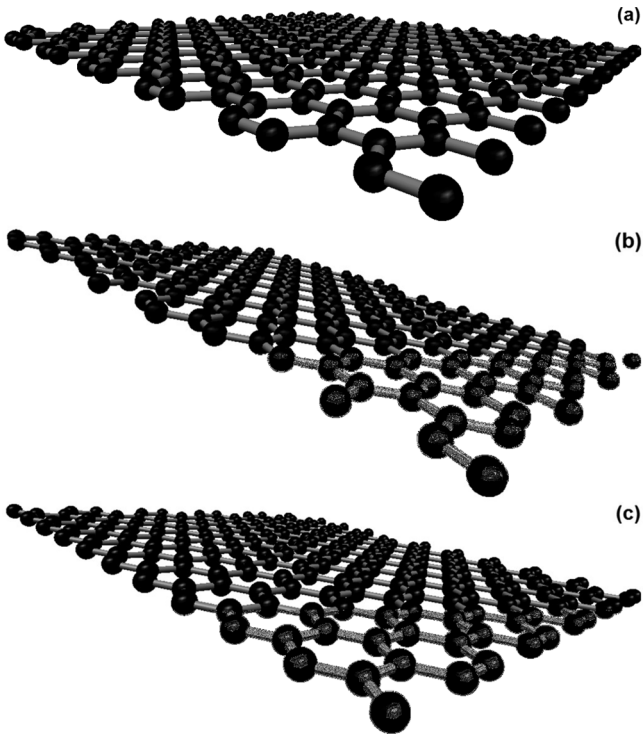

Fig. 2. Different types of SLG in accordance with their electrical properties: (a) intermediate bandgap semiconducting $(n, 0)$, (b) small bandgap semiconducting $(n - m = 3i)$, and (c) metallic (n, m).

zigzag graphene if $m = 0$ [4]. Moreover, it can be classified as intermediate bandgap semiconducting if $m > n$, small bandgap semiconducting if $n - m = 3i$ where i is an integer, and finally, metallic graphene if $n = m$, as shown in Fig. 2. Isolated or free-standing graphene is a single atomic plane of graphite suspended in an environment embedded in their extremes. Graphene can self-repair holes in its sheets by exposing to molecules containing carbon with the aim of obtaining a perfect aligning into hexagons, completely filling with carbon atoms all holes in its structure.

B. Electrical Properties of Graphene

Charge carriers in graphene can travel thousands of interatomic distances without scattering through its structure thanks to their carrier mobility whose values are as high as 10 000 $\mathrm{cm^2V^{-1}s^{-1}}$ at room temperature (10 times higher than in silicon, and it is improved with high quality GNRs), which are very common in this material [5], [6]. Electronic properties of 2-D graphene come from its gapless, massless, chiral Dirac spectrum derived on density and temperature-dependent carrier transport in doped or gated graphene and observed through fractional quantum Hall effect [7]–[9] and Klein tunneling [10]–[12]. Due to massless chiral Dirac spectrum, there is a quantized Landau level which is shared by electrons and holes. Since, it do not exists bandgap in graphene, carrier dispersion is presented, which generates a direct transition between electron-like transport to hole-like transport, when an adequate gate voltage is applied between the charge neutral Dirac point and the point where gate is localized [13]. Graphene has an insulating behavior at low enough carrier densities. In particular,

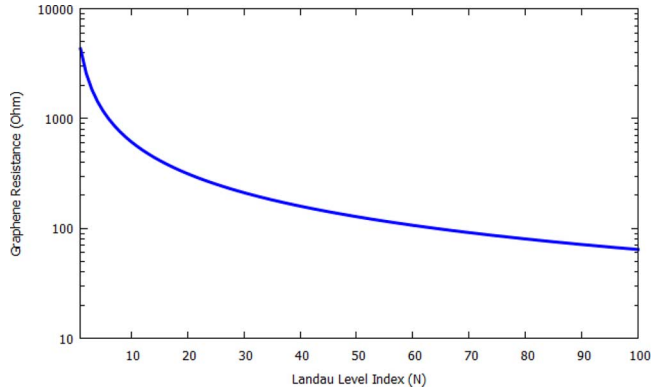

Fig. 3. Graphene resistance versus Landau level index.

BLG and MLG structures present a transport bandgap derived of intrinsic spectral bandgap generated by the confinement of carriers and the biased electrical field, due to their own weak antilocalization behavior. Electron-electron interactions in strong magnetic fields can be presented in two ways: 1) weak coupling limit, in which electron-hole excitations involve collective modes such as linear magnetoplasmons, linear dispersion and vanishing band mass, and 2) strong coupling limit, where partially filled relativistic Landau levels are presented due to exciting resonance phenomena [14]. The two-terminal device resistance based on graphene (R_G) between the Landau levels is given by [15]

$$R_G = \frac{h}{4(N + \frac{1}{2})e^2} \tag{1}$$

where N is an integer corresponding to the Landau level index, h is Planck's constant, and e is the electron charge. The behavior of graphene resistance versus Landau limit index is sketched in Fig. 3, i.e., its conductance is quantized [11].

III. Modeling of Electronic Devices

The modeling of electronic devices consists in a computer simulation of a real system using mathematical concepts, which are run on a single computer or in computer networks. The modeling allows to the designer predict the electrical behavior with the aim of optimizing the desired performance before fabricating electronic devices. In Section III-A, negative differential resistance is studied as a phenomenon involved in high frequency electronic devices. The effect of the effective screening length on performance of transistors is analyzed in Section III-B. The role of the tunable bandgap presented by bilayer graphene on electronic devices is discussed in Section III-C. In Section III-D, the behavior of the drain voltage and static power in logic gates is evaluated. The frequency's behavior of the transistors based on graphene is studied by means of the maximum frequency, and cutoff frequency, which are detailed in Section III-E. In Section III-F, small-signal models for transistors based on graphene are presented. Finally, intrinsic delay time is estimated in Section III-G.

A. Negative Differential Resistance (NDR)

A schematic of a three-terminal top-gated graphene field-effect transistor (GFET or GNRFET) is illustrated in Fig. 4,

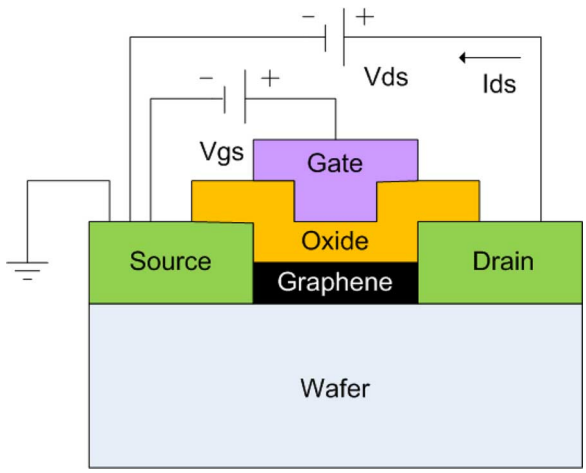

Fig. 4. Three-terminal graphene field-effect transistor.

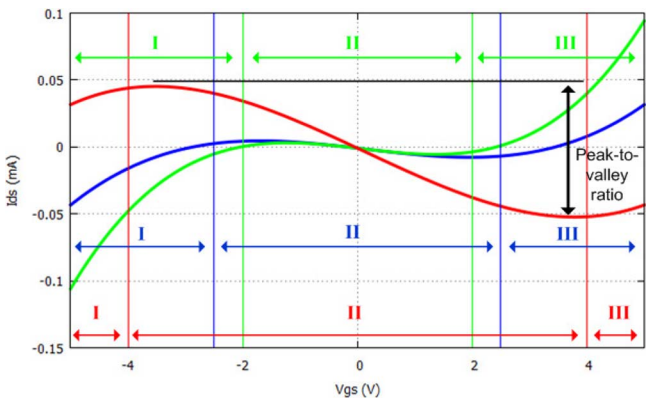

Fig. 5. Negative differential resistance (NRD) effect presented in GFET.

[16]. Electronic devices such as frequency multipliers, memories, fast switches, and high-frequency oscillators up to the THz range, present a negative differential resistance (NDR) behavior, where non-ohmic current-voltage characteristics as sketched in Fig. 5, are obtained by realizing changes in coefficients of polynomial expression relating drain-source current and gate-source voltage. Region I represents the tunneling current, Region II is associated with the negative differential resistance, and finally, Region III corresponds to the conventional forward-bias current.

The peak-to-valley ratios can be controlled with the changes in third-order and first-order terms of the expression between I_{ds} and V_{gs} of the FET transistor, which can be generically expressed by the mathematical relationship

$$I_{ds} = aV_{gs}^3 + bV_{gs}^2 + cV_{gs} + d \tag{2}$$

where a, b, c, and d are constants related with the fabrication parameters of the device. The constant a, modifies the amplitude of the I_{ds}, and constant c changes the magnitude of the interval of values of V_{gs} where negative differential resistance is presented. Moreover, constants b and d modify waveform of the curve I_{ds} versus V_{gs}.

In practice, NDR requires small contact resistances, very good electrostatic control over all length of the channel, and low scattering of the electrical carriers by the electrical field applied among terminals of the transistor.

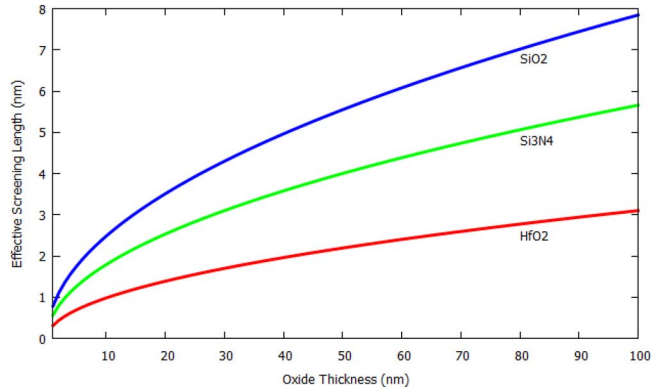

Fig. 6. Effective screening length versus oxide thickness used in gate for field effect transistors based on BLG.

B. Effective Screening Length

In particular, 2D-materials can achieve the ideal effective screening length (ESL), λ, and they can be exploited beyond the quantum capacitance limit (QCL) with the aim of reducing the channel length in transistors [17]. In the case of devices where an electrical channel is based on single and double layer graphene, λ can be determined by the expression

$$\lambda = \sqrt{\frac{\varepsilon_G d_G d_{OX}}{\varepsilon_{OX}}} \tag{3}$$

where ε_G and d_G are the dielectric constant and thickness of the graphene, and ε_{OX} and d_{OX} are the respective quantities for the oxide used in the gate. Here, λ was evaluated for different values of oxide thickness and different types of oxides used in integrated circuits (see Fig. 6).

The reduction of ESL increases the quantity of drain-source current of the transistor, and therefore, the intrinsic gate delay and dynamic power are reduced, which increases the performance of digital circuits based on graphene transistors. Thus, the use of dielectrics with very high dielectric constants is the best option to reduce ESL.

Boron nitride can be used as a dielectric oxide in the gate to place graphene in an electronic device due to similarity of the honeycomb lattice structure and comparable lattice spacing [10], [18]–[20]. When bilayer graphene is used, their atoms experience different onsite energies, and therefore, until four electronic bandgaps are available for electrical conduction, as shown in Fig. 7. These bandgaps are due to the presence of two nearly parallel conduction bands above two nearly parallel valence bands within electronic structure near the Fermi level of a graphene bilayer [21].

C. Tunable Bandgap of the Bilayer Graphene

Materials such as graphene present an electronic bandgap that can be tuned by applying a variable external electrical field, and it determines their electrical transport properties used in the design and optimization of electronic devices [21]. The use of top and bottom gates in GFETs allows controlling independently the electronic bandgap and carrier doping concentration [22]. In

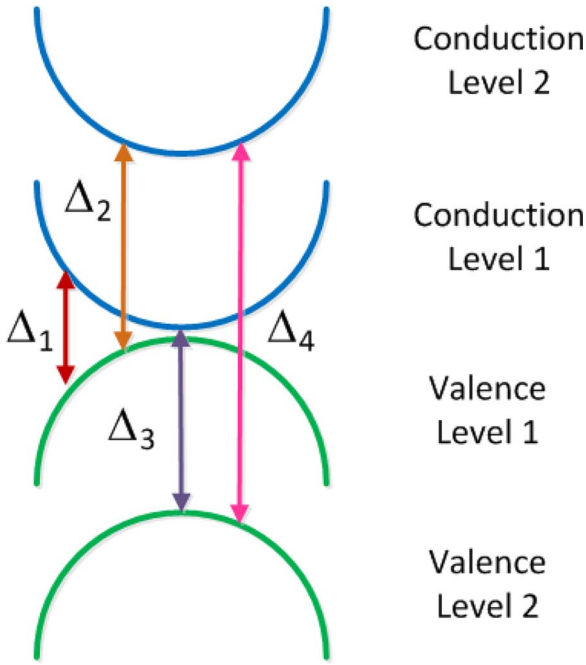

Fig. 7. Different bandgaps presented by bilayer graphene.

[21], was reported that with a gate-tunable bandgap up of 250 meV with an order of magnitude higher than the room-temperature thermal energy (25 meV), it is possible to achieve the intrinsic potential of bilayer graphene for nanoelectronic applications. In addition, tunability of the threshold voltage to achieve high on/off ratio bilayer graphene devices will allow the development of functional devices such as complementary inverters by means of dual gated p- and n-type bilayer graphene FETs [22].

D. Drain Voltage Versus Drain Resistance and Static Power Versus Drain Resistance

A logic gate with two inputs based on a GFET is shown in Fig. 8. Different logic gates can be obtained thanks to transference curve R versus V_{gs} of the monolayer graphene, as was presented in [23].

The output of two-input logic gates based on a single graphene transistor or GNRFET depends on the drain resistance (R_D), channel-resistance based on graphene (R), and bias voltage (V_{DD}), in accordance with the (4) [23]

$$V_D = \frac{R_D}{R + R_D} V_{DD} \tag{4}$$

and, the static power dissipated by transistor is given by

$$SP = \frac{V_{DD}^2}{R + R_D}. \tag{5}$$

The behavior of the drain voltage and static power versus drain resistance for logic gate of Fig. 8, it is shown in Fig. 9. The GNRFET static power can be reduced only if a higher channel resistance R is used, thus, strategies to increase electrical resistance of the graphene must be developed. In addition, it is necessary to point that high threshold voltage (V_H) and low threshold voltage (V_L) of the logic levels are restricted by bias voltage.

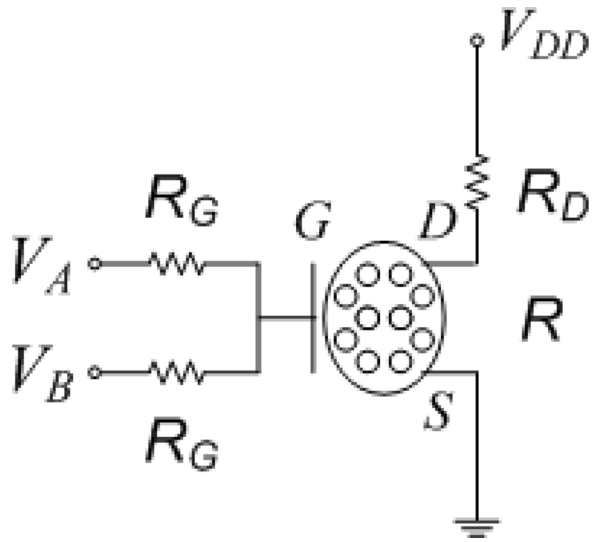

Fig. 8. Two-input logic gate based in a single transistor based on graphene.

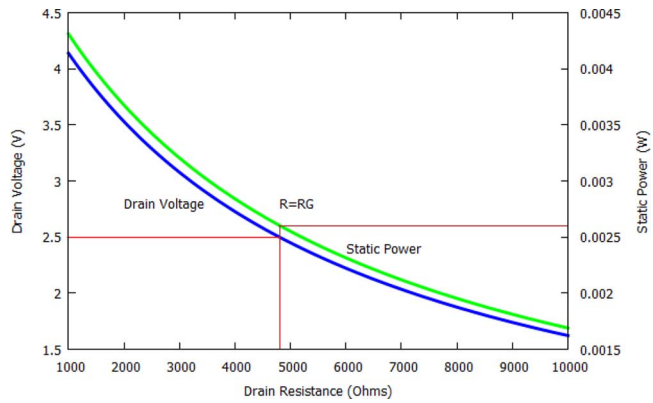

Fig. 9. Drain voltage versus drain resistance (blue line) and static power versus drain resistance (green line) for logic gates (illustrated in Fig. 8) based on GFETs.

E. Maximum Frequency and Cutoff Frequency

Some important parameters of performance of GFETs for very high frequencies are their cutoff frequency and maximum frequency. Both parameters determine the boundary in the frequency response of field-effect transistors. Cutoff frequency represents frequency which gain of the transistor begins to be reduced rather than passing through. The cutoff frequency of the single graphene transistor or GNRFET illustrated in Fig. 10, it is given by (6) [24], [25]

$$f_T = \frac{g_m}{2\pi C_{gs}} \tag{6}$$

where C_{gs} is the gate-to-source capacitance, and g_m is the transconductance of the transistor. In radio-frequency (RF), maximum frequency is the highest radio frequency that can be used for transmission between two points. The maximum frequency of the GFETs can be obtained by means of mathematical expression

$$f_{\max} = \frac{g_m}{4\pi C_{gs}\sqrt{g_d(R_s + R_G)}} \tag{7}$$

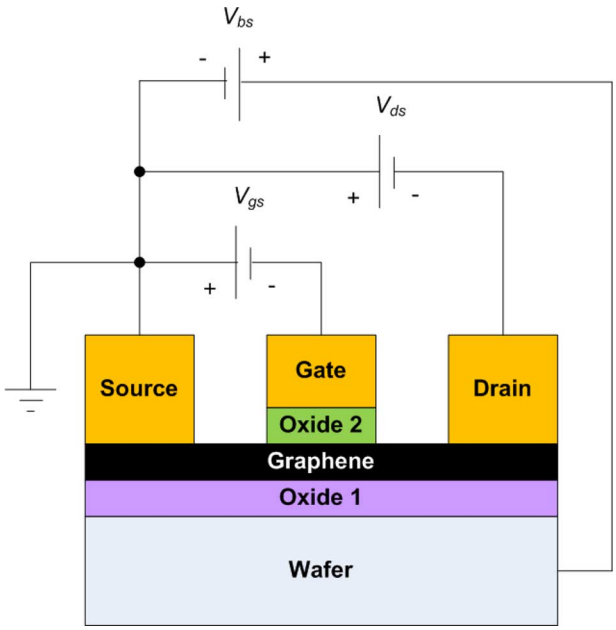

Fig. 10. Dual-gate graphene transistor controlled by field-effect.

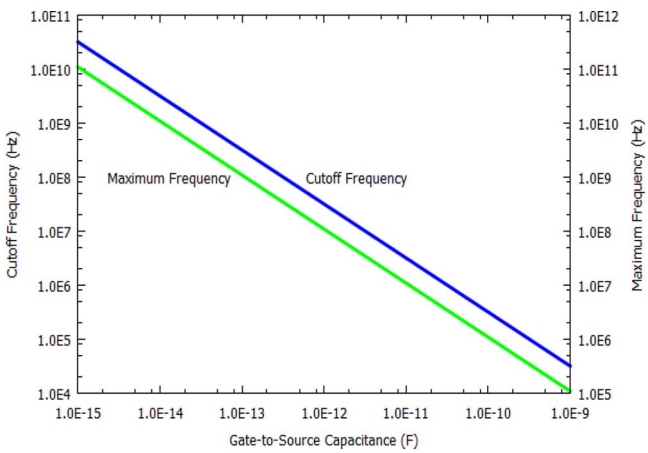

Fig. 11. Cutoff frequency (blue line) and maximum frequency (green line) versus gate-to-source capacitance of a GFET [(6) and (7)].

where g_d is drain conductance, R_S is source resistance, and R_G is gate resistance.

The behavior of the cutoff frequency and maximum frequency with respect to C_{gs} of the GFET (Fig. 10) is depicted in Fig. 11. Blue line represents maximum frequency that GFET can achieve during its operation in accordance with the value of the gate-to-source capacitance. A very high frequency can be obtained when a very small capacitance is presented between gate and source. A similar behavior is obtained for maximum capacitance under identical conditions. In addition, cutoff frequency is large with respect maximum frequency by a factor of five times for any value of gate-to-source capacitance of the GFET.

An alternative mathematical relationship for determining maximum frequency was developed in [25], [26]

$$f_{\max} = \frac{f_T}{2\sqrt{g_{DS}(R_G + R_i + R_s) + 2\pi f_T C_{GD} R_G}} \tag{8}$$

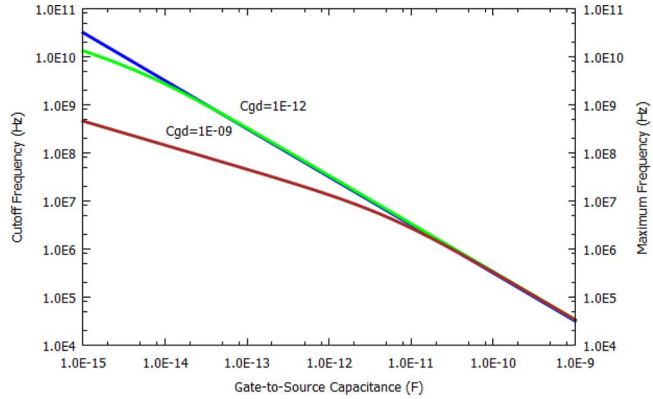

Fig. 12. Cutoff frequency (blue line) and maximum frequency (green line and brown line) versus gate-to-source capacitance of a GFET [(6) and (8)].

where R_i is the channel-sided charging resistance of the gate/source capacitance, R_G is the gate resistance, C_{GD} is the gate-to-drain capacitance, g_{DS} is the differential source/drain conductance, and f_T is the cutoff frequency. The behavior of maximum frequency with respect to C_{GS} and compared with f_T is sketched in Fig. 11. It can be visualized that the value of C_{GD} modifies the behavior of the curve for high frequencies.

Two curves were obtained with the aim of studying the effect of C_{GD} on maximum frequency (see Fig. 12). It can be observed that C_{GD} must be very small with the aim of achieving a similar value of maximum frequency and cutoff frequency for all values of gate-to-source capacitance.

Other mathematical relationships to determine cutoff frequency and maximum frequency were proposed in [27]–[29], include GFET's transconductance within the model. The mathematical relationships for cutoff frequency and maximum frequency for the extrinsic frequencies of the GFET are the following:

$$fr = \frac{gm}{2\pi(C_{GS} + C_{GD})\left[1 + g_{DS}(R_D + R_S) + \frac{C_{GD} g_m (R_D + R_S)}{C_{GD} + C_{GS}}\right]} \tag{9}$$

and

$$f_{\max} = \frac{gm}{4\pi C_{GS}\sqrt{g_{DS}(R_G + R_i + R_S) + g_m R_G \frac{C_{GD}}{C_{GS}}}} \tag{10}$$

where g_m is the GFET's transconductance. Both expressions imply that to achieve high f_T and $f_{\max}$, the transistors's transconductance should be high and all other elements of the equivalente circuit should be as small as possible [27]. In addition, the elements of the intrinsic transistor and the gains directly implied in the values of f_T and $f_{\max}$ are sensitive to the dc bias conditions as was described in [27], therefore, new techniques to cancel such dependence must be developed.

Both f_T and $f_{\max}$ reflect important figures of merit of transistor performance with respect to the frequency of the electrical input signal [30]. f_T represents the intrinsic behavior of the transistor channel, whereas $f_{\max}$ depends on fabrication process.

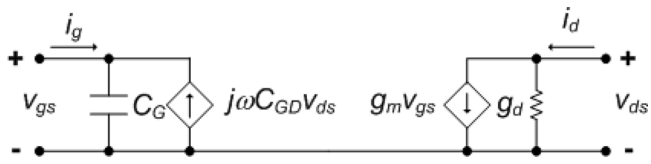

Fig. 13. Small-signal intrinsic model of a GFET.

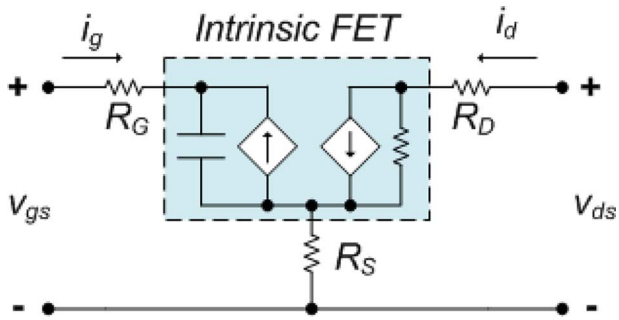

Fig. 14. Small-signal extrinsic model of a GFET.

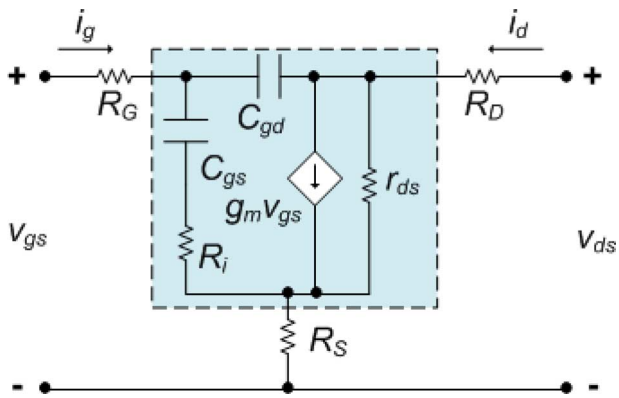

Fig. 15. Small-signal model for GFETs used in analog/RF circuits.

F. Small-Signal Model

In [31], it was proposed a small-signal intrinsic model for a transistor based on graphene, as shown in Fig. 13. This model contains classical circuit elements such as capacitors, resistors, and voltage-controlled current sources interconnected in a two-port network, which is based on admittance parameters used in electronics to replace FETs in circuit analysis.

A small-signal extrinsic model of a GFET is shown in Fig. 14. The model is based on the intrinsic device of Fig. 13, and includes three resistors which represent gate (R_G), drain (R_D), and source (R_S) resistance in series, that are connected to inputs of the intrinsic device terminals.

An equivalent circuit of GFETs that can be used for modeling analog/RF circuits is depicted in Fig. 15 [31]. The shaded rectangle represents those elements of the intrinsic transistor which represent gate-source capacitance C_{gs}, gate-drain capacitance C_{gd}, the transconductance g_m, the differential drain resistance g_{ds}, and R_i channel-sided charging resistance. Elements externally illustrated are the gate resistance R_G and the source/drain series resistances R_S and R_D, respectively.

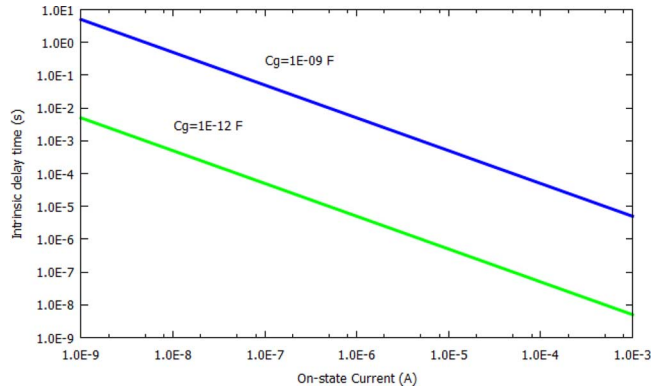

Fig. 16. Intrinsic time delay versus on-state drain current.

Each model can be used under different approaches in accordance with the electrical parameters that designer desires to estimate and emphasize.

G. Intrinsic Delay Time

An important performance parameter that allows knowing the switching-speed in ac operation of a transistor is called intrinsic delay time τ_S, which is given by [32]

$$\tau_S = \frac{C_G V_{DD}}{I_{on}} \tag{11}$$

where I_{on} is the on-state drain current, V_{DD} is the bias current, and C_G is the gate capacitance. The behavior of the intrinsic delay time versus on-state drain current is shown in Fig. 16. High-drain currents reduce intrinsic delay time involved in GFET switching-speed. It is expected that extremely-fast electron transit-time can be achieved, that is, short periods of few femtoseconds are involved. GFETs must be faster than that submicrometer planar FETs [33].

IV. Current Advances and Future Perspectives

Graphene devices have a short history, which has impressed to all by their future expectations. A lot of problems must be solved before they are used completely at industrial level around of the world. Some current advances and future perspectives are discussed in the next subsections.

A. Current Advances

The main trends are focused in applying graphene in the design of RF amplifiers, and CMOS-like digital logic [30]. Technical issues such as gate resistance, source-to-drain tunneling current flow, variability by dimensions and process, parasitic resistance and capacitances, and high power consumption, continue being the main problem to solve in the use of transistors based on graphene. For example, the effect of parasitic elements increases the overall delay time during operation of these devices. Thus, new transistor designs must be developed to reduce or even avoid parasitic elements, since change of channel material is not sufficient. Some researchers do not expect that graphene can be used in commercial circuits in a near- and medium-term future [30]. However, new mechanisms of electrical conduction must be discovered, visualized, studied, simulated, and used, since traditional concepts are now obsolete.

Quantum mechanics must be more exhaustively exploited to develop devices using unique properties of graphene, where flexible substrates and printed electronics can be one reality in electronic industry. However, technical performance variables such as high current saturation, high intrinsic gain, large on-off ratios, excellent electrostatic, and better immunity against short-channel effects, are the most promising parameters of the use of graphene in electronic devices.

Vargas-Bernal in [4] proposed that four types of GFETs could be built: 1) back-gated GFETs [34], 2) top-gated GFETs [35], [36], 3) wrap-around gate GFETs, and 4) suspended GFETs. The last two topologies are not available now, but these can be fabricated in this decade. Back-gated GFETs have large parasitic capacitances and poor gate control, but when smooth edges of the GNR are achieved, on/off ratios as high as 10^6 can be achieved, which can be very attractive to digital integrated circuits. As was shown previously, top-gated GFETs are the preferred option for analog integrated circuits due to the reduction of parasitic capacitances and an excellent gate control. It is necessary pointing that entire rectangle of GNRs will be gated with the aim of completely exploiting graphene in wrap-around gate GFETs. Gating is directly associated with the distance from the gate terminal to the graphene layer or layers, and with the dielectric breakdown of the oxide used as spacer who separates both materials [10].

In accordance with Novoselov [37], graphene will used after 2021, until compound semiconductors (*III-V* materials) fail to satisfy high-frequency device requirements. A broadband RF mixer working at frequencies up to 10 GHz, it was implemented using graphene field-effect transistor (GFET) in [38]. It achieved a 27-dB conversion loss at 4 GHz, which was higher with respect to another mixers previously published, therefore, it is even feasible implement amplifiers and oscillators for wireless communication systems.

Recently, a three-terminal active device based on graphene, and called barrister was introduced, which adjusts its gate voltage to control a Schottky barrier formed by graphene and silicon [39]. They demonstrated its use by means of logic circuits, where the possibility of incorporating n-type and p-type allows to the designer achieving on/off ratios, and current densities attractive to high-speed logic circuits.

B. Trends in Electrical Modeling of Graphene Devices

Since different applications require different qualities and fabrication methods, in the next years will be essential to obtain different mathematical models for predicting the electrical behavior of the graphene, in electronic devices used for integrated circuits. Graphene will be established as benchmark material when electronic device prototypes can be sufficiently competitive, through precise control of electronic properties with the aim of being led to industrial processes. Thus, electronic devices based on graphene will continue being the center of worldwide research efforts.

A lot of effort must be developed to understand and model the correlation between geometric or electronic defects on electrical transport of the graphene. Different methods to gating graphene nanoribbons in electronic devices must be achieved, and new models for electrical performance of the electronic devices based in them, must be proposed. This gating can be attained through of the use of bi-layer or multi-layer graphene. The gate resistance value depends on the gate voltages applied. Thus, novel mathematical models capable of predicting electrical parameters will be developed in a near future. There is a promising perspective on the use of graphene-based tunable templates to modify and control electrical properties. These templates require post-treatment of the graphene, which increases the number of technological steps in device fabrication, such as exfoliation. This process must be mathematically modeled to determine electrical behavior, before electronic device is physically fabricated.

Mathematical models for determining intrinsic gate delay time, maximum frequency, and cutoff frequency for all types GFETs, must be developed for knowing the fundamental limit of such devices. Strong oscillations of the graphene electronic conductance, and the presence of Coulomb blockade peaks, must be incorporated into mathematical models of the electrical properties.

Substrate imperfections and the 1-D defects in graphene must be incorporated in the models used, to determine their effects on electrical performance of the electronic devices, these until now only have been indirectly measured. It is essential to develop a systematic modeling of the electrical effect of effective length of the channel, under various fabrication process conditions, and device geometries.

Finally, the mathematical modeling of hybrid structures, that is, graphene combined with other materials, must be developed to predict electrical properties of the new devices that are being developed. A new generation of electronic devices [40]–[44] will be consolidated in this decade through of the use of heterostructures, where 3-D semiconductors will be developed to fulfill the requirements of the electronic industry. Thus, graphene must be used in nanocomposites or hybrid materials as carbon nanotubes to be completely exploited.

V. Conclusion

Graphene is an emerging material with potential applications in electronic devices due to its high carrier mobility, high saturation velocity, high current densities, and ultra-thin thickness to fabricate ultra-high speed transistors with cutoff frequency exceeding 1 THz. Until now a broad theoretical understanding of the electrical transport in SLG has been achieved, however, a lot of work must be done to determine electrical properties of BLG and MLG systems. The application of graphene in electronic devices is at its infancy due to that many device ideas are at proposal stages, however, the mathematical modeling is an excellent tool to forecast electrical properties of devices fabricated with graphene. To achieve this objective, it is necessary to develop new simulators for predicting the electronic behavior of the devices based on graphene with a special emphasis to very high frequencies both in analog and digital integrated circuits.

Nowadays, mathematical expressions of the electrical parameters of devices based on graphene are evaluated individually or are indirectly measured, and these must be combined in a unique simulation tool. The use of these devices in RF will be strategic to develop the new generation of devices capable of exceeding to RF-MEMS, and other current technologies. Mathematical

simulations show as the use of high-k dielectrics, small dielectric thickness, small contact-resistances, very good electrostatic control over all length of the channel, and low scattering of the electrical carriers by electrical field applied between terminals of the transistor, can increase the viability of devices based on graphene for digital and analog integrated circuits.

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