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A novel graphene nanoribbon field effect transistor with two different gate insulators

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HIGHLIGHTS

- A novel structure with two different gate insulators for GNRFET (TDI-GNRFET) is proposed.
- Mode-space Non-Equilibrium Green's Function (NEGF) formalism in the ballistic regime is used.
- TDI-GNRFET has lower leakage current and higher I_{on}/I_{off} ratio in comparison with low-K GNRFET.
- TDI-GNRFET has smaller capacitances and lower intrinsic delay in comparison with high-K GNRFET.
- The proposed TDI-GNRFET has good Drain Induced Barrier Lowering (DIBL) and subthershold swing.

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ABSTRACT

In this paper, a novel structure for a dual-gated graphene nanoribbon field-effect transistor (GNRFET) is offered, which combines the advantages of high and low dielectric constants. In the proposed Two Different Insulators GNRFET (TDI-GNRFET), the gate dielectric at the drain side is a material with low dielectric constant to form smaller capacitances, while in the source side, there is a material with high dielectric constant to improve On-current and reduce the leakage current. Simulations are performed based on self-consistent solutions of the Poisson equation coupled with Non-Equilibrium Green's Function (NEGF) formalism in the ballistic regime. We assume a tight-binding Hamiltonian in the mode space representation. The results demonstrate that TDI-GNRFET has lower Off-current, higher On-current and higher transconductance in comparison with conventional low-K GNRFET. Furthermore, using a top-of-the-barrier two-dimensional circuit model, some important circuit parameters are studied. It is found that TDI-GNRFET has smaller capacitances, lower intrinsic delay time and shorter power delay product (PDP) in comparison with high-K GNRFET. Moreover, mobile charge and average velocity are improved in comparison with low dielectric constant GNRFET. The results show that the TDI-GNRFET can provide Drain Induced Barrier Lowering (DIBL) and Subthreshold Swing near their theoretical limits.

1. Introduction

Conventional Si-CMOS devices have been utilized in the semiconductor industry for decades. Nowadays, it is really difficult to keep up with Moore's Law because of several challenges and limitations [1].

Graphene is a honeycomb two dimensional carbon material. It has absorbed most interest in theoretical and experimental scopes due to its novel electronic characteristics, such as high mobility and good compatibility with common planar semiconductor technology. Graphene is a zero gap material; nevertheless, when patterned into nanoscale ribbons, a bandgap opens due to the lateral quantum confinement. The narrow stripes of graphene with width less than 100 nm, known as graphene nanoribbons (GNRs), are quasi-one-dimensional materials exhibiting finite energy gaps [2,3]. GNRs can be either metallic or semiconductor depending on the crystallographic direction of the ribbon axis. The oscillatory behavior of band gap is predicted for semiconducting narrow armchair ribbons as a function of their width [4].

Graphene can be an evolutionary replacement to conventional CMOS where it replaces Si as the channel material. Therefore, Graphene nanoribbons are being as a promising candidate for the next generation of transistors, specifically as the channel for transistors, because of their excellent transport properties [5,6]. Transistors made of GNRs are called Graphene-Nano-Ribbon Field

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Effect Transistors (GNRFETs), which have been explored in recent studies as potential alternatives to CMOS devices [1].

The gate-leakage current is an important device parameter that takes a major hit due to continued scaling. Device scaling requires gate oxide thickness (t_{ox}) to be scaled for maintaining high On-current (I_{on}) and reducing short channel effects. The gate dielectric leakage current increases with reducing the oxide thickness and becomes the most important contributors of the Off-current (I_{off}). This leakage current over many millions of transistors on a chip results in a large power dissipation which can burn out the chip [7,8].

In order to reduce transistor leakage current, researchers have looked for years at the alternative gate dielectric materials. They found that the gate dielectric material with high dielectric constant will increase gate capacitance without the existence of leakage current. While using a material with a lower dielectric constant as gate dielectric material will reduce parasitic capacitances [9,10].

In this paper, a new GNRFET design based on two different dielectric materials is offered. In the proposed device that is called Two Different Insulators GNRFET (TDI-GNRFET), the gate insulator is made of both high and low dielectric constant materials. In order to simulate the device characteristics; we solve the Schrödinger equation coupled with the Poisson equation in the ballistic regime, using the NEGF in a mode space representation. We employ the tight-binding method in our study [6]. The results are investigated and compared with the conventional structures of GNRFET. Furthermore, we have used a two-dimensional circuit model for analyzing the GNRFETs. It is an endeavor to extract important characteristics of the GNRFETs such as gate, source, drain and quantum capacitances, intrinsic delay time, power-delay product, mobile charge, average velocity, DIBL and subthreshold swing.

This paper is organized as follows: Section 2 presents device geometry which contains conventional GNRFET and the proposed TDI-GNRFET structure. Section 3 represents the calculation method for simulation of the aforementioned GNRFETs. A two-dimensional modeling method is introduced in detail in Section 4, and the modeling results are shown in this part as well. Finally, Section 5 concludes this paper.

2. Device geometry

Fig. 1 shows a schematic representation of the dual-gated GNRFET in conventional structure. The channel material is assumed to be a single-layer armchair graphene nanoribbon (A-GNR) with an index of $n=12$, sandwiched between two layers of gate oxides. The index n, denotes the number of dimmer carbon atom lines transverse to transport direction. The width and length of this GNR channel are assumed to be $W=1.35$ nm and $L=10$ nm, respectively. The thickness of each insulating layer is chosen to be $t_{ox}=1.5$ nm. The channel is taken to be intrinsic; the source and drain regions are assumed to be heavily doped GNR with doping concentration value of 5×10^{-3} dopants per carbon atom.

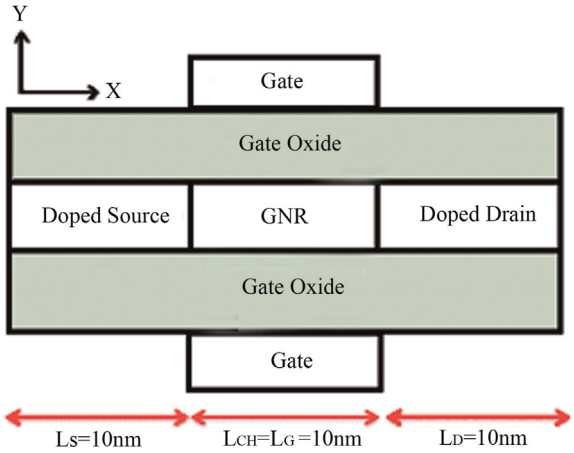

Fig. 1. Schematic of a dual gated GNRFET with a conventional structure.

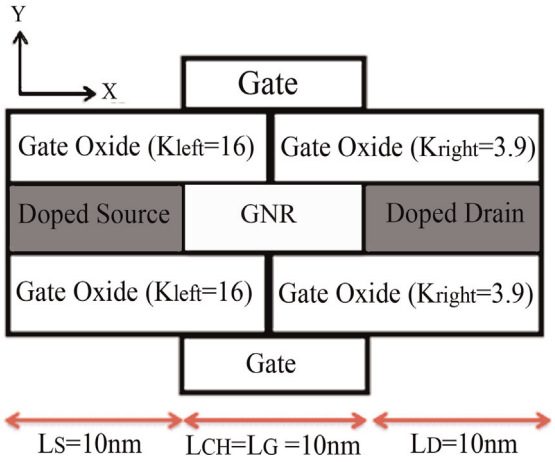

Fig. 2. The proposed structure for TDI-GNRFET.

As earlier mentioned, we present a new structure of dual-gated GNRFET with two different gate insulators. Fig. 2 shows the schematic of the TDI-GNRFET. Our proposed structure has two different gate insulators. It benefits the advantages of materials with high and low dielectric constants. Keeping this in mind, the gate length of the transistor shown in Fig. 1 is divided into two equal sections, which can be seen in Fig. 2. In order to decrease the capacitances, the gate dielectric at the drain side (right side) is selected as a material with low dielectric constant ($K_{right}=3.9$). Contrarily, the gate dielectric at the source side (left side) is chosen as a material with high dielectric constant ($K_{left}=16$) to improve On-current and reduce leakage current.

3. Implementation method

The Non-Equilibrium Green's Function (NEGF) formalism is used to solve the Schrödinger equation in the ballistic regime, together with the self-consistent solution of the two-dimensional Poisson equation. Device Hamiltonian for the GNR is determined by the tight-binding method. To decrease the computational cost of the simulations, the mode space approach is used. This method enables us to decouple the two-dimensional problem into one-dimensional decoupled lattices, which reduce the size of the problem in comparison with the real-space mode [6,11].

Description of the NEGF method has been explained in Refs. [12,13]. The basis of this method was on obtaining the retarded Green's function of the device as computed by the following equation:

$$G(E)=\left[(E+i0^{+})I-H-U-\sum_{S}-\sum_{D}\right]^{-1} \quad (1)$$

where $\sum_S$, $\sum_D$, H, E and I are self-energy of the source contact, self-energy of the drain contact, Hamiltonian matrix of the device, energy value and identity matrix, respectively. U is the self-consistent potential matrix that is determined by the solution of a two dimensional (2-D) Poisson equation. The local density of states

(LDOS) due to the source and drain can be written as

$$D_{S(D)} = G\Gamma_{S(D)}G^{+} \tag{2}$$

where $\Gamma_{S(D)}$ is the energy level broadening due to the source (drain) contact:

$$\Gamma_{S(D)} = i\left(\sum_{S(D)} - \sum_{S(D)}^{+}\right) \tag{3}$$

Consequently, the transmission coefficient versus the energy can be calculated as

$$T(E) = trace\left(\Gamma_S G \Gamma_D G^{+}\right) \tag{4}$$

Now, the current–voltage characteristic is obtained using $T(E)$ and the Landauer–Buttiker formula as follows [14]:

$$I = \frac{2q}{h}\int_{-\infty}^{+\infty} dE T(E)\left\{f\left(E, \mu_S\right) - f(E, \mu_D)\right\} \tag{5}$$

With $f(E, \mu_{S(D)})$ being the Fermi–Dirac distribution of electrons in the contact at chemical potential $\mu_{S(D)}$. In order to calculate the electrostatic potential, the Poisson equation is solved in a two-dimensional grid system within the structure of:

$$\nabla^2 U(x, z) = -\frac{\rho}{\varepsilon} \tag{6}$$

where ε and ρ are dielectric constant and charge density, respectively. The continuous form of the Poisson equation is discretized by applying the second-order finite difference scheme. The charge density is given by [14]

$$\rho = \frac{1}{2\pi}\int_{-\infty}^{+\infty} dE\{f(E, \mu_S)G\Gamma_S G^{+} + f(E, \mu_D)G\Gamma_D G^{+}\} \tag{7}$$

Fig. 3 shows the potential profile for TDI and conventional GNRFETs. We observe that the energy band diagram for a TDI-GNRFET has a barrier in the middle of the channel due to different dielectric constants at the drain and source sides of gate oxides.

The simulated I_{DS}–V_{GS} characteristics of the proposed and conventional GNRFETs are illustrated in Fig. 4. As shown, TDI-GNRFET has a lower Off-current compared to conventional GNRFET with low dielectric constant. This is due to more thermal emission current stemming from superior control of the gate potential on the channel near to source. This effect helps reducing Off-current and increasing On-current.

Fig. 5 depicts the I_{on}/I_{off} ratio for TDI and conventional GNRFETs. As it shows, the TDI-GNRFET has higher I_{on}/I_{off} ratio than conventional GNRFET with low dielectric constant.

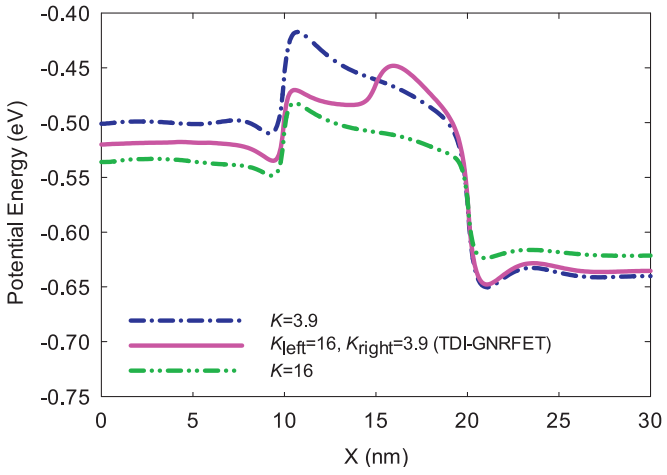

Fig. 3. Potential energy across the device for TDI-GNRFET and conventional GNRFETs with $K=3.9$ and 16.

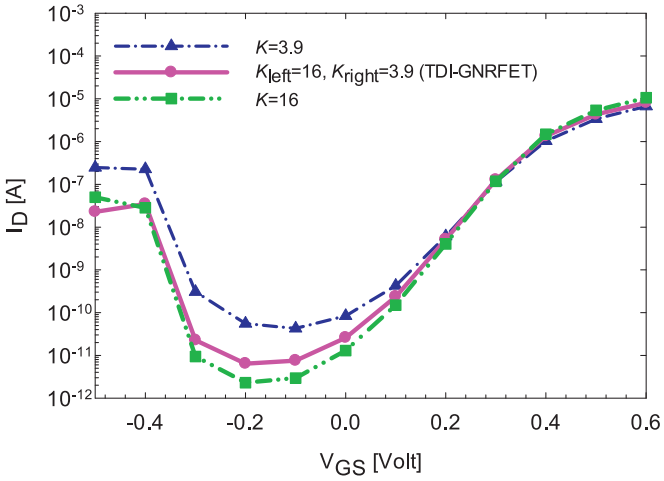

Fig. 4. The I_D–V_{GS} characteristic for TDI-GNRFET and conventional GNRFETs with $K=3.9$ and 16 at $V_{DS}=0.6$ V.

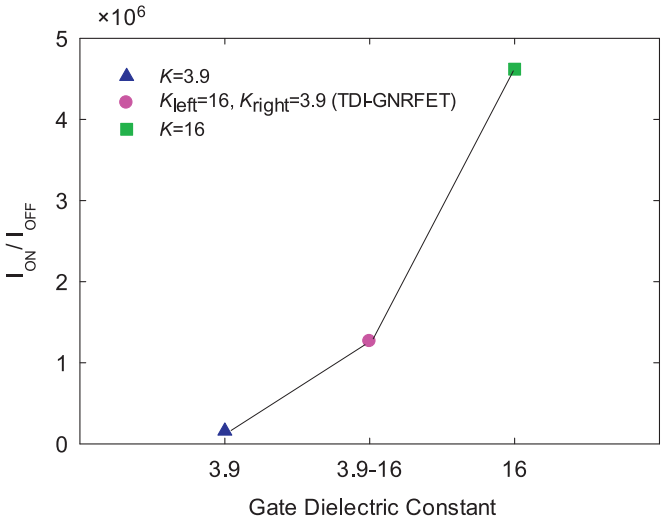

Fig. 5. I_{on}/I_{off} ratio for a TDI-GNRFET and conventional GNRFETs with $K=3.9$ and 16.

The calculated I_{DS}–V_{DS} characteristics of TDI and conventional GNRFETs are plotted in Fig. 6. As can be seen, the TDI-GNRFET has the higher delivering capability due to increase of thermal

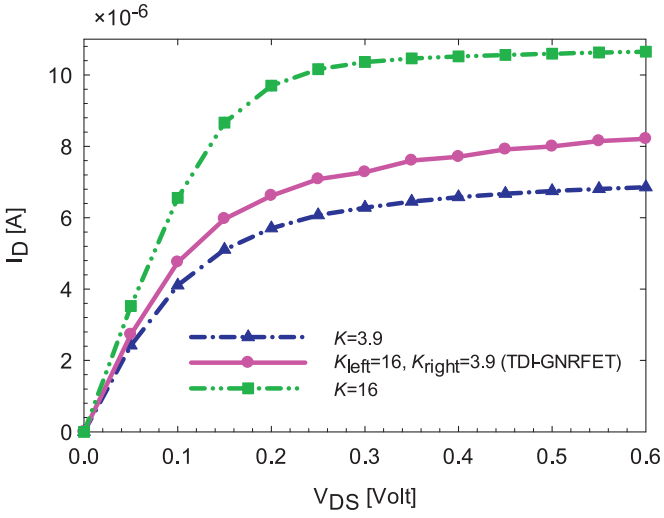

Fig. 6. Simulated current I_{DS} versus V_{DS} for conventional GNRFETs with dielectric constants of $K=3.9$ and 16 and a TDI-GNRFET at $V_{GS}=0.6$ V.

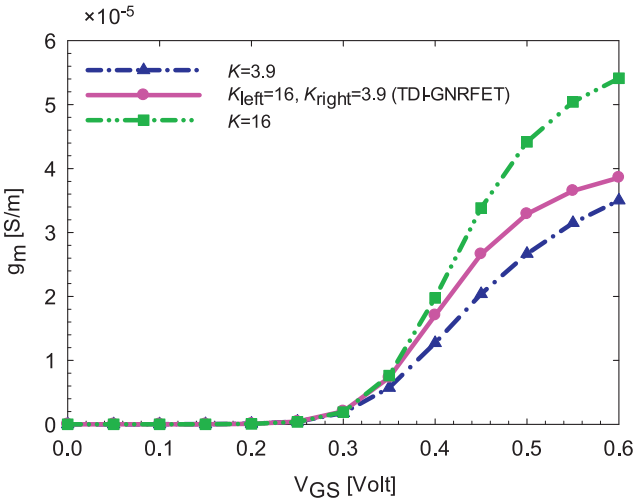

Fig. 7. Transconductance versus the gate voltage for a TDI-GNRFET and GNRFETs with $K=3.9$ and 16 at $V_{DS}=0.6$ V.

emission current in comparison with a GNRFET of low dielectric constant.

Fig. 7 illustrates the transconductance for TDI and conventional GNRFETs. It is given by [15]

$$g_m = \frac{\partial I_D}{\partial V_G} \tag{8}$$

For TDI-GNRFET, the transconductance increases due to the more controllability of the gate on channel near the source in comparison with a GNRFET with low dielectric constant. In addition, it decreases because of the less control ability of the gate on channel at the drain side when it is compared to a GNRFET with high dielectric constant.

4. Two dimensional model

To treat transistor electrostatics analytically, we adopt a capacitance two-dimensional model. It is used to study other characteristics of TDI and conventional GNRFETs. This is a "top-of-the-barrier" MOSFET model which can, however, capture 2-D self-consistent electrostatics and quantum capacitance effects in ballistic mosfets [16].

The carrier density calculation is self-consistently coupled to Poisson's equation solved at the top of the barrier through a simple capacitive model involving the gate insulator capacitance (C_G), drain capacitance (C_D), and source capacitance (C_S). The capacitive model is illustrated in Fig. 8. The potential at the top of the barrier (U_{scf}) is controlled by the gate, source and drain potentials.

The mobile charge is induced in the graphene nanoribbon when an electric field is applied between the drain and source of GNR transistor. The induced charge is evaluated using U_{scf} and the value of the two Fermi levels of E_{F1} and E_{F2}. The amount of induced mobile charge at the top of the barrier is [17]

$$Q_{top} = -q(N_S + N_D) \tag{9}$$

where N_S and N_D are the density of positive velocity states filled by the source, and the density of negative velocity states filled by the drain, respectively. The equilibrium electron density at the top of the barrier is N_0, which is calculated under zero terminal biases. These parameters are determined by the Fermi-Dirac probability distribution as follows:

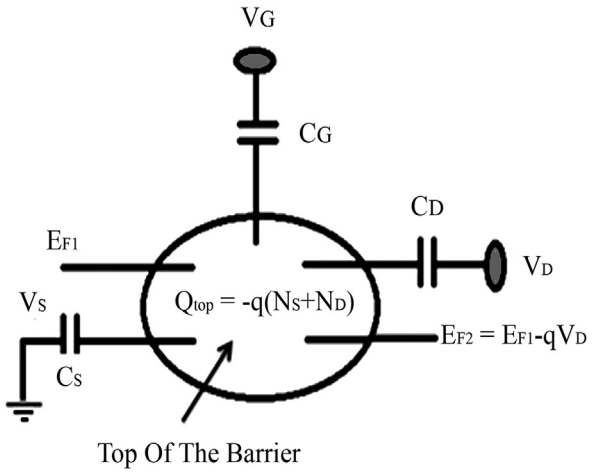

Fig. 8. Two-dimensional circuit model for ballistic transistors.

$$N_0 = \int_{-\infty}^{+\infty} D(E) f(E - E_f) dE \tag{10}$$

$$N_S = \frac{1}{2}\int_{-\infty}^{+\infty} D(E - U_{scf}) f(E - E_{f_1}) dE \tag{11}$$

$$N_D = \frac{1}{2}\int_{-\infty}^{+\infty} D(E - U_{scf}) f(E - E_{f_2}) dE \tag{12}$$

where $D(E)$ is the density of states at the top of the barrier; U_{scf} is the self-consistent voltage at the top of the barrier, E_f is the Fermi level, and f is the equilibrium Fermi function. $E_{f1}=E_f$ and $E_{f2}=E_f-qV_{DS}$ are source and drain Fermi levels respectively. Finding the self-consistent potential involves solving the two-dimensional Poisson equation as shown by the three capacitors in Fig. 8 with the bias induced charge $\Delta N=(N_S+N_D)-N_0$ at their common terminal. So the expression of the total potential U_{scf} becomes:

$$U_{scf} = U_L + U_P \tag{13}$$

where U_L is the Laplace potential at the top of the barrier due to terminal biases with ignoring the presence of the mobile charge in the channel and U_P is calculated using the linearized Poisson equation, where the potential is proportional to the charge unbalance in the channel. The equations of U_L and U_P are as follows:

$$U_L = -q(\alpha_G V_G + \alpha_D V_D + \alpha_S V_S) \tag{14}$$

$$U_P = \frac{q^2}{C_\Sigma}\Delta N \tag{15}$$

where

$$\alpha_G = \frac{C_G}{C_\Sigma},\ \alpha_D = \frac{C_D}{C_\Sigma},\ \alpha_S = \frac{C_S}{C_\Sigma} \tag{16}$$

where C_Σ is the parallel combination of the three capacitors shown in Fig. 8. Afterward, the drain current can be obtained from (17):

$$I_{DS} = \int_{-\infty}^{\infty} J(E - U_{scf})\left[f(E - E_{f_1}) - f(E - E_{f_2})\right] dE \tag{17}$$

where $J(E-U_{scf})$ is the "current density of states" which is expressed as

$$J(E - U_{scf}) = \frac{1}{2} q\left(\frac{2}{\pi}\sqrt{\frac{2(E - U_{scf})}{m^*}}\right) D(E - U_{scf}) \tag{18}$$

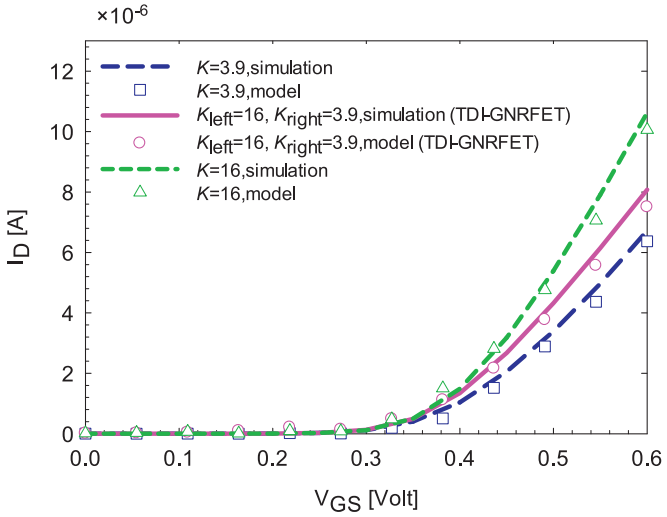

Fig. 9. I_{DS}–V_{GS} characteristics in linear scale for modeling and simulation of TDI and conventional GNRFETs at V_{DS}=0.6 V.

Now, we take the results of the TDI and conventional GNRFETs modeling. Fig. 9 shows I_D–V_{GS} characteristics of modeling and simulation for TDI and conventional GNRFETs in linear scale. As shown in Fig. 9, there is a good agreement between modeling and simulation results. By this matching, other characteristics of GNRFETs can be extracted as following.

Fig. 10 illustrates the mobile charge diagram as a function of gate-source voltage for TDI and common GNRFETs. For GNRFET with high dielectric constant, the gate voltage has a strong effect on the channel, which causes more mobile charges.

The carrier velocity is expressed as [9]

$$\langle v\rangle = \frac{I_D(V_{GS}, V_{DS})}{Q(V_{GS}, V_{DS})} \tag{19a}$$

Therefore, the average velocity of the carrier at the top of the barrier is defined by [9],

$$\langle v\rangle = \frac{I_D(V_{GS}, V_{DS})}{-q[N_S(V_{GS}, V_{DS}) + N_D(V_{GS}, V_{DS})]} \tag{19b}$$

Fig. 11 shows the average electron velocity at the top of the barrier versus gate voltage for TDI and conventional GNRFETs. We

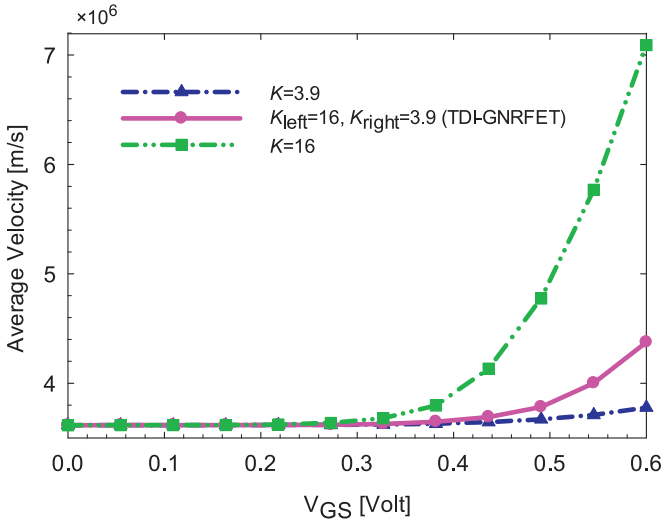

Fig. 11. Average velocity versus gate voltage for a TDI-GNRFET and GNRFETs with K=3.9 and 16 at V_{DS}=0.6 V.

observe that the average electron velocity at the top of the barrier increases with V_{DS}. It is higher for high-K gate insulator.

There is a relation between the local potential and the charge. This effect can be described by a nonlinear quantum capacitance (C_Q) [17].

$$C_Q = \frac{d(qN)}{d(-U_{scf}/q)} = q^2 \int_{-\infty}^{+\infty} D(E)\left(-\frac{\partial f(E-E_F)}{\partial E}\right)dE \tag{20}$$

where $N=N_S+N_D$ is the electron density at the top of the barrier. Quantum capacitance as a function of gate voltage is shown in Fig. 12.

As can be seen, when the gate voltage is high, the barrier height between the source and drain decreases, which increases the electron density in the channel, thus the quantum capacitance increases.

The gate capacitance (C_G) can be modeled as a series combination of insulator capacitance (C_{ins}) and the quantum capacitance (C_Q), that is [18],

$$C_G = \frac{C_{ins}C_Q}{C_{ins}+C_Q} \tag{21}$$

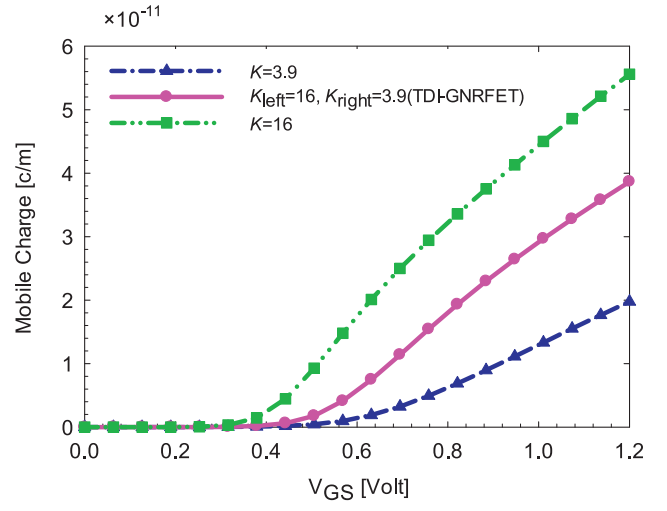

Fig. 10. Mobile charges versus gate voltage for a TDI-GNRFET and GNRFETs with K=3.9 and 16 at V_{DS}=0.6 V.

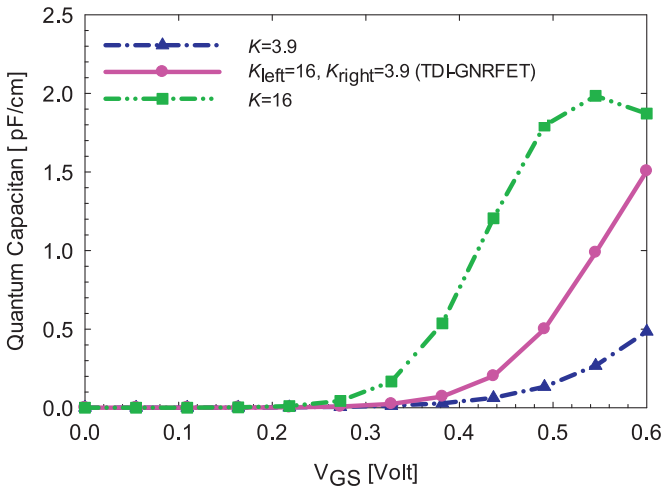

Fig. 12. Quantum capacitance versus the gate voltage for a TDI-GNRFET and GNRFETs with K=3.9 and 16 at V_{DS}=0.6 V.

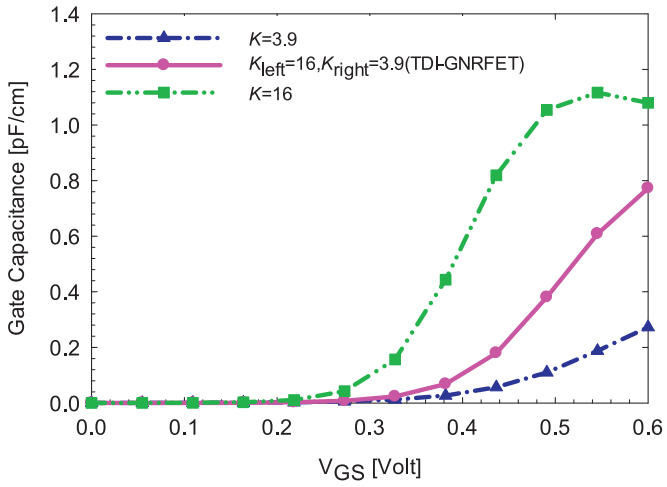

Fig. 13. Gate capacitance versus the gate voltage for a TDI-GNRFET and GNRFETs with $K=3.9$ and 16 at $V_{DS}=0.6$ V.

The gate-insulator capacitance can be calculated by the simple expression [18],

$$C_{ins} = N_G K \varepsilon_0 \left(\frac{W}{t_{ins}} + \alpha \right) \tag{22}$$

where N_G is the number of gates, K is the relative dielectric constant of the gate insulator, t_{ins} is the gate-insulator thickness, and α is a dimensionless fitting parameter.

Fig. 13 shows the variation of C_G versus the gate bias for TDI and conventional GNRFETs at $V_{DS}=0.6$ V. As can be seen, gate capacitance is higher for high-K GNRFET.

Intrinsic delay time (τ_s) is also an important performance metric that characterizes the limitations on switching speed and AC operation of a transistor. Once the gate capacitance is calculated, τ_s is given by [18],

$$\tau_s = \frac{C_G V_{DD}}{I_{ON}} \tag{23}$$

where the On-current is the drain current at $V_G=V_D=V_{DD}=0.6$ V. Fig. 14 shows the variation of switching delay time versus gate voltage for TDI and conventional GNRFETs. We observe that the GNRFET with high dielectric constant has a higher delay time in comparison with others.

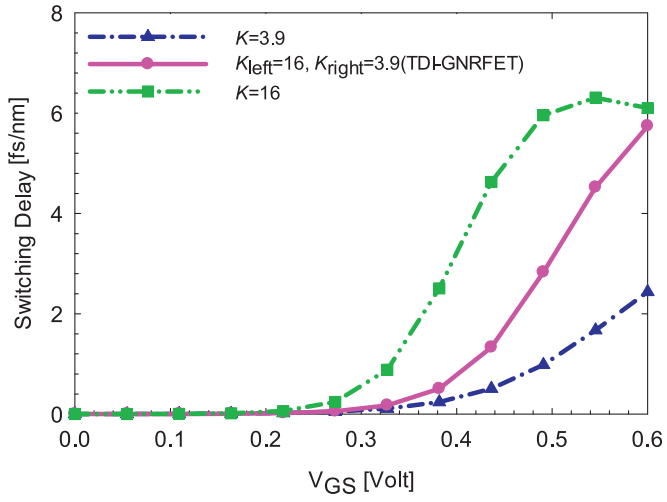

Fig. 14. Switching delay time versus the gate voltage for a TDI-GNRFET and GNRFETs with $K=3.9$ and 16 at $V_{DS}=0.6$ V.

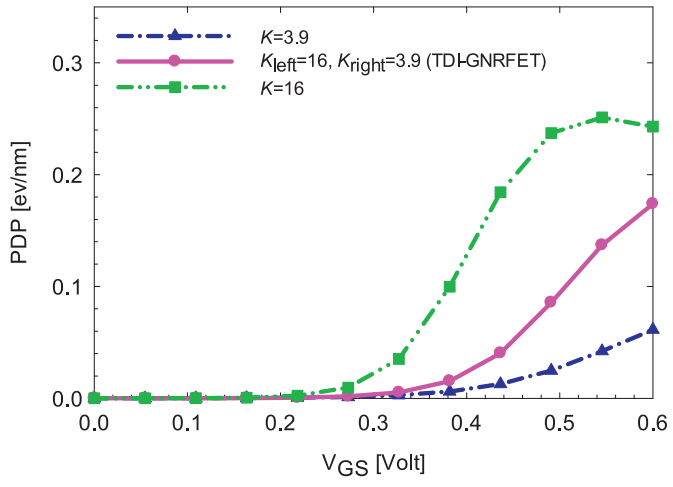

Fig. 15. Power-delay time product versus the gate voltage for a TDI-GNRFET and GNRFETs with $K=3.9$ and 16 at $V_{DS}=0.6$ V.

Power-Delay Product (PDP) is another key parameter in the switching performance of the device. This parameter indicates energy consumed per switching event of the device. The value of PDP can be obtained from [18],

$$PDP = (I_{ON} V_{DD}) \tau_s \tag{24}$$

Fig. 15 illustrates the PDP diagram versus gate voltage for TDI and conventional GNRFETs. We observe that the GNRFET with high dielectric constant has a higher power-delay product in comparison with others.

Another important figure of merit for FETs is the subthreshold swing (SS) defined as [15]

$$SS = \frac{dV_G}{d(\log(I_D))} \tag{25}$$

Table 1 illustrates subthreshold swing for TDI and conventional GNRFETs. We observe that subthreshold swing decreases and is close to its theoretical limit with increasing K. The reason is that using the high gate insulators reduce leakage current and afford low subthreshold swing. At a certain gate voltage, if a high drain voltage is applied, the barrier height can decrease and lead to an increased drain current. Thus, the drain current is controlled by the gate and the drain voltages. This effect is called Drain-Induced Barrier Lowering (DIBL) and is characterized by the number of millivolts of translation per volt of change in drain voltage. For FETs, this effect is defined by reducing the threshold voltage (V_T) and is given as [19,20]

$$DIBL = \frac{\partial V_T}{\partial V_D} \tag{26}$$

Table 1
Subthreshold swing, DILB effect and the capacitances of source and drain for a TDI-GNRFET and GNRFETs with $K=3.9$ and 16.

	Subthreshold swing (SS) (mV/dec)	DIBL (mV/V)	Capacitance (pF/cm)	
			C_D	C_S
GNRFET with $K=3.9$	172.3072	81.9763	0.0249	0.0603
TDI-GNRFET with $K_{left}=16$ and $K_{right}=3.9$	128.6129	55.2951	0.0635	0.1540
GNRFET with $K=16$	83.9373	51.1491	0.1021	0.2477

In a high dielectric constant, DIBL decreases because of the more control of the gate on the channel. This feature can be seen in Table 1 too. Furthermore, this table shows the calculated capacitances for TDI and conventional GNRFETs. For TDI-GNRFET, the amount of C_D and C_S are smaller than high-K GNRFET and bigger than low-K GNRFET. Higher capacitance is caused by greater influence of gate potential on the channel.

5. Conclusion

In this paper, we proposed a new structure for GNRFET with two different gate insulators. This novel structure uses the advantages of high and low dielectrics. In our proposed TDI-GNRFET, the gate length is divided into two equal sections. The gate dielectric at the drain side (right side) is selected from a material with low dielectric constant to decrease the capacitance on the channel near the drain, while the gate dielectric at the source side (left side) is chosen from a material with high dielectric constant to improve On-current and reduce leakage current.

In order to simulate the electronic properties of the proposed GNRFET structure in the ballistic regime, the mode space NEGF coupled with Poisson equation has been used, and the simulated characteristics have been compared with those of conventional GNRFETs. Furthermore, we have used a two-dimensional capacitance model to treat transistor electrostatics analytically.

The results have indicated that the TDI-GNRFET has higher I_{on}/I_{off} ratio, transconductance, mobile charge and average velocity in comparison with the conventional GNRFET with low dielectric constant. In addition, the proposed GNRFET has higher gate, source and drain capacitances. Comparison between the conventional GNRFETs and TDI-GNRFET revealed that the TDI-GNRFET had lower quantum capacitance, smaller intrinsic delay time and shorter power-delay product compared to GNRFET with high dielectric constant. Furthermore, the proposed structure affords better DIBL and subthreshold swing than conventional GNRFET with high dielectric constant.

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