Microwave Class-F and Inverse Class-F Power Amplifiers Designs using GaN Technology and GaAs pHEMT

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ABSTRACT **— This paper presents the designs and results of two high-efficiency harmonics-tuned microwave power amplifiers (PA): the first one is a 2 GHz class-F PA in monolithic integrated circuit (MMIC) by using GaN HEMT technology, and the other one is a 2.45-GHz inverse class-F PA using packaged GaAs pHEMT devices with PCB technology. In the class-F MMIC PA, field-plated GaN HEMT device is used for high-power performance. The 2.0-GHz class-F MMIC PA achieves a PAE of 50%, 38 dBm output power, and 6.2 W/mm power density. The inverse class-F PA at 2.45 GHz achieves 22.6 dBm output power and 73% PAE at 3 dB compression, and has very low cost.**

Index Terms **— Power amplifiers, high efficiency, class F, inverse class-F, MMIC, GaN HEMT, GaAs**

I. INTRODUCTION

Radio frequency (RF) and microwave PA is the most expensive component in radio transmitters of modern communications and radar systems. A high PAE is one of the key requirements in RF/microwave PA designs, as it will lead to low power consumption, reduced cooling requirements, small battery size and low cost in RF front ends. To achieve a high PAE, it is necessary to drive the active device heavily into compression, leading to highly non-linear behaviour. Popular design techniques include those based on harmonic manipulation such as Class-F and Inverse Class-F [1,2], or switching mode such as Class-E [3,4], etc. The characteristics of these different high-efficiency modes are best appreciated by observing the shape of the voltage and current waveforms at the output of the active device. In contrast to the old days when the class-F PA designers focused on the harmonics tuning at the output only, many recent work on class-F and inverse class-F PAs have shown the importance of considering the harmonics tuning at both the input and the output. For example, the 2nd harmonic input termination has been shown experimentally to have a significant influence on efficiency and linearity [2,5], demonstrating the need to integrate it into the design process. Many work on harmonics-tuned PA have been reported by using GaAs devices for class-F PA in MMIC or hybrid circuits [6-10], and SiGe HBT for MMIC class-F PA [11], etc. This paper presents the design and results of two high-efficiency PAs: one is a 2 GHz class-F MMIC PA by using GaN HEMT technology, and the other one is a very low cost inverse class-F PA at 2.45 GHz which uses packaged GaAs pHEMT devices and printed circuit board (PCB) technology. A multi-harmonics source pull/load pull simulation-based design methodology is employed.

II. PRINCIPLES OF CLASS-F AND INVERSE CLASS-F PA AND DESIGN METHDOLOGY

A. Class-F and inverse class-F PA Basics

The class-F PA achieves high efficiency and high output power by using harmonic resonators in its output network to shape the drain waveforms in the time domain. Ideally, the load must be short at even harmonics and open at odd harmonics. The drain voltage waveform includes odd harmonics and approximates a square wave, while the drain current waveform includes even harmonics and approximates a half sine wave.

In practical realizations of microwave class-F PA, only the first three harmonics are considered, as higher harmonics can be shorted by the output drain capacitance C_{ds}. The input harmonics tuning is very important here as it plays an important role in shaping the driving waveform at the device input, and modifying the harmonic components at the device output, etc [6].

In the inverse class-F PA, the load must be short at odd harmonics and open at even harmonics. The drain current waveform includes odd harmonics and approximates a square wave, while the drain voltage waveform includes even harmonics and approximates a half sine wave. Again, up to the third harmonics are considered at both the input and the output networks.

B. Design Methodology

The design methodology employs a multi-harmonics load-pull/source-pull approach to find optimum harmonic loads at both the input and output of the active device at the first three harmonics [2]. This approach, which is simulation-based, is an extension of the one proposed in [6] for experimental device characterization. The advantage of using a simulation-based approach is that it does not need an expensive multi-harmonic load-pull/source-pull experimental setup as well as time-consuming and potentially troublesome measurements. Instead, the process is carried out with a commercial Harmonic-Balance (HB) simulator using a non-linear model for the transistor.

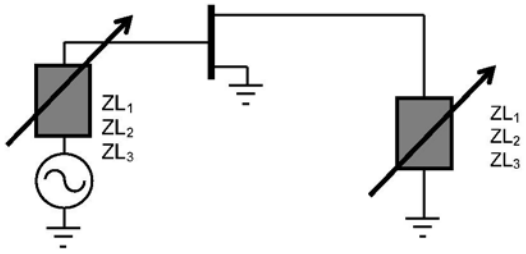

Fig. 1. Multi-harmonics load-pull/source-pull simulation

In the multi-harmonics load-pull/source-pull methodology, the variables are varied one at a time in a determined order based on relative importance and reported interactions, leading them to be successively adjusted to optimum values. The designs procedures are:

- The harmonic loads shown in Fig. 1 are initially set to their ideal values. For example, in Class-F PA designs, the output 2nd and 3rd harmonic load ZL_2 and ZL_3 are set to be zero and infinite respectively, whereas the other harmonic loads are set to be 50 Ω; in inverse class-F design, the ZL_2 and ZL_3 are set to be infinite and zero respectively;
- A fundamental load-pull simulation is performed, *i.e.*, the complex output load ZL_1 is varied to sweep the Smith chart;
- ZL_1 is set to the determined optimal value and ZS_2 is swept by source-pull simulation so as to fix it to its optimum value. At this stage, it is necessary to re-optimize ZL_1 to take into account the influence of the new ZS_2 [6];
- The remaining harmonic loads ZL_2, ZL_3 and ZS_3 are then successively swept ant set to their optimum values. Throughout the process, the fundamental source impedance ZS_1 is adjusted automatically for each simulation point to achieve a conjugate match of the input impedance of the device, thus maintaining a constant drive level;
- After the optimized loads have been determined at both the input and the output for the first three harmonics, input/output lumped-element networks are synthesized to achieve the optimized harmonic loads have been determined at both the input and the output;
- Distributed components, such as Spiral conductors and MIM capacitors in MMIC, and quarter-wave bias line and open stub in PCB, will need to be accurately characterized through electromagnetic simulations (here EM Momentum in ADS from Agilent Technologies is used);
- The whole circuit including the biasing circuit will be optimized again and checked by viewing the drain waveforms, before the final circuit is produced.

III. 2GHZ CLASS-F mmic PA using GAn TECHNOLOGY

A. Circuit Design

GaN devices are very useful for compact high-power microwave PA applications. The 2.0 GHz MMIC class-F PA uses a field-plated GaN HEMT device with a 0.7 μm gate length, 8x125 μm gate width and 0.7 μm field-plate length. Fig. 2 shows the schematic of the PA. The harmonic trap (L_3, C_3) at the drain is used to tune the 2nd harmonic, and the output network (L_3, C_3, L_4, C_4) is used to terminate the 3rd harmonic and transform the 50 Ω load to optimum impedance at the drain output, as required for class-F operation. A harmonic trap (L_2, C_2) at the gate is employed for input harmonic tuning. As the device is potentially unstable, a stability resistance (R_1) is added at the input. The circuit simulation is carried out by using the HB simulator in ADS. A bias-dependent and scalable large-signal EEHEMT1 model was used for simulations. Fig. 3 shows a photo of the PA, which measures 1.9 mm by 1.5 mm. To validate the class-F design, simulated drain voltage and current waveforms are shown in Fig. 4, where a quasi class-F operation is demonstrated.

B. Measurements of the 2.0 GHz class-F MMIC PA

The circuit was fabricated on a SiC substrate using MOCVD-grown GaN. The PA is measured at a drain voltage of 28 V. A maximum power of 36 dBm is achieved, corresponding to a power density of 4.0 W/mm. The maximum PAE is 50.4%, and the gain is about 10 dB. The simulated and measured results of output power match well. Fig. 5 shows the performance of PA measured at a drain voltage of 35 V. The PA achieves a maximum power of 38 dBm, corresponding to a power density of 6.2 W/mm. The gain is about 10 dB, and a maximum PAE of 50 % is achieved in this case.

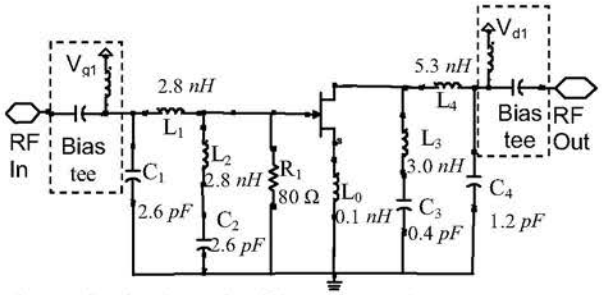

Fig. 2. Circuit schematic of the 2.0 GHz class-F PA

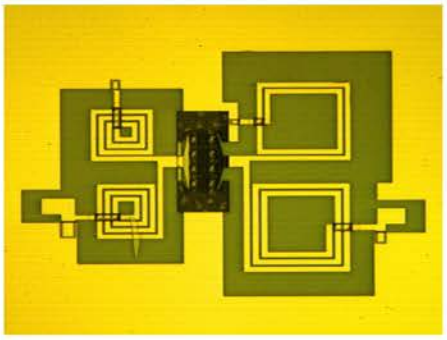

Fig. 3. Photo of the chip of PA

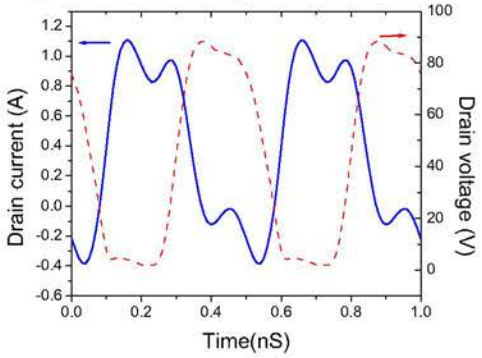

Fig. 4. Drain current and voltages waveforms

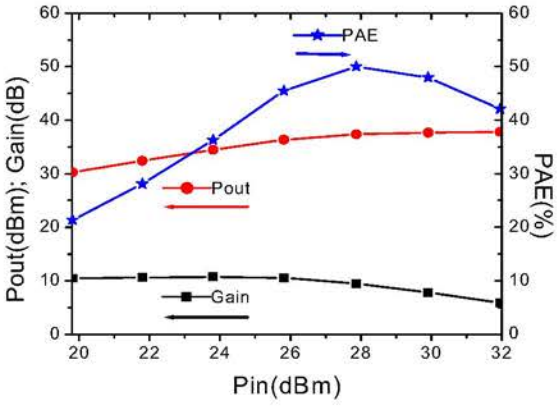

Fig. 5. Power, gain and PAE results of 2.0 GHz PA with a Vds of 35 V

IV. LOW-COST 2.45 GHZ INVERSE CLASS-F PA USING PACKAGED GAAS PHEMT IN PCB TECHNOLOGY

A. Circuit Design

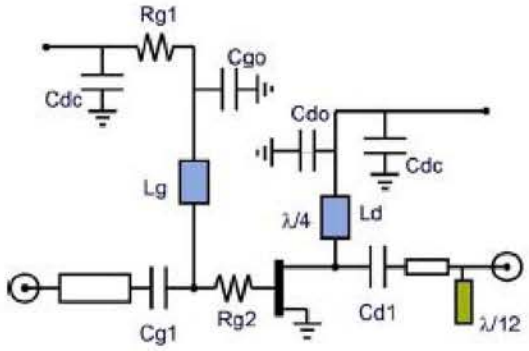

Fig. 6. Circuit configuration of the inverse class-F PA

Very low-cost RF PAs can be realized by using low-cost packaged devices and PCB technology. Here GaAs pHEMT device ATF 34143 from Agilent Technologies is employed because of its low cost and the availability of its nonlinear model from the company's web site. The design is based on the multi-harmonics source-pull/load-pull simulation, i.e., the input/output networks are optimized to achieve the desired harmonic loads up to the third harmonic frequency.

Fig. 6 shows the circuit topology, where the DC biasing is done by using a quarter-wave line shorted by a RF bypass capacitor. Resistors are used in the gate bias circuit and on the gate for achieving the stability. A $\lambda/12$ open-circuited microstrip stub is used to control the 3rd harmonic at the output. The 2nd harmonics at the input and output are provided by adjusting the length of quarter-wave bias lines. To check the mode of PA operation, the voltage and current waveforms at the drain output are simulated by using ADS and shown in Fig. 7, which confirms the quasi inverse class-F mode of operation.

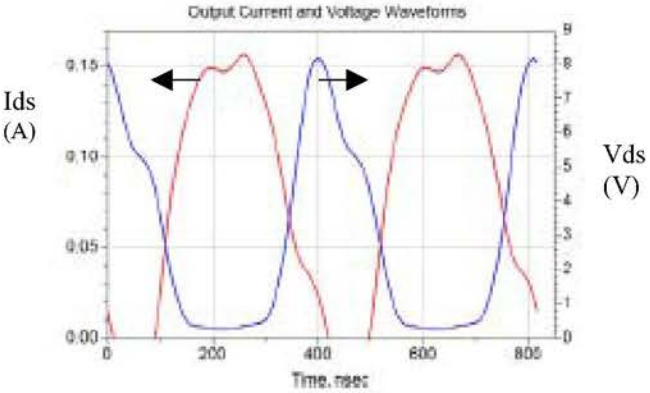

Fig. 7. Simulated drain waveforms in time domain

B. Experimental implementations

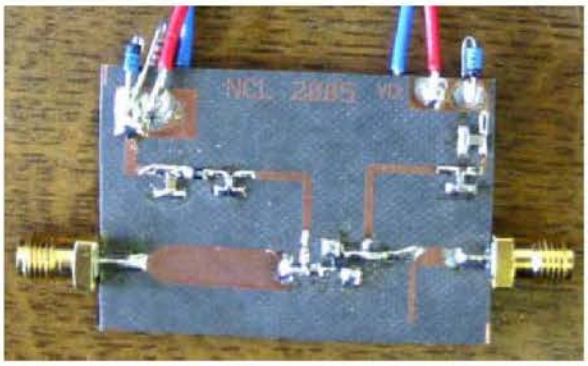

Fig. 8. Photo of the inverse class-F PA

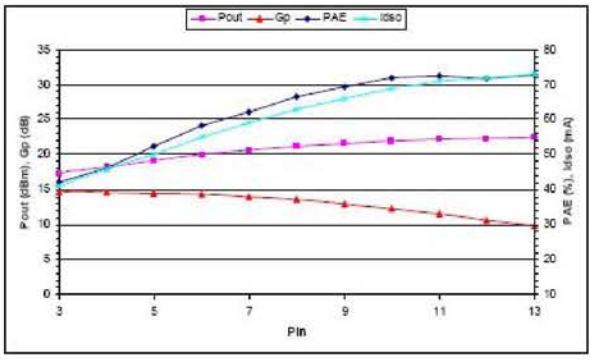

Fig. 9. Measured performance versus input power (f=2. 45GHz, Vds0=3V)

The inverse class-F PA was fabricated by using PCB technology. It uses a Duroid substrate (Er=2.33) with a thickness of 0.79 mm. Fig. 8 shows the photo of the PA, which has a size of 48× 32 mm. The circuit was biased in class-AB for 21 mA drain current and 3 V drain bias voltage. The measured results of Pout, Gain and PAE are given in Fig. 9. The circuit achieves 21.3 dBm output power at 1dB compression together with 13.6 dB gain and 68% PAE. In saturation, it achieves 22.6 dBm output power and 73% PAE.

V. CONCLUSIONS

Designs and results of two high-efficiency harmonics-tuned microwave PAs are presented: the first one is a 2 GHz class-F MMIC PA using GaN HEMT technology, and the other one is a 2.45 inverse class-F PA using packaged GaAs pHEMT devices with PCB technology. The 2.0-GHz class-F MMIC PA achieved a PAE of 50%, 38 dBm output power, and 6.2 W/mm power density. The inverse class-F PA at 2.45 GHz achieved 22.6 dBm output power and 73% PAE at 3 dB compression, and has very low lost due to the use of PCB technology and cheap devices. Further work is to improve the linearity of high-efficiency PAs using LINC technique [11] and to realize highly compact RF front ends using active antennas [12], etc.

ACKNOWLEDGEMENT

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