Assembly and Wiring Technologies on PLC Platforms for Low-Cost and High-Speed Applications

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Abstract

The hybrid integration of silica-based planar lightwave circuit (PLC) platforms and semiconductor opto-electronic devices is a technology that shows promise for the development of highly functional opto-electronic modules. These modules are expected to offer both optical signal and electrical signal processing functions. The silica PLC has already realized various optical signal processing functions such as those in the couplers, the switchs and the arrayed waveguide grating (AWG) wavelength multiplexers. Therefore, the technologies to improve the performance of electrical circuits on PLC platforms are significant to realize high-functional opto-electronic modules. We introduced a PLC platform with a silica-on-terraced silicon (STS) structure. Using the PLC platform, we can easily align opto-electronic devices to the silica wave guide. However, the silicon substrate caused parasitic capacitance and propagation loss in the electrical circuits on the platform.

We developed several technologies to improve the electrical circuit performance of the PLC platform considering both low-cost and high-speed applications. The PLC platform for a low-cost applications employed thin film solder with a small silicon terrace area and wires on the overcladding. These technologies could decrease the parasitic capacitance and also could realize the simple structure that suited low-cost applications. The 50-Mbit/s optical wavelength-division multiplexing (WDM) transceiver that employed these technologies showed excellent receiver sensitivity of -37 dBm at a burst signal of 50-Mbit/s. The PLC platform for high-speed applications used solder bumps and coplanar transmission lines. These technologies could minimize the CR time constant and electrical propagation loss of coplanar transmission lines. These technologies were applied to wide-bandwidth transmitter and receiver modules. The transmitter module showed a very wide 3-dB bandwidth of 11 GHz and the receiver module also showed a wide 3-dB bandwidth of 8 GHz. These modules operated successfully at a 10-Gbit/s NRZ signal with a receiver sensitivity of -8 dBm. The excellent performance of the WDM transceiver module and the 10-Gbit/s transmitter and receiver modules indicated that the technologies employed in these PLC platforms effectively suppress electrical deterioration due to the use of a silicon substrate.

I. Introduction

Since the amount of data flow on networks is rapidly increasing, extensive studies have been carried out on systems using WDM and time-division multiplexing (TDM). These systems require highly functional modules that integrate optical signal processing, opto-electronic signal conversion and electronic signal processing functions. For example, the WDM transceiver module for a subscriber system [1] needs the functions of WDM and both O-E and E-O signal conversion. On the other hand, the high-speed photoreceiver module for an optical interconnection system [2] needs photo diodes (PDs) and preamplifiers that operate at a high bit rate of over 10 Gbit/s. Therefore, the electrical circuits on a silica PLC platform need the same performance as conventional electrical modules that consist of electrical integrated circuits (ICs).

The operation speed and receiver sensitivity of opto-electronic modules using a PLC platform has been limited by the parasitic capacitance and electrical propagation loss in transmission lines. These problems are due to the conductance of the silicon substrate. The silicon substrate cause large parasitic capacitance between wires and solder pads. The capacitance increases the CR time constant and results in poor receiver sensitivity. Furthermore, the larger loss tangent (tan δ) of the silicon substrate results in a large propagation loss at the transmission line [4]. This loss limits the operation bandwidth of modules for the high-frequency applications such as transmitter and receiver modules for the 10-Gbit/s optical interconnection systems.

We demonstrated several modules employing PLC platforms for both low-cost applications and high-speed applications. The 50-Mbit/s optical WDM transceiver for the subscriber systems was composed of a dielectric WDM filter, a laser diode (LD) and PDs assembled on the surface of a PLC platform [1]. This module required low capacitance at the assembly and wiring region as well as a simple structure to reduce its fabrication cost. The 10-Gbit/s transmitter and receiver array modules for the high-speed optical interconnection systems were composed of an LD array and a monolithically integrated photoreceiver array flip-chip bonded on the PLC platforms [2, 3]. These modules needed minimized parasitic capacitance in the assembly region and low loss transmission lines in the wiring region. Therefore, these two types of modules employed different technologies for the assembly region and the wiring region to achieve high performance.

In this paper, we will describe the technologies used in the WDM transceiver module and the 10-Gbit/s optical transmitter and receiver modules. Section II shows the basic configuration of the silica-based PLC platform and its drawbacks in realizing the high-performance electrical circuits. Section III presents the technologies to achieve low capacitance solder pads for low-cost and high-speed applications. Section IV discusses

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the technologies for the low capacitance wiring for the low-cost applications and the low-propagation-loss transmission lines for the high-speed applications. In Section V, the configuration and performance of the two types of modules fabricated using these technologies are shown.

II. Basic configuration of the PLC platform

Figure 1 shows the schematic illustration of the silica-based PLC platform. This platform consists of three regions. The PLC region employs a embedded low-loss silica waveguide formed on the terraced silicon substrate. This configuration is called the silica-on-terraced silicon (STS) structure [5]. The silica waveguide structure was fabricated using frame hydrolysis deposition (FHD). This is the same technique as conventional silica-based PLCs [6]. Therefore, the versatile optical circuits already obtained by silica-based PLC are applicable to the PLC platforms. The assembly region consists of the silicon terraces and the solder pads. The semiconductor opto-electronic devices are flip-chip bonded to this region and electrically connected by solder. The wiring region is used to interconnect the power lines and signal lines between the opto-electronic devices and the circuits outside the module. The electrical integrated circuits (IC's) are also able to be assembled on this region.

Figure 2 shows the schematic cross-section of the PLC platform. The surface of the silicon terrace is formed to be an exact height in reference to the silica waveguide core. Therefore, the height of the waveguide core of the silica waveguide and the opto-electronic device can be easily aligned by contacting the surface of the device against the silicon terrace [7] . The silicon terrace also acts as a heat sink for the semiconductor devices. The solder and the electrode are formed by the evaporation and the lift-off process. The insulation between the solder and the silicon terrace is achieved by silica film with a thickness of around 0.5 μm. This thin silica film causes large capacitance between the solder and the silicon terrace. The electrode in the wiring region is formed on the silica undercladding to decrease the effect of the silicon substrate.

III. Technologies for Device Assembly Region

Figure 3 is the close-up of a conventional assembly region. The parasitic capacitance appears between the solder film and the silicon terrace where the silica thickness is comparatively thin. This capacitance can be decreased using thick silica film between the solder and the silicon terrace. However, the thicker silica film lowers the accuracy of mechanical contact alignment for the vertical direction. Therefore we employed two technologies to reduce the parasitic capacitance in the assembly region. In the first, we used the solder film with a smaller-area silicon terrace. In the second, we employed the solder bump and the bonding pads formed on the undercladding. The former technology is suited to low cost application because of its simple structure. The latter is used for high-speed application due to its lower parasitic capacitance.

Figure 4 shows the schematic cross-section of the assembly region employing the small-area silicon terrace. The terrace

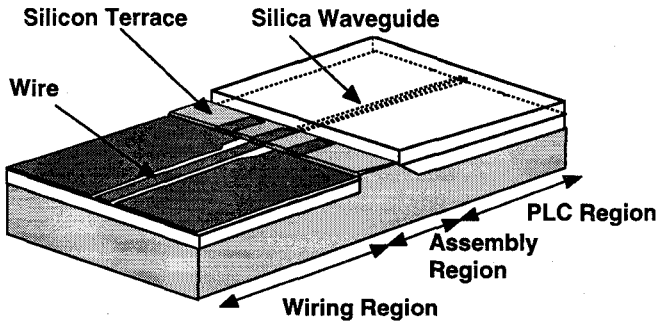

Figure1. Schematic configuration of PLC platform

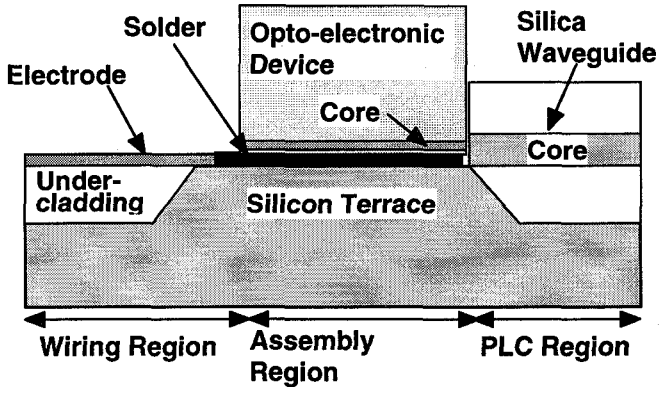

Figure 2. Cross-sectional view of PLC platform

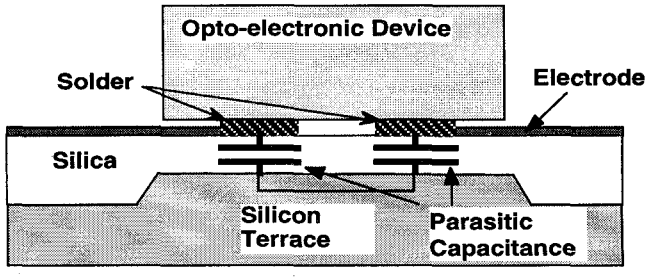

Figure 3. Parasitic capacitance at assembly region

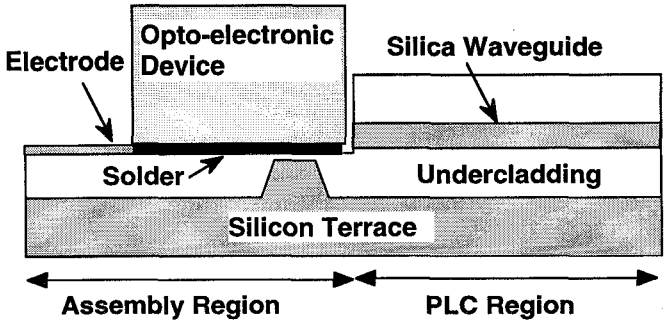

Figure 4. Assembly region using small-arrea silicon terrace

area is minimized to a sufficient size to hold the chip at an accurate height. In this structure, most of the wire area can be formed on the silica undercladding the thickness of which is more than 10 μm. This structure is formed by two fabrication steps; (1) gold electrode evaporation and lift off and (2) Au/Sn eutectic solder film evaporation and lift off. This simple fabrication process is suited to the low cost applications. However, a greater reduction in the parasitic capacitance in the silicon terrace is required for application where 10-Gbit/s operation is needed.

Figure 5 shows the schematic configuration of the assembly region for the high-speed operation [8]. In this structure, all bonding pads are formed on the undercladding to minimize the parasitic capacitance between the pads and silicon substrate. To facilitate vertical-direction mechanical contact alignment using the silicon terrace, solder bumps are employed to connect the opto-electronic device and the PLC platform. This structure was formed by the following process; (1) gold electrode evaporation and lift off, (2) silica glass sputtering followed by contact window opening using reactive ion etching (RIE), (3) evaporation of the Ti/Pt/Au solder pad and lift off and (4) Au/Sn eutectic solder film evaporation and lift off. The solder and the solder pad were designed so that the bump height after reflow is higher than the gap between the opto-electronic device and the electrode (shown by "g" in Fig. 5). The height of the bump was designed by choosing the ratio of the solder film diameter and the solder pad diameter. Figure 6 shows the measured relationship between the diameter ratio and the solder bump height after the reflow. This figure reveals that a diameter ratio of 1.5 can be used for a PLC platform whose gap (g) is less than 10 μm. The fabrication process for the solder bump is rather complicated but the parasitic capacitance can be minimized by using undercladding.

IV. Technologies for the Wiring Region

For low-cost applications where the operation bandwidth is under 1 GHz, the main concern about wiring is the reduction of parasitic capacitance. As described in Section III, the parasitic capacitance can be decreased by inserting silica undercladding between the electrode and the silicon substrate. However, the electrode on the undercladding still has large capacitance when the length of the wire is over 1 mm. In this case, we employ the electrode on an overcladding. The silica thickness is the sum of the undercladding and the overcladding. Therefore, the parasitic capacitance is able to be decreased to the half of that on the undercladding. The electrode on the overcladding can be formed in the same process that the electrode in the assembly region is made. Therefore, this structure does not increase the fabrication steps.

We used a coplanar line or a microstrip line on the platform for wide bandwidth application. The coplanar line was used to connect the solder pad and the wire-bonding pad. However, the propagation loss of the coplanar line formed on the PLC platform was larger than that of the coplanar line formed on the alumina substrate. For example, the propagation loss of the coplanar line on the 1.5-μm thick silica layer was 17 dB/cm at 10 GHz. This is due to the larger loss tangent (tan δ) of the silicon

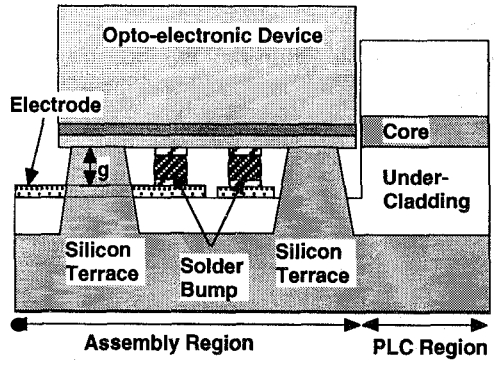

Figure 5. Assembly region using solder bumps

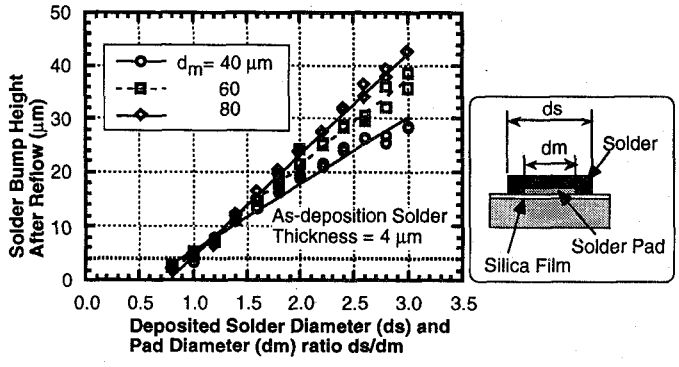

Figure 6. Solder bump height after reflow

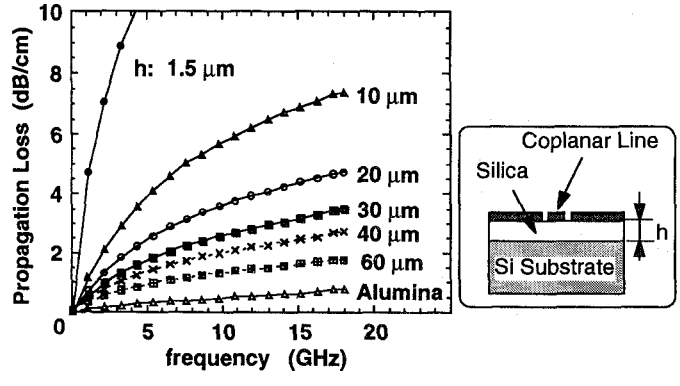

Figure 7. Coplanar line loss at variouse silica thicknesses

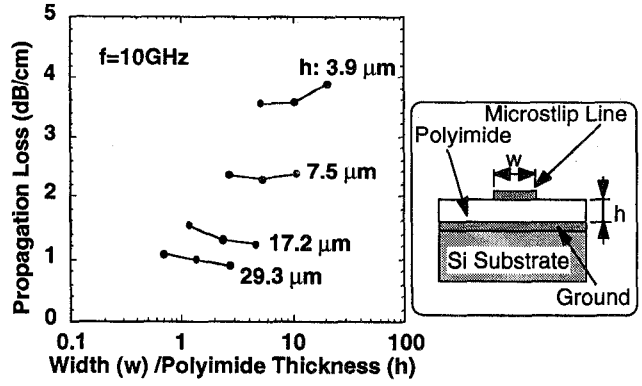

Figure 8. Microstrip line loss at different polyimide thicknesses

substrate. In order to reduce propagation loss, the coplanar line was formed on the silica undercladding [4]. Figure 7 shows the frequency dependence of propagation loss at different silica thicknesses under the electrode. This figure reveals that the loss decreases as the thickness of the undercladding increases. However, the thick cladding results in comparatively large bending of the substrate because of the thermal expansion coefficient difference between the silica and silicon. To suppress this bend, the thickness of the undercladding is designed to be around 25 μm. Therefore, the silica layer thickness on the assembly and wiring region is 15 μm when the height of the solder bumps is 10 μm. The measured propagation loss of the coplanar line on the 15-μm thick undercladding is about 4 dB/cm at 10 GHz. This loss is still larger than that of the coplanar line formed on the alumina substrate but the coplanar line is applicable when the wire length is short.

The microstrip line on the PLC platform has the advantage of being insensitive to undercladding thickness. This is because the ground electrode shields the electrical field to the silicon substrate [4]. The microstrip line is composed of a lower electrode on the platform which acts as a ground, polyimide insulation layer and upper electrode for the wiring. The two electrodes were formed by gold evaporation and lift off. The propagation loss of the microstrip line depends on the thickness of the polyimide. Figure 8 shows the measured propagation loss of the microstrip lines at different polyimide thicknesses. For example, a polyimide thickness of 29 μm realizes 0.9 dB/cm propagation loss at 10 GHz. Therefore, the microstrip line can be used for longer electrical interconnection on the PLC platform.

V. Hybrid Opto-electronic Modules using PLC Platform

We developed two types of opto-electronic modules using the technologies. One was the 50-Mbit/s WDM transceiver for the subscriber system and the other was the 10-Gbit/s optical transmitter and receiver modules for optical interconnection. These two types of modules employed different technologies for the assembly region and the wiring region to realize high-performance operation.

Figure 9 shows the schematic configuration of the WDM transceiver module [9]. This module receives and transmits 1.3-μm wavelength 50-Mbit/s signals at the COM port. It also receives a 1.55 μm wavelength signal from the COM port and passes it to the other optical port. The WDM function is realized by a dielectric filter inserted at the silica waveguide. Three opto-electronic devices were flip-chip bonded; a spot size converted laser diode (SS-LD) [10] and two waveguide photo diodes (WGPD's) [11]. One WGPD was used as the light power monitor for the auto-power-control (APC) operation of the LD and the other WGPD was used for the optical signal receiver.

We chose a simple structure for the assembly and the wiring region to reduce fabrication costs. The assembly region employed solder film on a small-area silicon terrace. The wiring region employed electrodes on the overcladding. The wires at

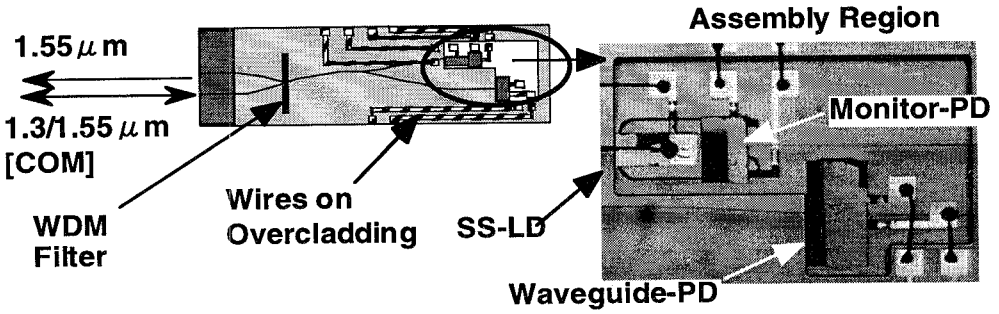

Figure 9. Scheamtic configuration of WDM transceiver

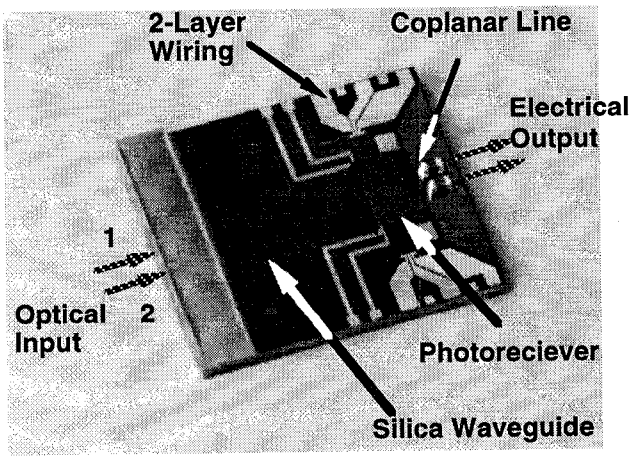

Figure 10. Configuration of 10-Gbit/s reciever submodule

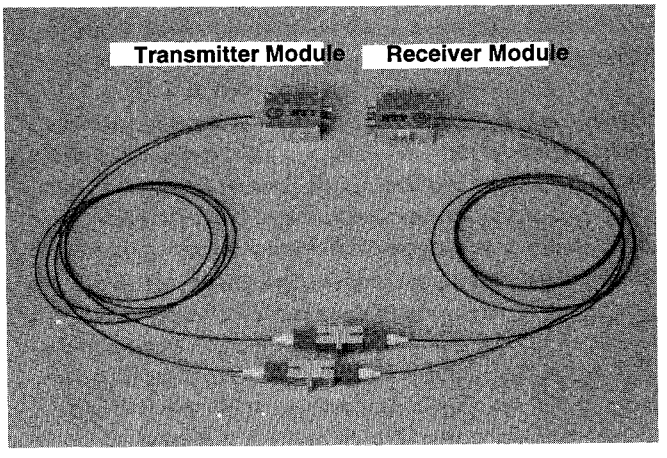

Figure 11. Phograph of 10-Gbit/s modules

the assembly and the wiring regions were connected by bonding wires. The combination of the small-area silicon terrace and the wiring on the overcladding, decreased the parasitic capacitance between the wires for the receiver circuit to 0.1 pF. This low capacitance resulted in good receiver sensitivity of -37 dBm at a 50 Mbit/s burst signal.

Figure 10 shows a photograph of the 10-Gbit/s photoreceiver submodule [2, 8]. The configuration of the 10-Gbit/s transmitter submodule was almost the same [3]. These submodules used the same technologies to achieve a wide operation bandwidth. The assembly region employed a solder pad formed on the undercladding to minimize parasitic capacitance. The receiver module used 16 In solder bumps to flip-chip bond the monolithic photoreceiver array. The transmitter module used 8 Au/Sn bumps. The signal lines at the wiring region used the coplanar lines on the undercladding. The wire length was as short as 1.5 mm for the receiver submodule and 1 mm for the transmitter submodule. In addition, the power lines used two-layer wiring to reduce parasitic inductance on the wire and to obtain the electrically-stable ground electrode. The wires consisted of polyimide insulation layer sandwiched between two gold electrodes. Two chip capacitors and two chip resistors were also assembled on the receiver and transmitter submodules, respectively. The chip capacitors were used to cut the DC voltage on the output signal of the receiver submodule and the resistors were used to provide 50-ohm input impedance for the transmitter submodule.

The two submodules were assembled on packages to evaluate the performance at 10-Gbit/s operation. Figure 11 shows a photograph of these modules. The size of the module was 36 x 39 mm. The receiver module showed a responsivity of 0.16 A/W at a wavelength of 1.55 μm. Figure 12 shows the frequency response of the receiver modules. The module showed a 3-dB bandwidth of 7.8 GHz. This performance was almost the same with the on-wafer measurement results of receiver submodule. This bandwidth was mainly due to the photoreceiver bandwidth. Figure 13 shows the CW light output power against current (I-L) characteristics of the transmitter module at room temperature. The output power was 0.87 and 0.79 mW at an injection current of 50 mA. Figure 14 shows the frequency response of the module. The transmitter module showed a very wide 3-dB bandwidth of 11 GHz. The obtained bandwidth was limited by the characteristics of the discrete LD.

Back-to-back bit-error-rate characteristics were measured using these modules. Figure 15 shows the measured bit-error-rate characteristics at 10 Gbit/s NRZ. During the measurement no external equalization was used. These characteristics show that these modules have sufficient bandwidth to operate at 10 Gbit/s. From this figure, the measured sensitivity was -8 dBm at a bit error rate of 10^{-9}. The typical receiver sensitivity of the monolithic receiver array measured by on-wafer measurements was around -15.5 dBm [12]. Therefore the sensitivity difference between the photoreceiver chip and the module was about 7.5 dB. The optical loss of the receiver module was estimated to be about 6 dB. This includes the optical loss due to several reasons;

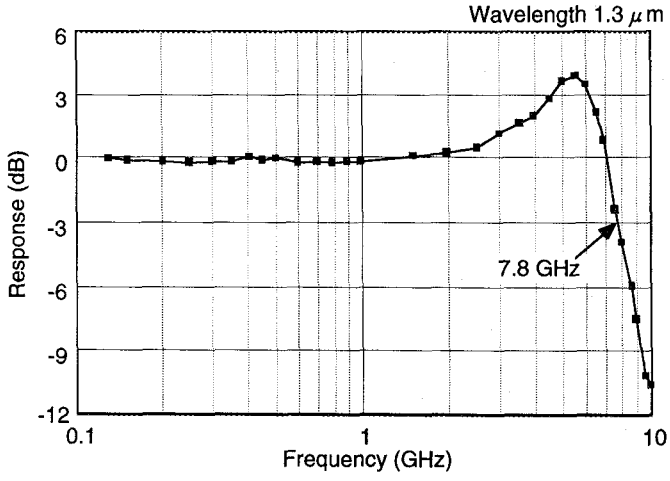

Figure 12. Frequency response of 10-Gbit/s receiver module

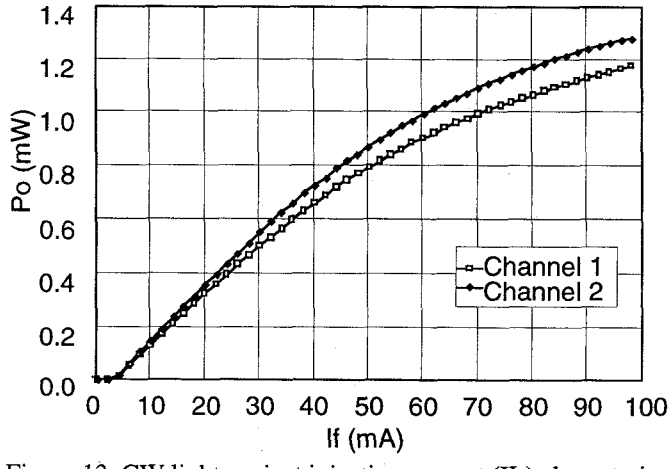

Figure 13. CW light against injection current (IL) characteristics of the transmitter module at room temperature

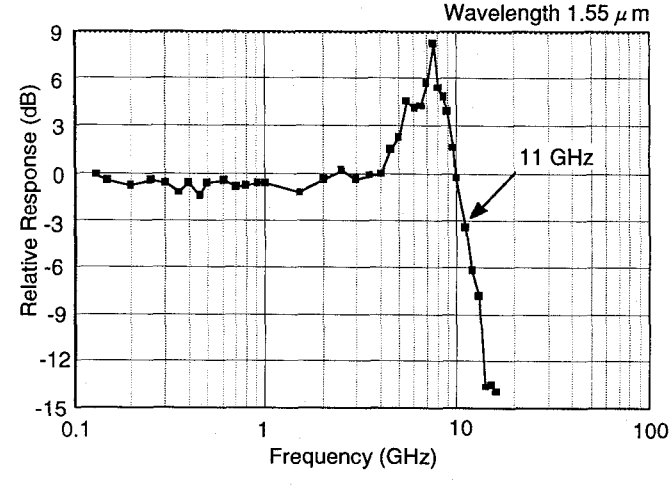

Figure 14. Frequency response of 10-Gbit/s transmitter module

the mode-field difference between the silica wave guide and the monolithic photoreceiver, the misalignment of the photoreceiver array chip against the silica waveguide core and optical propagation loss in the PLC waveguide. The other 1.5 dB difference may have been due to pulse shape deterioration.

VI. Summary

We described the assembly and wiring technologies employed on PLC platforms. Solder film on small-area silicon terraces and wire formed on the overcladding were used to reduce parasitic capacitance. Using these technologies, we fabricated WDM transceiver module for low-cost applications. This module showed a good receiver sensitivity of -37 dBm at a burst signal of 50 Mbit/s. We also employed solder bumps and coplanar lines on the undercladding to minimize the parasitic capacitance in the solder pads and reduce propagation loss in the coplanar transmission lines. We used these technologies to fabricate wide-bandwidth transmitter and receiver array modules. These modules operated successfully at a 10 Gbit/s NRZ signal showing a receiver sensitivity of -8 dBm. The combination of these hybrid integration technologies and highly functional silica-based optical circuits should make the PLC platform a key component in future systems using the wavelength-division multiplexing and time-division multiplexing.

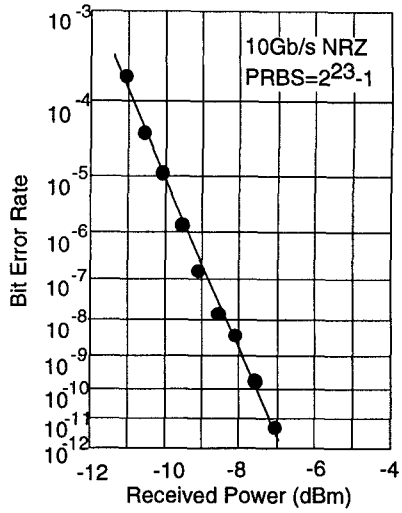

Figure 15. Back-to-back BER characteristics of 10-Gbit/s modules

Acknowledgments

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