Impact of Architecture on Performance of USB to Serial Adapters

Introduction

With the ever-increasing computing power of today's PCs it is necessary to have supporting technology that is able to keep up and not bog down the system. Human interface devices and other peripherals that attach to a PC are usually the bottleneck when it comes to overall processor speed and data throughput.With processors working in excess of 1.5 GHz, hard disks that operate at a minimum of 7200 rpm, and CD-ROMs that read and write at upwards of 32x, it is necessary to have external I/O devices that operate faster than the 115 kbps standard parallel port.

Several technologies have been developed over the past ten years that address this issue of slower external I/O devices. Two of the hottest technologies are USB and Fire Wire. Both of these technologies have been developed to increase the overall data throughput between the processor and external devices.These technologies have allowed, and will allow, higher-bandwidth peripherals to be developed and implemented for the PC, digital video cameras, broadband digital cable modems, and HDTV to name a few. The technology is quickly matching the pace of the computing power of a PC.

This paper focuses on the USB technology, specifically on the new USB 2.0 specifications. Thediscussion begins with an introduction to USB technology, the physical topology, and how it operates.Following, a detailed discussion on the USB 2.0 technology will be presented covering the component parts, layered architecture, data flow types, and packetization specifics. In addition a brief discussion on an emerging compliment to USB 2.0, the USB On-the-go, will be presented.Finally a comparison between USB 2.0 and IEEE 1394 (Fire Wire) will be presented.

Part 1: Overview of USB Technology

Universal Serial Bus (USB) was originally created and released as a standard in 1995 with USB 1.0. It was jointly developed by Compaq, Hewlett-Packard, Intel, Lucent, Microsoft, NEC, and Phillips, which make up the USB Implementers Forum (Ziller, 2002). This same group has just released specifications for USB 2.0. The overall motivation for the development of USB stemmed from three main sources:

- Connection of the PC with the telephone: The convergence of the telephony and data networks has spawned a race to develop technologies that can work to interconnect the two with ease.

- Port expansion: The development of a port that supported multiple devices would lessen the confusion when working with external I/O devices.

- Ease-of-use: If all of the computer's I/O devices could connect to a single port, the fear of setting up a computer would virtually disappear (USB, 2000).

With these three fundamental motivations, USB technology was developed and has become an industry standard for the interconnection of peripheral I/O devices. This section takes an elementary look at the physical characteristics, physical and logical topology, and how it all works. 1.1 Physical Characteristics and Throughput Capabilities Universal Serial Bus technology is exactly as it sounds. It is a bus, which is a mechanism for transferring data and instructions from one point to another, that transmits data bit by bit or in a serial fashion and is able to communicate universally to many different devices. The USB is simply another way of transferring information between external I/O devices and the internal processor of the computer.

Information can be transferred in many different ways between devices connected to a computer. Table 1.1 summarizes some of the different types and rates of transfer for different standards and busses available. As the table shows, the transfer rates vary widely from .115 MB/s with a standard parallel port, up to 400 MB/s with a Fiber channel.

I. Background

Sealevel Systems utilizes a unique architecture for adapters used to convert signals from USB ports to serial devices. It is important that the marketplace have empirical data comparing the relative performance of a dedicated USB UART design like the “Sealevel architecture” versus the “industry average architecture” of a shared throughput design.

II. Test Objective

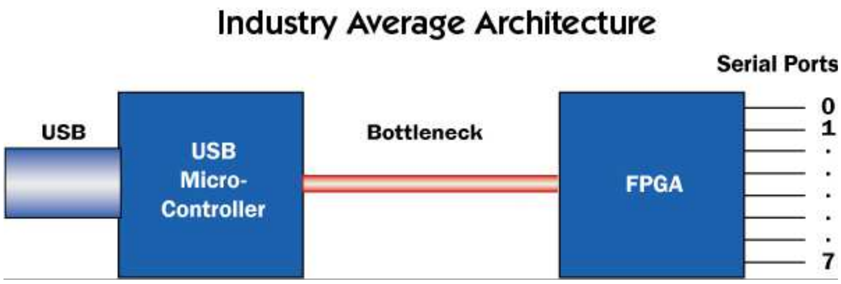
Determine the impact of architecture on the performance of USB to Serial Adapters in order to assist users in selecting products most appropriate for their applications.

III. Findings

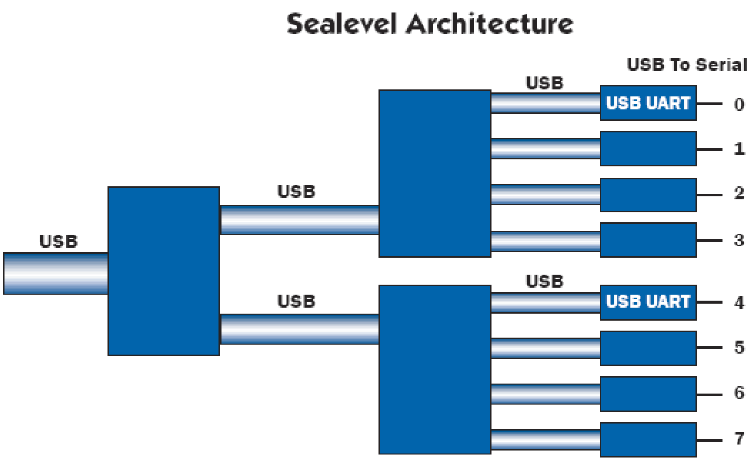
There is a significant difference in performance between the “Sealevel architecture” and “industry average architecture” for USB serial adapters. Performance testing of 8-port USB serial adapters proved that the architecture determines the maximum baud rate and more importantly, the throughput of connected serial devices.

The “Sealevel architecture” uses a USB UART interface that delivers significantly faster and more reliable communications.

The “industry average architecture” 8-port USB serial adapter utilizes a USB microcontroller and a single FPGA wired to all eight serial ports. The interface between the microcontroller and FPGA creates a bottleneck because the serial devices are sharing the throughput of the microcontroller. As a result, each additional serial device added substantially reduces the speed of all eight serial ports.



In contrast, the “Sealevel architecture” 8-port serial adapter (Item# 2801) couples each port with a dedicated USB UART chip. This is equivalent to connecting eight single-port USB serial adapters to the host, thereby allowing each serial port to run at maximum speed. (All Sealevel SeaLINK USB serial adapters have this architecture advantage.) The bottleneck found in the industry standard architecture is the limiting factor and the speed of the USB connection (e.g., USB 1.1 vs. USB 2.0) does not affect throughput.



IV. Test Procedures

Tests on the USB serial adapters utilized a desktop computer with a 3GHz Intel Pentium4 CPU, 2GB of RAM, and a fresh install of Windows XP.

The USB serial adapters were installed per manufacturer instructions and RS-232 loopback plugs were placed on all eight serial ports.

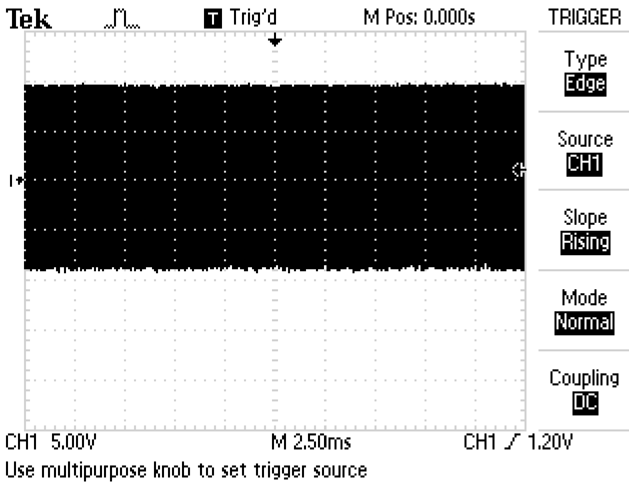
The test was conducted using WinSSD, a serial communications utility. WinSSD provides terminal mode operation and enables modifying default UART settings. WinSSD allows toggling modem control signals, transmitting test patterns, initiating loopback tests, and performing bit error rate testing (BERT) and throughput monitoring.

Each serial port was set at the maximum baud rate, then multiple instances of WinSSD were launched with each serial port opened in order and the bit error rate test (BERT) initiated. The transmit (Td) and receive (Rd) data rates (throughput) were added together for all open ports and compared.

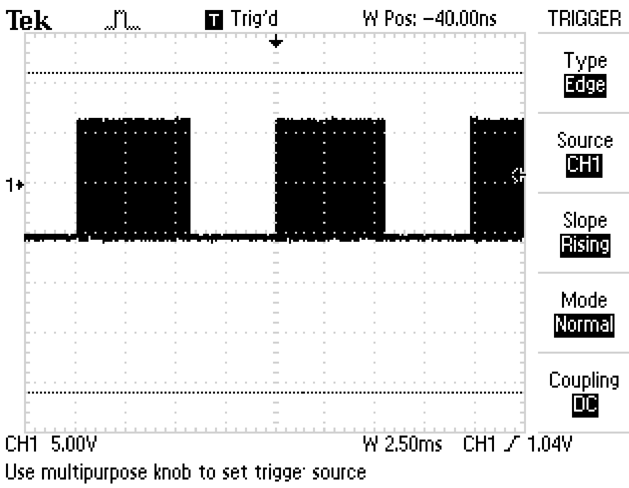
V. Detailed Findings

A. Throughput with One Port Opened

With one port on the "Sealevel architecture" adapter open at the standard baud rate of 115.2K bps, the oscilloscope confirmed that the throughput matched the baud rate with a continuous stream of data



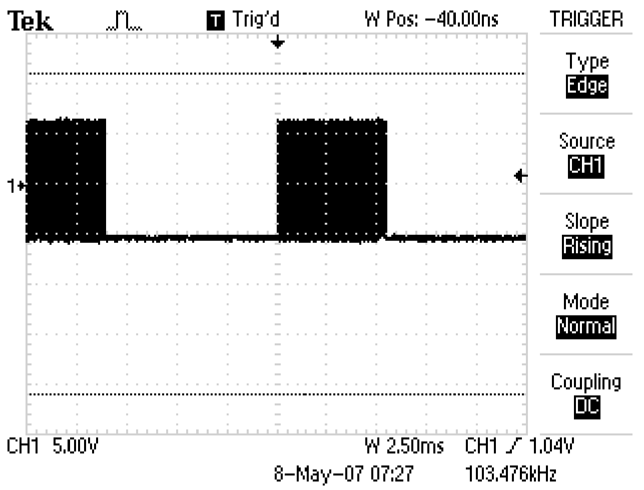
With one port on the "industry average architecture" adapter open at the standard baud rate of 115.2K bps, data was transmitted in bursts rather than in a continuous stream and the actual data rate was only approximately 65K bps.



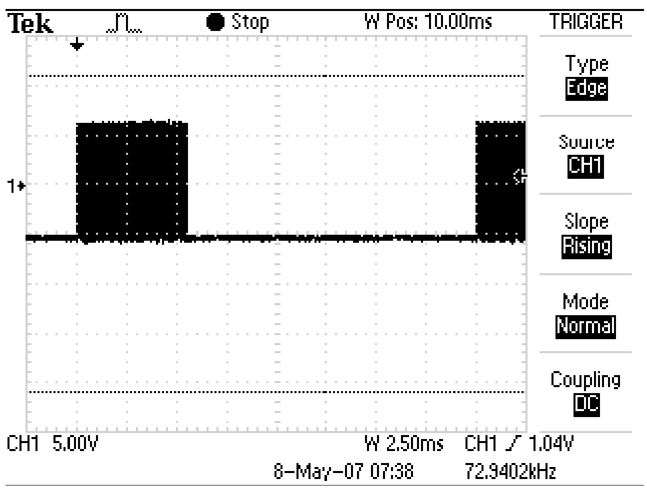
B. Throughput with Multiple Ports Opened

Data rates for the “Sealevel architecture” USB serial adapter remained continuous at the specified baud rate as multiple ports were sequentially opened.

When the second port on the “industry average architecture” adapter was opened at 115.2K bps, the data rate on the first serial port dropped to approximately 48K bps.



When the third port on the “industry standard architecture” adapter was opened at 115.2K bps, the data rate on the first serial port dropped to only 33K bps.

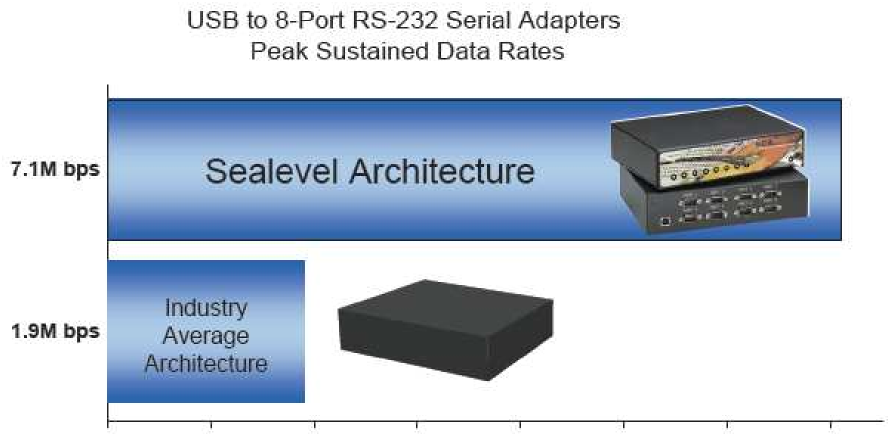


When attempting to open all eight serial ports on the “industry standard architecture” adapter, the Loopback Pattern Test in WinSSD showed that the data was corrupted. Additionally, a lock-up occurred on multiple serial ports necessitating that they be closed and re-opened in order to regain functionality.

C. Total Throughput

At the maximum baud rate specified for the product, the bi-directional data rate for the “Sealevel architecture” USB serial adapter was a peak 7.1M bps across all eight serial ports running concurrently.

The bi-directional data rate for the “industry average architecture” USB serial adapter at the maximum baud rate was a peak 1.9M bps across only four ports running simultaneously. Opening additional serial ports beyond four resulted in the ports locking up. Only four serial ports would operate concurrently at the specified maximum baud rate.



VI. Conclusion

"Sealevel Architecture" Provides Faster, More Reliable Data Transmission.

Testing revealed that two key design and component advantages contribute to this superior performance.

1. "Sealevel architecture" allows each port to run at maximum speed

The "Sealevel architecture" couples each port with a dedicated USB UART chip. This is a superior design because it is equivalent to connecting eight single-port USB serial adapters to the host, thereby allowing each serial port to run at maximum speed. (All Sealevel SeaLINK USB serial adapters have this architecture advantage.)

2. "Sealevel Architecture" Produces Continuous Transmission Stream

When the first port on the "Sealevel architecture" USB serial adapter was opened, the oscilloscope confirms that the throughput matches the baud rate with a continuous stream of data. Even as additional ports were opened, the first serial port delivered a continuous stream of data.