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TSV Stress-Aware ATPG for 3D Stacked ICs*

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***Abstract*—Thermo-mechanical stress due to TSV fabrication processes is a major concern in 3D integration. TSV stress not only degrades the mechanical reliability of 3D ICs but it also affects the electrical properties, such as electron and hole mobility, of the MOS devices surrounding TSVs. Variations in carrier mobility result in a change in the timing profile of the circuit, which has an impact on delay-fault testing. We show quantitatively using the SDQL metric that test quality is significantly reduced if the test patterns are generated with TSV stress-oblivious circuit models. We evaluate the impact on TSV stress on delay testing by considering layouts for several 3D logic-on-logic benchmarks. The test escape rate is higher for processes with lower yields. Our results also indicate that we can improve the test quality by using TSV-stress aware cell libraries in a conventional ATPG flow with commercial tools, with negligible impact on pattern count. We therefore conclude that any detrimental impact of TSV stress on pattern effectiveness and test quality can be overcome by using stress-aware models for test generation.**

I. Introduction

Three-dimensional (3D) stacking with through-silicon-vias (TSVs) is a promising technology that can sustain Moore's Law by providing high-bandwidth and high-speed interconnects between chips [1], [2]. TSVs are short metal pillars that go through the silicon substrate and connect the front side of one die with the back side of another die. Due to their small dimensions, TSVs offer a number of benefits over conventional stacking methods, such as higher interconnect density, higher performance, and lower power consumption. Figure 1 shows a generic 3D stack and Figure 2 shows a detailed layout of a circuit with TSVs.

Despite the numerous benefits offered by 3D integration, test challenges for 3D ICs must be addressed before volume manufacturing and defect screening can be feasible [3], [4]. One of the serious problems confronting 3D integration is that of thermo-mechanical stress due to TSV processing. The thermal expansion coefficient of copper, a common TSV fill material, is significantly higher than that of silicon: $17 \times 10^{-6}/K$ versus $3 \times 10^{-6}/K$ [5]. Due to this mismatch, TSVs are likely to cause residual stress in the silicon during fabrication and thermal cycling. One of the effects of thermal stress is mobility variation in MOS devices in the proximity of TSVs. These variations lead to a change in the timing profile of the circuit [6], [7], which affects delay-fault testing.

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Recent work on 3D IC testing has targeted solutions to overcome problems related to test access in 3D ICs and TSV testing. We focus here on post-bond delay-fault testing of internal die logic in 3D ICs, a problem that has received much less attention in the literature. We study the impact of timing variations due to TSV stress on the quality of test patterns generated to screen small-delay defects (SDDs). In particular, we focus on the following problems: (i) How severe is the impact of TSV-induced stress on the effectiveness of patterns for SDDs and test escapes? (ii) To what extent can test escapes be reduced by including analytical TSV stress models as a preprocessing step in the ATPG flow? (iii) What is the impact of TSV stress-aware ATPG on pattern count and how does the process yield affect test escapes due to TSV-induced stress?

We assume that SDD testing is done after stacking, such that the clock tree for functional operation is available for at-speed capture cycles. We show that the use of TSV stress-oblivious circuit models results in a significantly increased escape rate of faulty chips. The level of this increase depends on the yield of the fabrication process; we conclude that accurate modeling of TSV stress is more important for processes with lower yields.

The impact of TSV stress on pattern effectiveness is quantified using the statistical delay quality level (SDQL) metric [8]. This is a key metric in our approach, since the SDQL of a chip correlates with the expected test escape rate due to small-delay defects. We also show that the test escape can be reduced considerably by incorporating TSV stress in cell timing libraries and using these libraries with a commercial timing-aware ATPG tool. Therefore, any detrimental impact of TSV stress on pattern effectiveness and test quality can be overcome by using stress-aware models for test generation. We also show that TSV stress-aware testing leads to negligible increase, if any, in pattern count.

The remainder of this paper is organized as follows. In Section II, we give an overview of related prior work, including 3D SIC testing, small-delay testing, and mobility variations due to TSV stress. Section III describes our methodology to create TSV stress-aware test patterns using conventional ATPG tools. In Section IV, we present experimental results obtained with 3D logic-on-logic benchmarks. Finally, Section V concludes the paper.

II. Related Prior Work

A. 3D IC Testing

3D ICs introduce new challenges for test engineers such as test access during the entire 3D test flow, which may include the

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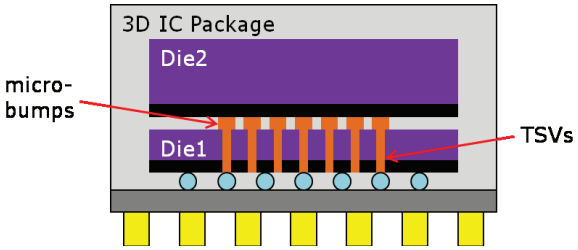

Fig. 1. 3D stacked IC consisting of two dies.

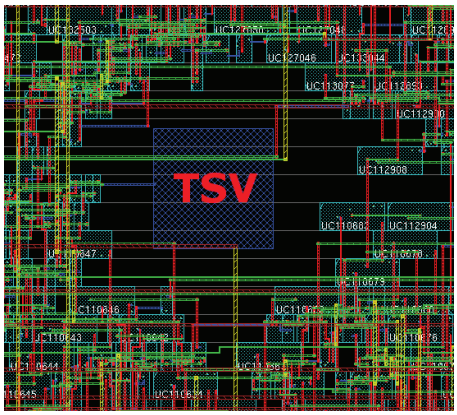

Fig. 2. 3D IC layout: circuitry around TSV.

following test insertions [9]:

- *Pre-bond test* is carried out to obtain known good die before stacking;
- *Post-bond test* is carried out during and after stacking;
- *Final test* targets the entire stack and package to ensure outgoing product quality.

Test access for all of these insertions requires an extension of the conventional (2D) DfT architecture. This issue has been addressed in [9]–[12], where a 3D architecture based on die-level wrappers has been proposed. This architecture is currently being considered for standardization by the IEEE P1838 Working Group [13].

TSV test poses new challenges for test engineers. In particular, pre-bond TSV testing is difficult, since with current probe technology, we cannot probe individual TSVs due to their small dimensions. Recently, some new built-in self-test (BIST) methods have been proposed to detect faulty TSVs before die bonding without mechanical contact [14], [15]. Another possible solution is to probe multiple TSVs at a time [16], a proposal that leverages recent advances in probe technology [17]. While the above methods all target important aspects of 3D IC testing, they do not consider the impact of TSV-induced stress on pattern effectiveness for delay testing. This paper fills this void by integrating TSV stress modeling with ATPG for delay testing.

B. SDD Testing and SDQL

Due to continuous miniaturization, integrated circuits have become more susceptible to process variations and resistive defects. As a result, SDDs have become more prevalent [18]. Despite the fact that their size might be small compared to the clock period, SDDs can cause errors if the length of a path affected by them exceeds the clock period. Therefore, effective and low-cost screening for SDDs is important to ensure product quality.

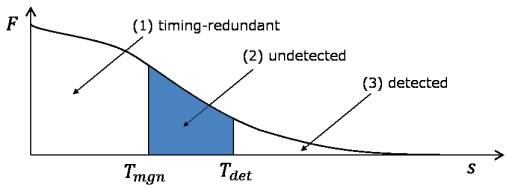

Fig. 3. Delay distribution $F(s)$.

Several methods have been proposed in the literature to test for SDDs [18]–[20].

To quantify the effect of TSV stress on the quality of a delay-fault test, we use the statistical delay quality level (SDQL) proposed in [8]. With this metric, we can quantitatively estimate the test escape rate due to delay defects and evaluate the increase in test quality if TSV stress-aware circuit models are used for ATPG.

SDQL computation is based on the assumption that delay defects follow a probability distribution $F(s)$, where s is the size of the defect, and that the defects are equally distributed over all sites. This distribution is dependent on the manufacturing process and can be obtained by analyzing manufacturing data [21].

Figure 3 shows an example of a delay-defect distribution function. For each delay fault, this function is divided intro three regions by T_{mgn} and T_{det}, which are defined as follows. The time margin T_{mgn} for a fault is the slack on the longest of the paths that can propagate this fault:

$$T_{mgn} = T_{ck,f} - \max_i(T_i), \tag{1}$$

where $T_{ck,f}$ is the functional clock period and T_i are lengths of the sensitizable paths. A fault can only be detected if its size T_{det} exceeds the slack of the path sensitized by a particular test:

$$T_{det} = T_{ck,t} - T_{sens}, \tag{2}$$

where $T_{ck,t}$ is the test clock period and T_{sens} is the length of the sensitized path. As Figure 3 shows, delay faults can be put into three categories dependent on their size s: (1) timing-redundant, (2) undetected, and (3) detected. The area below the curve in the undetected region represents the probability of the fault being undetected and escaping the test. The summation of these probabilities for all faults is called SDQL [8]:

$$SDQL = \sum_{k}^{2N} \int_{T_{mgn}}^{T_{det}} F(s)\,\mathrm{d}s, \tag{3}$$

In this work, we use the SDQL metric to show that the use of TSV stress-oblivious circuit models may lead to a significantly increased escape rate for 3D ICs.

C. Mobility Variation due to TSV Stress

Due to a mismatch in thermal expansion coefficients of copper and silicon, TSVs cause thermo-mechanical stress in the surrounding silicon. This stress affects not only the mechanical device reliability but also material properties such as carrier mobility [22], which results in timing variations of the devices. Recent studies have reported up to $\pm 10\%$ variations for individual cells [6].

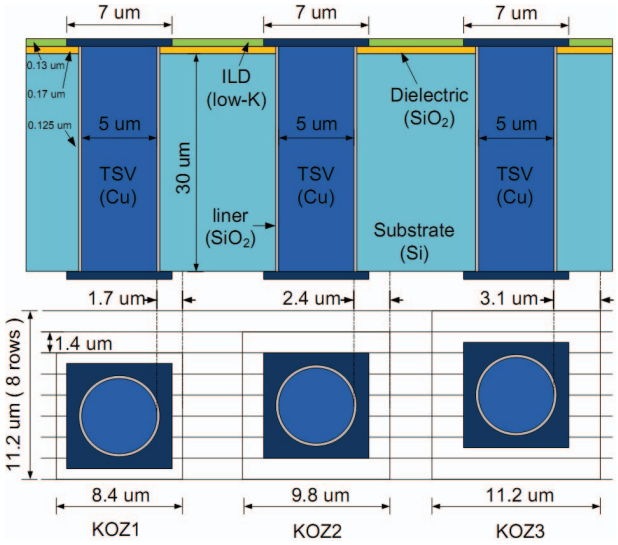

Fig. 4. The TSV structure and three different KOZ sizes used in our studies.

Since a correct timing model of the circuit is crucial for delay testing, we need an efficient methodology to take TSV stress into consideration in the ATPG flow.

In the literature, we can find a simple closed form formula for the thermo-mechanical stress caused by a TSV, known as the Lamé stress solution [6]. However, this model is 2D in its nature, capturing only the information in the x and y directions on the wafer surface, and it fails to capture the true 3D nature of the TSV stress field near the wafer surface. Since there is no simple formula for the 3D stress field available in the literature, we can apply the methodology outlined in [7] for full chip analysis. The main idea of this methodology is to perform a finite-element analysis (FEA) for a single TSV and use linear superposition to estimate the total stress σ_{rr} due to multiple TSVs.

The resulting σ_{rr} serves as an input to compute the carrier mobility variation, which can be expressed as a function of σ_{rr} and the device channel orientation θ with respect to the TSV [6]:

$$\frac{\Delta\mu}{\mu}(\theta) = -\Pi \times \sigma_{rr} \times \alpha(\theta), \tag{4}$$

where $\alpha(\theta)$ is the orientation factor as a function of the angle θ between the channel orientation and the center of the TSV, and Π is the piezo-resistive coefficient at $\theta = 0$. Π can be extracted using the methodology described in [23].

The estimated carrier mobility change can be used to update the timing information of the devices around TSVs for a more accurate circuit model.

III. Methodology

Our approach consists of two major parts:

1) Generation of a TSV stress-aware circuit model;
2) Test pattern generation and simulation.

The rest of this section describes the two steps in detail.

A. TSV Stress-Aware Model Generation

The TSV structure considered in our simulations is shown in Figure 4. The TSV diameter, height, landing pad size, and liner

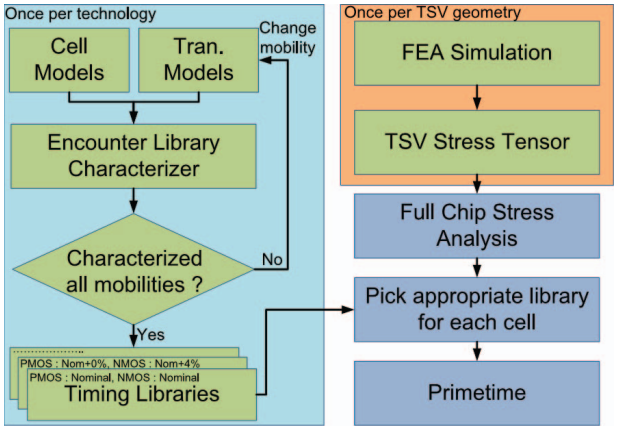

Fig. 5. The design flow used to obtain TSV-stress-aware timing

thickness are assumed to be 5 μm, 30 μm, 7 μm, and 125 nm, respectively. The TSV is assumed to be made of copper, and the liner of SiO_2. The material properties used in our experiments are: CTE (ppm/K) for Cu = 17, Si = 2.3, SiO_2 = 0.5; Youngs modulus (GPa) for Cu = 110, Si = 130, SiO_2 = 71. We also consider three different keep-out-zone (KOZ) sizes of 1.7 μm, 2.4 μm and 3.1 μm as shown. This corresponds to 6, 7 and 8 standard cell rows in the Nangate 45 nm technology library. A larger KOZ will mean less impact of TSV stress on the gates. However, increasing the KOZ will affect other design metrics such as area and wirelength.

The overall design flow used to obtain stress aware timing is shown in Figure 5. We first start with creating a timing library with different mobility values. We start with the nominal PMOS and NMOS mobility, and characterize all the cells in increments of 4%. The next step is stress calculation, and this is performed as outlined in [7]. We first perform FEA simulation of the stress generated by a single TSV using the FEA software ABAQUS [24]. At any given point in the chip, the stress can be represented by its nine-component stress-tensor as follows:

$$\sigma = \sigma_{ij} = \begin{bmatrix} \sigma_{11} & \sigma_{12} & \sigma_{13} \\ \sigma_{21} & \sigma_{22} & \sigma_{23} \\ \sigma_{31} & \sigma_{32} & \sigma_{33} \end{bmatrix}$$

The first index i indicates that the stress acts on a plane normal to the i axis, and the second index j denotes the direction in which the stress acts. In cylindrical coordinates, the three indices $1, 2$, and 3 represent r, θ, and z respectively. Since the stress of a single TSV is radially symmetric, we only need to store the stress tensors along one arbitrary radial line. The steps outlined so far only need to be performed once and the results can be used for any design.

For any given design, we need to perform full-chip stress analysis. For computation of stress due to multiple TSVs, we use linear superposition. The stress at each point in the chip is simply the vector sum of the stress caused by all TSVs at that point. A vector sum of the stress components is performed by transforming the cylindrical stress tensor into its Cartesian form, adding the components individually along the x, y and z axis, and then transforming it back to cylindrical coordinates.

With the stress tensor at each point in the design, the corresponding change in mobility of electrons (NMOS) and holes

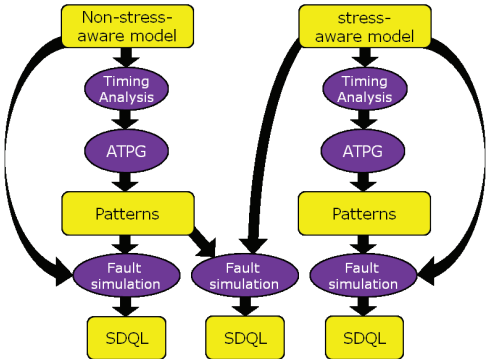

Fig. 6. ATPG tool flow.

(PMOS) can be computed using the measured piezoresistive coefficients given in [23], assuming (100) silicon. With this approach, we obtain the change in mobility due to TSV stress for each cell in the design.

The appropriate timing library can then be picked from the pre-characterized set of timing libraries. All the libraries, netlists, and parasitics are fed into Synopsys Primetime to get TSV-stress-aware timing results.

B. TSV-Stress-Aware ATPG

Delay-fault ATPG relies on correct circuit timing information, which is used to generate the path profile in order to target the longest sensitizable paths for each fault. In 3D ICs, timing variations in devices due to TSV stress might occur, resulting in a change of the timing profile of the circuit. The slacks for paths that include the the affected devices can increase or decrease dependent on the device type (PMOS or NMOS) and on the location relative to the TSVs, changing the longest sensitizable path for certain delay faults. If these changes are not taken into account, the ATPG tool might propagate faults through paths that are shorter than the actual longest path. This will invariably result in a lower test quality, since delays of a particular size will not be detected.

To evaluate the impact of the TSV-induced stress on the test quality, we have developed a tool flow using conventional timing analysis and ATPG tools: Synopsys PrimeTime and TetraMax, respectively. Figure 6 gives an overview of the flow. As input, we use the original (non-stress-aware, NSA) models and the modified (stress-aware, SA) models. First, we perform timing analysis with PrimeTime to extract the slack data. Next, we generate two delay test pattern sets with TetraMax: one using the NSA and the other using SA models. Finally, we perform fault simulation and compute SDQL with TetraMax using the following combinations.

1) The NSA pattern set on the NSA model. The results of this simulation show the test quality that is expected if TSV stress is not present.
2) The NSA pattern set on the SA model. The simulated SDQL numbers indicate the actual test quality of the NSA pattern set.
3) The SA pattern set on the SA model. The simulated SDQL numbers indicate the actual test quality of the SA pattern set, i.e., under realistic conditions of TSV stress.

TABLE I
DESIGN STATISTICS FOR THE BENCHMARKS USED IN THIS PAPER

Benchmark	# Gates	# Scan FFs	3D Impl.	# TSVs
des_perf	26,251	1,984	2-die	419
			3-die	884
			4-die	1322
cf_rca_16	156,624	20,480	2-die	589
			3-die	676
			4-die	953
cf_fft_256_8	299,273	75,723	2-die	2193
			3-die	4717
			4-die	5843

IV. CASE STUDY

A. Test Vehicles

In this paper, we use three benchmarks taken from the open cores benchmark suite [25]. They are synthesized and scan-inserted using the Nangate open cell library, at the 45 nm node. Table I gives an overview of the design data, including gate, scan flip-flop and TSV count. We partition the netlist and create three different stacks for each core: two-die, three-die, and four-die stacks. For each die, we use a 3D force-directed placer to place the gates [26]. This placer places TSVs in a regular fashion, and assigns nets to TSVs using a 3D Minimum Spanning Tree approach.

Once we have the placement result, we route each die separately in Cadence Encounter. Assuming the TSV resistance and capacitance to be 50 fF and 50 mΩ, respectively [27], [28], we carry out timing analysis in Synopsys Primetime. We treat dies as modules, and TSVs as top level interconnections. Primetime is also used to get die-level timing constraints, and these are used to perform timing optimization in Cadence Encounter. We also obtain stress aware timing from the methodology outlined in Section III-A. Some sample layouts of des_perf are shown in Figure 7, along with the obtained PMOS mobility maps.

FEA simulation and library characterization took a relatively long time: eight hours and 180 hours, respectively. However, these steps need to be done just once per technology and the results can be re-used for all designs mapped to this technology. The actual mobility computation only took several minutes per layout.

B. ATPG Results

We applied the flow depicted in Figure 6 to different benchmarks. In this experiment, we used the distribution function that the authors of [8] obtained by analysing experimental data presented in [21]. We assume that delay defects greater than 10 ns are screened out by stuck-at tests, therefore the probability of delay defects with $s > 10$ ns is zero. The function was normalized such that the area under the curve is unity:

$$\int_0^\infty F(s)\,\mathrm{d}s = 1$$

The resulting probability distribution function is:

$$F(s) = \begin{cases} 1.97e^{-2.1s} + 0.005 & \text{if } 0 \le s \le 10 \\ 0 & \text{else} \end{cases}$$

Table II shows the test escape rate of the chips expressed in defective parts per million (DPPM). The DPPM is calculated as

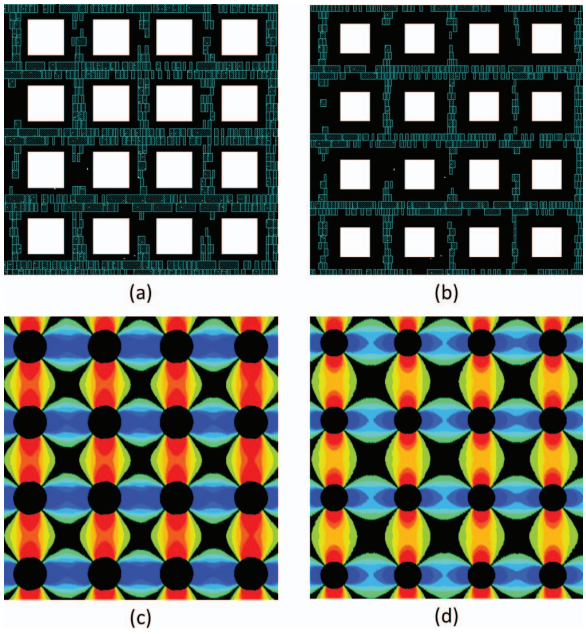

Fig. 7. (a,b) Layout screenshots for KOZ1 and KOZ3 of benchmark des_perf. White rectangles indicate TSVs, and blue indicates standard cells. (c,d) The corresponding PMOS mobility maps. Black indicates TSVs. Green, red and blue represent nominal, positive, and negative mobility change respectively.

SDQL normalized by the number of delay-faults N:

$$DPPM = \frac{1}{N} SDQL$$

The results indicate that the actual escape rate of the NSA patterns (Row 2) is significantly higher than the estimated one (Row 1). This implies that neglecting TSV-stress in the ATPG flow by using a NSA model leads to decreased test quality.

The results presented in Table II also show that the test escape rate of the optimized patterns (Row 3) almost equals the one initially targeted (Row 1). Therefore, if TSV stress is taken into account during ATPG, it has no significant impact on the test quality. This is also true for small keep-out zones: regardless of the KOZ size, the test quality can reach the level of a circuit without the timing variation effects caused by TSV stress.

Table III shows the number of test patterns generated for different combinations. We observe that there is no significant variation in pattern count between the NSA and SA patterns for the same implementation. This implies that a stress-aware ATPG flow has negligible impact on pattern count compared to a conventional ATPG flow. In addition, we observe that the size of the KOZ has no impact on pattern count.

In addition to the experiment described above, we applied the flow to the benchmarks using the simplified distribution function $F(s) = \lambda e^{-\lambda s}$ with different values of λ. Small values of λ correspond to a flatter function $F(s)$, which implies that larger delays are more likely to occur. Therefore, smaller λ should lead to higher test-quality degradation of non-optimal (non-stress-aware) patterns, which can be expressed as the DPPM ratio r between the DPPM values of the NSA and SA test patterns:

$$r = \frac{P_{escape}(\text{NSA})}{P_{escape}(\text{SA})} = \frac{SDQL(\text{NSA})}{SDQL(\text{SA})} \quad (5)$$

TABLE II
DEFECTIVE PARTS PER MILLION FOR VARIOUS DESIGNS.

Design		Patterns - Model	KOZ1	KOZ2	KOZ3
des_perf	2-die	NSA patterns - NSA model	24.8	25.0	27.2
		NSA patterns - SA model	177.1	180.0	190.7
		SA patterns - SA model	23.9	23.7	28.1
	3-die	NSA patterns - NSA model	35.8	38.1	43.9
		NSA patterns - SA model	101.1	110.3	120.7
		SA patterns - SA model	34.1	38.7	42.8
	4-die	NSA patterns - NSA model	41.5	46.1	47.7
		NSA patterns - SA model	183.1	203.1	219.3
		SA patterns - SA model	40.8	44.6	47.7
cf_rca_16	2-die	NSA patterns - NSA model	4.05	4.26	4.38
		NSA patterns - SA model	5.70	6.00	6.16
		SA patterns - SA model	4.17	4.41	4.52
	3-die	NSA patterns - NSA model	5.00	5.19	5.20
		NSA patterns - SA model	7.81	8.00	8.01
		SA patterns - SA model	4.83	4.90	4.81
	4-die	NSA patterns - NSA model	4.70	5.20	4.27
		NSA patterns - SA model	7.55	8.22	6.87
		SA patterns - SA model	4.63	5.31	3.95
cf_fft_256_8	2-die	NSA patterns - NSA model	608.82	578.80	590.85
		NSA patterns - SA model	935.97	921.75	934.07
		SA patterns - SA model	617.55	578.41	591.05
	3-die	NSA patterns - NSA model	597.53	591.61	608.31
		NSA patterns - SA model	907.90	901.32	941.54
		SA patterns - SA model	604.73	592.37	609.87
	4-die	NSA patterns - NSA model	741.06	761.206	733.96
		NSA patterns - SA model	1072.54	1126.64	1099.41
		SA patterns - SA model	761.27	775.97	739.12

TABLE III
PATTERN COUNT FOR VARIOUS DESIGNS.

Design		Patterns	KOZ1	KOZ2	KOZ3
des_perf	2-die	NSA patterns	5761	5672	5722
		SA patterns	5632	5666	5789
	3-die	NSA patterns	4382	4400	4468
		SA patterns	4373	4356	4417
	4-die	NSA patterns	3114	3166	3199
		SA patterns	3057	3080	3191
cf_rca_16	2-die	NSA patterns	9884	9697	9631
		SA patterns	10070	10007	9955
	3-die	NSA patterns	7770	7873	7818
		SA patterns	7865	7840	7912
	4-die	NSA patterns	5857	5935	6014
		SA patterns	6034	5927	6007
cf_fft_256_8	2-die	NSA patterns	21405	23270	23456
		SA patterns	21354	23326	23533
	3-die	NSA patterns	18495	17697	19927
		SA patterns	17993	17706	20174
	4-die	NSA patterns	20935	21031	21151
		SA patterns	21074	21223	21211

This conclusion is consistent with the simulated values of the DPPM ratio r depicted in Figure 8: r is decreases with λ. This implies that less mature the fabrication process (i.e., lower the yield), the more improvement in test quality that can be achieved using. Larger values of r indicate that higher test escapes (relative to what we get with TSV stress-aware patterns) will result if TSV stress is not considered for test generation. However, r also depends on the design. The TSV density in des_perf is relatively high compared to that in cf_rca_16, therefore the relative number of the devices affected by TSV stress is higher in des_perf. This results in a higher sensitivity of DPPM to accurate timing modeling.

The CPU time for the ATPG flow strongly depends on the design size. For a layout of des_perf, cf_rca_16, and cf_fft_256_8,

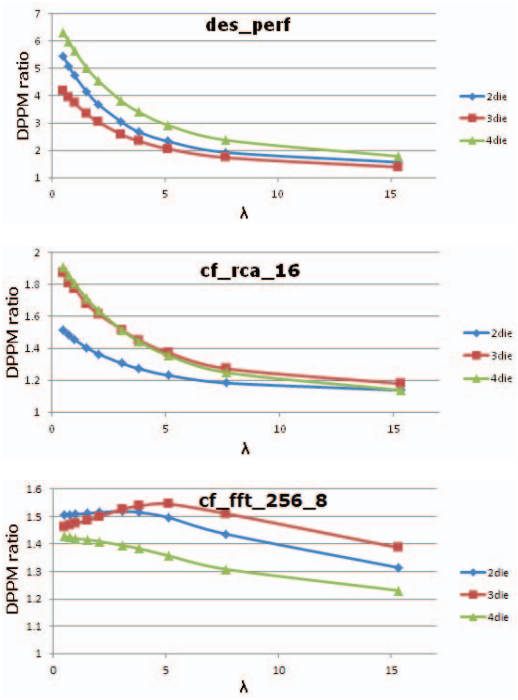

Fig. 8. DPPM ratio as function of λ.

the CPU time was one minute, 30 minutes, and four hours, respectively.

V. Conclusion

In this work, we evaluated the impact of TSV stress on the quality of SDD testing. We used an ATPG flow based on conventional ATPG tools to compare the test escape rate for the following cases: (1) anticipated test escape rate for TSV-stress unaware tests, (2) the actual test escape rate for TSV-stress unaware tests, and (3) the test escape rate for TSV-stress aware tests. Based on our results, we make the following conclusions.

- Neglecting TSV stress results in a significantly higher test escape rate compared to that obtained using a TSV-stress unaware ATPG flow.
- Using a TSV-stress aware ATPG flow will improves test quality and bring the escape rate back to the levels achieved using ATPG on circuits that are not affected by TSV stress. This is true for all KOZ sizes.
- Smaller KOZs are not an issue: even though the circuitry is stronger affected by TSV stress when using small KOZs, the ATPG flow with stress-aware models will still create high-quality tests. There is no noticeable impact on the pattern count.
- The degradation of the test quality if TSV stress is neglected is sensitive to the fabrication process quality. Therefore, the poorer the yield of the process, the more important is an accurate modeling of TSV stress in order to optimize the test quality.

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