Graphene Nanoribbon Tunneling Field-Effect Transistors With a Semiconducting and a Semimetallic Heterojunction Channel

Haixia Da, Kai-Tak Lam, *Student Member, IEEE*, G. Samudra, *Member, IEEE*, Sai-Kong Chin, and Gengchiau Liang, *Member, IEEE*

***Abstract*—We present a computational study of the device performance of graphene nanoribbon tunneling field-effect transistors (TFETs) with a heterogeneous channel. By varying the length and the energy bandgap (E_G) of the heterogeneous region, the ON- and OFF-state currents ($I_{\rm ON}$ and $I_{\rm OFF}$) can be effectively optimized independently. Both semiconducting and semimetallic heterogeneous regions are studied to understand the effects of E_G engineering on device behaviors. In addition, the effect of gate coverage (GC) over the heterogeneous region is also investigated. We found that device performance is greatly affected by the positioning of the gate to modify the region where band-to-band tunneling occurs. For a given $I_{\rm ON}/I_{\rm OFF}$ of eight orders, our results show that, for the semiconducting heterojunction, a higher $I_{\rm ON}$ can be obtained by having the gate partially covering the heterogeneous region. This is due to a combination of a short tunneling length and resonant states, which leads to an increase in carrier concentration for the tunneling mechanism. On the other hand, for the semimetallic case, a similar $I_{\rm ON}/I_{\rm OFF}$ is only attainable when the heterogeneous region is not covered by the gate. A large $I_{\rm OFF}$ is observed for even small GC due to the valence electrons from the source traveling to the conduction bands of the semimetallic region, enhancing the carrier transport toward the drain. Our study highlights the device design consideration required when optimizing the device performance of heterojunction TFETs.**

***Index Terms*—Graphene, heterojunction, tunneling transistors.**

I. Introduction

GRAPHENE is a 2-D zero energy bandgap (E_G) material, whose carriers behave as massless fermions. Their energy dispersion near Fermi level is linear and can be approximated with the Dirac equation [1]. It exhibits many novel properties that are not observed in conventional materials, such as the Klein paradox in a p-n junction and the quantum spin Hall effect [2], [3], which can enable new functional devices. As both the electrons and the holes have similar electronic properties, graphene can be used for n- and p-type field-effect transistors (FETs) with similar performance. These unique characteristics make graphene a potential successor to silicon in nanoelectronic devices as silicon approaches its fundamental limitations with the continuing miniaturization of device sizes [4]. In particular, due to its single-layer structure and compatibility with complementary metal–oxide–semiconductor technology, graphene's application in FETs has been experimentally demonstrated using graphene obtained by micromechanical cleavage of pyrolytic graphite [5]. While the absence of a sizable E_G seriously restricts the potential of a graphene FET in digital applications [6]–[10], a couple of novel functional devices exploiting other novel properties have been proposed. For example, the quantum reflective switch [11] based on the Klein paradox and the Veselago lens in graphene p-n junctions exploiting its electron-optic behaviors [12] have garnered much interest in the device community.

Nevertheless, much research effort has been focused on exploring how to open a usable E_G in graphene, such as by breaking the sublattice symmetry and by chemical functionalization [13], [14]. Among these methods, the reduction in dimensionality in graphene nanostructures, for example, carbon nanotubes (CNTs) and graphene nanoribbons (GNRs), has been found to be an effective way to induce E_G [15], [16]. For GNRs, the value of E_G is dependent on the ribbon width and is highly sensitive to an external stimulus, such as strain and electric field. As a result, GNRs enable a wide spectrum of tunable electronic devices [15]–[19]. From the device community, the current–voltage (I–V) characteristics of various graphene nanostructures have been reported [20]–[22] with promising potentials in FET applications. Although device performance of such fabricated FETs will be adversely affected by edge roughness [23], [24], GNR FETs are still considered as one of the most promising tunneling FETs (TFETs) [25]–[36] due to their low tunneling mass, direct bandgap, and compatibility with planar processing.

A heterogeneous junction (HJ) in a GNR has been introduced as a means to enhance the performance of GNR FETs. One such type of HJ TFET is by combining GNRs of different widths in the channel region, and its ability to improve the ON-state current ($I_{\rm ON}$) and the ON-state/OFF-state current ratio ($I_{\rm ON}/I_{\rm OFF}$) by choosing the appropriate HJ positions relative to the source has been investigated [37]. Another type of HJ TFET is based on a partially unzipped CNT, where a semimetallic CNT is connected to semiconducting GNRs. This results in high-speed devices with low energy dissipation [38],

Manuscript received October 25, 2011; revised December 27, 2011; accepted January 21, 2011. Date of publication March 15, 2012; date of current version April 25, 2012. This work was supported by the Agency for Science, Technology and Research, Singapore, Public Sector Funding (A*STAR PSF) under Grant 0821010023. The review of this paper was arranged by Editor K. Roy.

H. Da, K.-T. Lam, G. Samudra, and G. Liang are with the Department of Electrical and Computer Engineering, National University of Singapore, Singapore 117576 (e-mail: elelg@nus.edu.sg).

S.-K. Chin is with the Institute of High Performance Computing, Agency for Science, Technology and Research (A*STAR), Singapore 138632.

Digital Object Identifier 10.1109/TED.2012.2186577

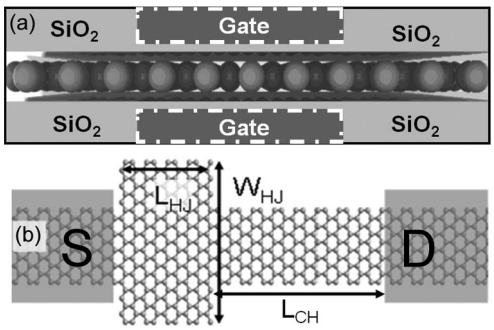

Fig. 1. (a) Side-view schematic of a simulated GNR TFET and (b) atomic model of the HJ TFET. The dark gray zones in (b) represent the source and the drain regions, and $L_{\rm HJ}$ and $W_{\rm HJ}$ are the length and width for the HJ region, respectively, whereas $L_{\rm CH}$ is the channel length. The gate length, $L_G = L_{\rm HJ} + L_{\rm CH}$ when the gate is fully covering the HJ region, i.e., GC $= 1$.

[39]. These investigations demonstrated that an HJ structure is useful in improving the performance of TFETs, owing to the modulated potential profile it creates, which enhances the band-to-band (BTB) tunneling rate across the source–channel interface during the ON-state. Additionally, an HJ structure provides a more abrupt switching point while maintaining a relatively low $I_{\rm OFF}$. However, the detailed device physics of the GNR HJ TFET with different E_G materials at the HJ region, and the difference between semiconducting and semimetallic HJ regions has not been systematically investigated.

Toward this end, we investigate the transfer characteristics of GNR TFETs with heterogeneous semiconducting and semimetallic GNRs with appropriate ribbon widths $(W_{\rm HJ})$. For the semiconducting case, the effect of different HJ lengths $(L_{\rm HJ})$ is also investigated. In addition, the influence of gate coverage (GC) over the HJ region on the device performance of GNR TFETs is explored. We demonstrate that the HJ region forms a quantum-well structure at the source–channel interface, and the resultant quantized state (QS) enhances the BTB tunneling currents. Variation in either $W_{\rm HJ}$ or $L_{\rm HJ}$ changes the energy level of the QS, and hence the I–V characteristics of GNR HJ TFETs. Furthermore, we observe that BTB tunneling occurs at the gate edge, and the placement of the gate edge by adjusting the different GC over the HJ region has a great effect on the I–V characteristics of the GNR HJ TFETs. We clarify the physical mechanism in the HJ TFET structures with semiconducting and semimetallic HJ regions, and our results highlight the design considerations required, in terms of geometrical parameters and gate placement, to optimize the performance of GNR HJ TFETs, and these results can be used as general design guidelines for HJ TFETs.

II. Simulation Approaches

The side-view schematic of the simulated double-gated GNR TFET is shown in Fig. 1(a), where the top and bottom silicon dioxide insulators have a thickness of 1 nm and a relative dielectric constant of 4. The channel is intrinsic for all devices, whereas the source and the drain are p- and n-doped, respectively. The top view of the device configuration is shown in Fig. 1(b), indicating a ribbon width $(W_{\rm HJ})$ of 1.2 nm $(E_G = 1.22$ eV) [15] for the whole device, except for the heterogonous region, which has different widths and lengths ($W_{\rm HJ}$ and $L_{\rm HJ}$), inserted between the source and the channel. In this paper, we have assumed that the channel GNRs are of the $N = 3m + 1$ family, which have large E_G [15]. To minimize the influence of the nominally thick GNR channel length $(L_{\rm CH})$, it is fixed at 14 nm in this study. The gate length (L_G) varies for different cases and spans a range between $L_{\rm CH} < L_G < (L_{\rm HJ} + L_{\rm CH})$ for GC $0 <$ GC < 1. For all cases, one edge of the gate is aligned with the channel–drain interface to minimize any variation on the fringing field effect at the drain contact.

The device physics and performance is investigated based on a mode-space ballistic quantum transport simulator using the nonequilibrium Green's function (NEGF) [40]–[43]. The device Hamiltonian for the GNR is a square matrix built from the Dirac equation [44], with the semimetallic HJ region modeled after a GNR with a very small energy gap, $E_G = 0$ eV $(W_{\rm HJ} = 200$ nm). In practice, the semimetallic HJ region can be constructed with the $N = 3m + 2$ GNRs, which have very small E_G. For example, a GNR with a $W_{\rm HJ}$ of 3.9 nm has a E_G of 0.06 eV. The matrix elements are defined as

$$h_{m,n}(l, k_y) = \begin{cases} U(l), & \text{if } m = n \\ i\hbar\nu_F \left[-\frac{\partial}{\partial x} + (-1)^m \times k_y\right], & \text{if } m \neq n \end{cases} \quad (1)$$

where m and n correspond to the matrix element position in the 2×2 matrix; x and y are the directions along and perpendicular to the channel, respectively; $U(l)$ is the self-consistent potential at a particular discretized point l along x; ν_F is the Fermi velocity of carriers in graphene set at 10^6 m/s; and k_y is a mode-space fitting parameter controlling the electronic band structure according to the width of the GNR. We note that, in the current mode-space model, the intermodal coupling, which is crucial in understanding the scattering processes, is absent in this ballistic-transport-based investigation.

The charge density within the device is calculated from the NEGF module, which is subsequently substituted in the 2-D Poisson equation solved using the finite-difference approach [45] in the plane containing the gate stack and transport directions. As the source and drain metal contacts are considered to be very far away, the boundaries of the device are set to the Neumann boundary condition, cf. solid lines in Fig. 1(a), except for the gate regions, where the Dirichlet boundary condition is used, cf. white dash-dot line in Fig. 1(a), and is fixed to the applied gate potential. The GNR region is modeled to be 3-Å thick with a dielectric constant of 2.5, which is similar to that of single-layer graphene [46], [47]. The potential profile is then fed back to the NEGF solver to recalculate the charge density, and the process is repeated until the difference in potential between iterations is less than 1% of the thermal energy, i.e., 0.26 meV at a room temperature of 300 K. Finally, the local density of states (LDOS), current density, and total currents are calculated for different gate biases under ballistic condition [41]. The origin of the x-axis is set at the beginning of the heterogeneous region near the source.

III. Results and Discussions

A. Effect of the Dimensions of the HJ Region

First, we focus on the transport properties of GNR HJ TFETs with different $L_{\rm HJ}$ and $W_{\rm HJ}$ at the HJ region. The HJ region

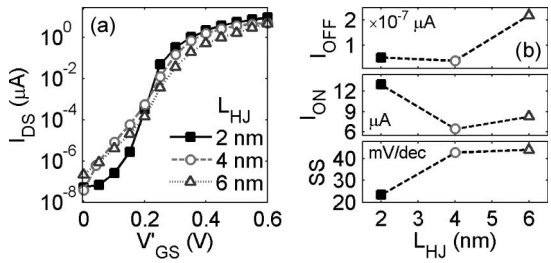

Fig. 2. (a) Transfer characteristics of GNR HJ TFETs with different HJ lengths, $L_{\rm HJ} = 2, 4,$ and 6 nm, respectively, where $V'_{GS} = V_{GS} - V_{DS}/2$ [19]. The applied drain bias (V_{DS}) is 0.6 V. (b) Extracted OFF-state current ($I_{\rm OFF}$), ON-state current ($I_{\rm ON}$), and SS versus $L_{\rm HJ}$. The dash lines are line guides.

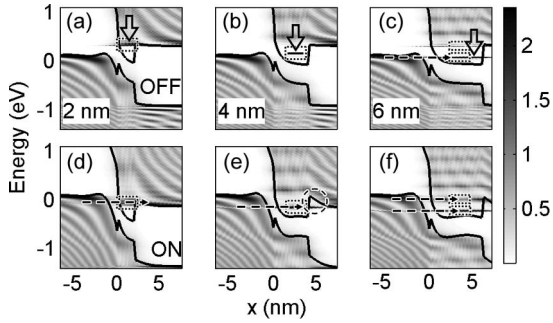

Fig. 3. (a)–(c) LDOS of the HJ TFETs for different $L_{\rm HJ} = 2, 4,$ and 6 nm at the OFF-state ($V'_{GS} = 0$ V), with quantum states highlighted within the dotted boxes in the well structure. (d)–(f) LDOS of the corresponding devices at the ON-state ($V'_{GS} = 0.6$ V), and the dash arrows indicate where BTB tunneling occurs. The colorbar indicates the LDOS values with a unit of [$\times 10^{23}$ cm^{-2} · eV^{-1}] and is applied to all plots.

is assumed to be fully covered by the gate, i.e., GC = 1. The effect of varying $L_{\rm HJ}$ on the I–V characteristics is investigated, and the results are summarized in Fig. 2(a). $W_{\rm HJ}$ is fixed at 2.5 nm, which results in a GNR with $E_{G-{\rm HJ}} = 0.40$ eV. It is observed that, as $L_{\rm HJ}$ increases from 2 to 6 nm, the device performances are degraded. $I_{\rm OFF}$, $I_{\rm ON}$, and subthreshold slope (SS) as a function of $L_{\rm HJ}$ are presented in Fig. 2(b), with the SS taken at the same gate voltage $V'_{GS} = V_{GS} - V_{DS}/2 = 0.2$ V for different $L_{\rm HJ}$, where $V_{DS}/2$ is the minimum current point of ambipolar current characteristics for the homogenous GNR TFETs [35].

In order to understand the transport mechanism at different $L_{\rm HJ}$ in detail, we calculated the LDOS at the OFF-state ($V'_{GS} =$ 0 V) and at the ON-state ($V'_{GS} = 0.6$ V), as shown in Fig. 3. In a conventional TFET, the dominant mechanism contributing to $I_{\rm OFF}$ is BTB tunneling, where the electrons in the valence band at the source tunnel across the energy bandgap of the channel to the continuum of empty states above the conduction band at the drain. For the case of an HJ TFET, due to the presence of the quantum well formed in the HJ region, the carrier transport becomes a two-step process. The electrons from the source initially tunnel into the QS in the quantum well, cf. Fig. 3(c), followed by tunneling across the remaining channel region toward the drain. Therefore, the $I_{\rm OFF}$ trend of HJ TFETs is influenced by the energy level of the QS formed in the HJ region. From the LDOS plots in Fig. 3(a)–(c), it is observed that the energy level of the first QS in the HJ region is lowered as $L_{\rm HJ}$ increases. For $L_{\rm HJ} = 6$ nm, the QS is lowered to the same energy level as the state in the source region, and the carriers are able to tunnel into the HJ region with a much larger probability. These carriers experience a shorter effective tunneling length toward the drain, resulting in $I_{\rm OFF}$ that is two orders larger. For the other two $L_{\rm HJ}$, there is no initial tunneling of carriers from the source to the HJ region, and the slight decrease in $I_{\rm OFF}$ for $L_{\rm HJ} = 4$ nm is a result of the increase in the total tunneling length.

In conventional TFETs at the ON-state, the main current contribution comes from BTB tunneling across the source–channel interface, and then, the carriers flow from the channel to the drain directly. The introduction of an HJ region reduces the tunneling length at the source–channel interface and enhances $I_{\rm ON}$, cf. Fig. 3(d) [38]. Unfortunately, the energy level of the lowest QS in the HJ region is lowered as $L_{\rm HJ}$ increases, and these carriers in the HJ region face an additional barrier between the HJ and the channel region, cf. dash circle in Fig. 3(e). In order for these carriers to move to the drain, tunneling across the triangular shape barrier on the right of the QS is necessary in Fig. 3(e), and hence, $I_{\rm ON}$ is degraded. However, a further increase in $L_{\rm HJ}$ results in the inclusion of the second or higher QS for the initial tunneling process in Fig. 3(f), leading to a slight increase in $I_{\rm ON}$ even if the phenomenon in Fig. 3(e) also occurs here. Note that, for the case of $L_{\rm HJ} = 2$ nm, only BTB tunneling is involved, and for larger $L_{\rm HJ}$, tunneling across the triangular barrier also plays a part in determining the current flow, which could contribute to the larger SS observed for larger $L_{\rm HJ}$ devices.

Next, we investigate how the I–V characteristics vary with different $W_{\rm HJ}$ at a fixed $L_{\rm HJ} = 2$ nm with the best performance from the above analysis. Varying $W_{\rm HJ}$ results in a change in the energy gap of the HJ region ($E_{G-{\rm HJ}}$), and for $W_{\rm HJ} =$ 2.5 and 1.5 nm, GNRs have $E_{G-{\rm HJ}} = 0.40$ and 0.95 eV, respectively [26]. The I–V characteristics of GNR HJ TFETs with different $E_{G-{\rm HJ}}$ are shown in Fig. 4(a). In addition to the aforementioned values, a semimetallic case ($W_{\rm HJ} =$ 200 nm, $E_{G-{\rm HJ}} \approx 0$ eV) and a homogeneous case ($W_{\rm HJ} =$ 1.2 nm, $E_{G-{\rm HJ}} = 1.22$ eV) are also included in Fig. 4(a) for comparison. For the semiconducting HJ cases, it is observed that, as $E_{G-{\rm HJ}}$ increases, the overall current decreases, with the $I_{\rm OFF}$ decrease much more prominent than $I_{\rm ON}$. $I_{\rm ON}$ decreases from 9.40 to 1.83 μA, whereas $I_{\rm OFF}$ decreased by two orders. $I_{\rm ON}/I_{\rm OFF}$ and the SS as functions of $E_{G-{\rm HJ}}$ are plotted in Fig. 4(b). Compared with the homogeneous cases, $I_{\rm ON}$ is slightly increased, but $I_{\rm OFF}$ increased a lot in the semimetallic HJ TFET. It is observed that $I_{\rm ON}/I_{\rm OFF}$ increases with $E_{G-{\rm HJ}}$, and the SS of the semiconducting HJs (at just above 20 mV/dec) is much lower than that of the semimetallic case.

The LDOS at the ON-states for $E_{G-{\rm HJ}} = 0.40$ and 0.95 eV are plotted in Fig. 4(c) and (d), respectively. An immediate effect of the change in $E_{G-{\rm HJ}}$ is observed in the tunneling length, which is increased by 16% as $E_{G-{\rm HJ}}$ is changed from 0.40 to 0.95 eV. In addition, the quantum-well structure diminishes as $E_{G-{\rm HJ}}$ increases, and the enhancement of $I_{\rm ON}$ due to the alignment of the QS is no longer possible. The combination of these two changes contributes to the reduced $I_{\rm ON}$ for larger $E_{G-{\rm HJ}}$. On the other hand, for the respective $E_{G-{\rm HJ}}$ at

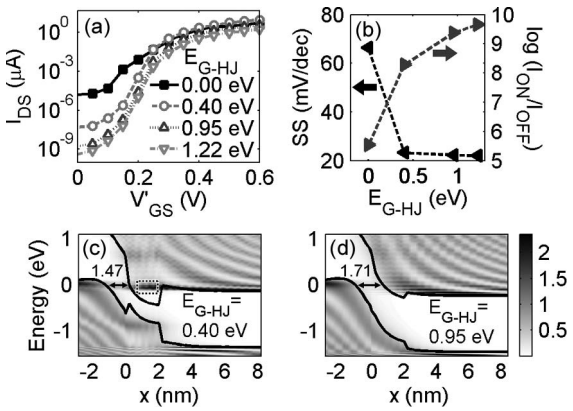

Fig. 4. (a) Current characteristics of GNR HJ TFETs for different HJ widths ($W_{\rm HJ} = 200, 2.5, 1.5,$ and 1.2 nm) and the corresponding bandgap ($E_{G-\rm HJ} = 0, 0.40, 0.95,$ and 1.22 eV). (b) $I_{\rm ON}/I_{\rm OFF}$ and SS of GNR HJ TFETs as a function of $E_{G-\rm HJ}$. The LDOS of devices with $E_{G-\rm HJ} =$ 0.40 and 0.95 eV are shown in (c) and (d), respectively, at $V'_{GS} = 0.6$ V. The dotted box in (c) indicates the quantum state formed in the well structure. The colorbar indicates the LDOS values with a unit of $[\times 10^{23}\ \rm cm^{-2} \cdot eV^{-1}]$ and is applied to (c) and (d).

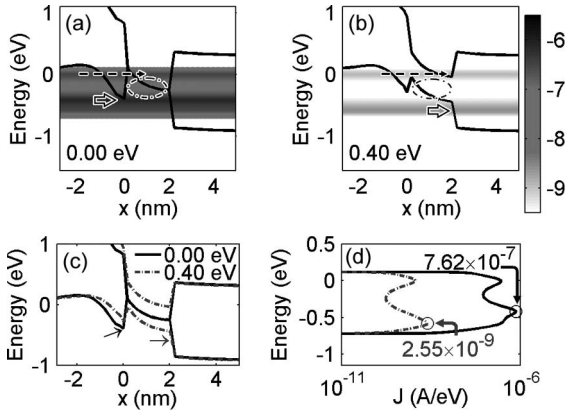

Fig. 5. Current flux for the GNR TFETs with (a) the semimetallic HJ ($E_{G-\rm HJ} = 0$ eV) and (b) the semiconducting HJ ($E_{G-\rm HJ} = 0.40$ eV), at $V'_{GS} = 0$ V. The colorbar applies to both (a) and (b) and represents the current density at each location in log scale with the unit [log(A/eV)]. (c) Band diagrams of the semimetallic and the semiconducting HJ cases, with arrows indicating the energy levels of the dark bands shown in (a) and (b). (d) Current density (J) at $x = 0$ nm. The source and the drain chemical potentials are at 0 and -0.6 eV, respectively.

OFF-states, $I_{\rm OFF}$ is mainly contributed by the tunneling across the channel, and it is observed that the effective tunneling length is longer for larger $E_{G-\rm HJ}$ and hence the reduced $I_{\rm OFF}$ for $E_{G-\rm HJ} = 0.95$ eV.

Furthermore, it can be found that the semimetallic case ($E_{G-\rm HJ} = 0$ eV) exhibits a dramatically large $I_{\rm OFF}$, 1.57×10^{-5} μA, compared with the semiconductor case ($E_{G-\rm HJ} =$ 0.40 eV) in Fig. 4(a). We examine the current flux at $V'_{GS} =$ 0 V, as shown in Fig. 5(a) and (b) for the two cases, in order to understand the difference in $I_{\rm OFF}$. It is observed that, in semiconductor and semimetal cases, the contributions of current come from carriers at two energy ranges (the darker bands), which are near the chemical potentials of the source and the drain. Near the source chemical potential (0 eV), there is BTB tunneling from the source to the HJ region [see dash arrows in Fig. 5(a) and (b)], and the tunneling length in the semimetallic case is shorter in the HJ region, and hence, a larger

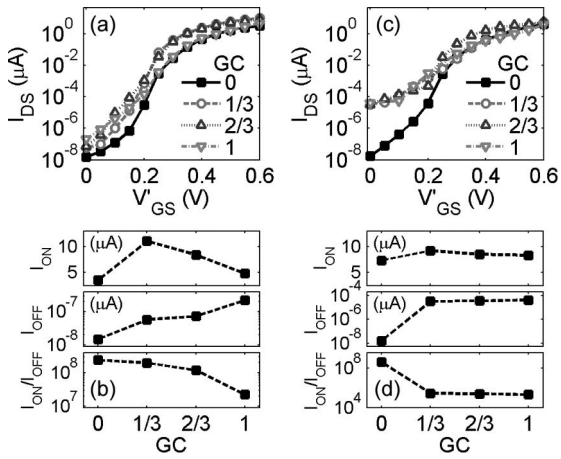

Fig. 6. Transfer characteristics of GNR HJ TFETs with different GC over the HJ region, GC $= 0, 1/3, 2/3,$ and 1 for (a) the semiconducting HJ ($E_{G-\rm HJ} =$ 0.40 eV), and the extracted $I_{\rm ON}$, $I_{\rm OFF}$, and $I_{\rm ON}/I_{\rm OFF}$ as a function of GC are shown in (b). The corresponding plots for the semimetallic HJ ($E_{G-\rm HJ} =$ 0 eV) are shown in (c) and (d), respectively. GC $= 0$ means the gate does not cover the HJ region, and vice versa. $V_{DS} = 0.60$ V for all simulations.

current flux is observed at that energy range. Near the drain chemical potential (-0.6 eV), the carrier contribution for the semimetallic case comes from a higher energy than that of the semiconducting case. To further illustrate the different mechanisms of the tunneling currents between the semimetal and the semiconductor cases, we superimpose the band diagrams in Fig. 5(a) and (b), as shown in Fig. 5(c). Whereas the Schottky barrier (arrow at $x = 0$ nm) determines the energy of carriers for transport for the semimetal case, the carriers are limited by the lowest point of the HJ region valence band (arrow at $x = 2$ nm) for the semiconductor case. In our simulation setup, the Schottky barrier is at a higher energy level than that of the lowest valence band, and hence, the dominant OFF-state current density for the semimetal is also higher than that of the semiconductor, near the drain chemical potential, cf. Fig. 5(d). Finally, the overall current density between the source and the drain is higher for the semimetallic case due to the absence of an energy bandgap in the HJ region, cf. dash-dot circles in Fig. 5(a) and (b), and these three factors combine to result in a higher $I_{\rm OFF}$ for the semimetallic case.

B. Effect of GC Over the HJ Region

Next, we investigate the influence of GC on the performance of the GNR HJ TFETs. $L_{\rm HJ}$ is chosen to be 6 nm for both the semiconducting ($E_{G-\rm HJ} = 0.40$ eV) and the semimetallic case ($E_G = 0$ eV). The I–V characteristics for the semiconducting HJ region are shown in Fig. 6(a), with the extracted $I_{\rm ON}$, $I_{\rm OFF}$, and $I_{\rm ON}/I_{\rm OFF}$ plotted in Fig. 6(b). The corresponding plots for the semimetallic HJ region are plotted in Fig. 6(c) and (d), respectively. For the semiconducting case, $I_{\rm ON}$ increases and subsequently falls to the original level as GC increases from 0 to 1, as shown in Fig. 6(b). On the other hand, $I_{\rm OFF}$ monotonously increases with GC by about an order of magnitude, resulting in a decreasing $I_{\rm ON}/I_{\rm OFF}$ as a function of GC. For the semimetallic case, $I_{\rm ON}$ is relatively constant, at about 8.3 μA for all GC, whereas $I_{\rm OFF}$ increases by three orders of magnitude as GC

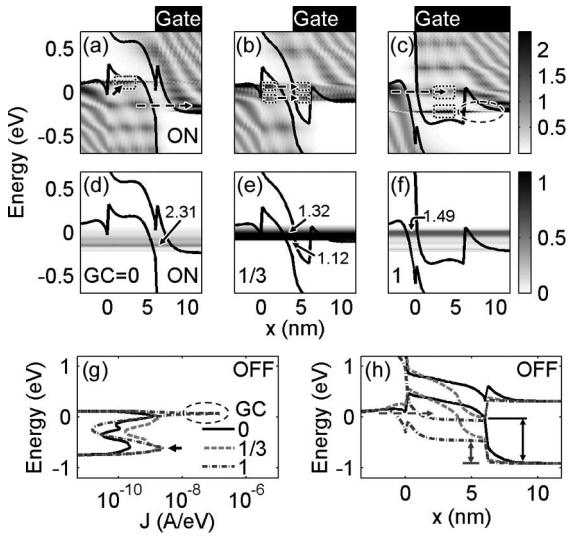

Fig. 7. LDOS of a GNR TFET with the semiconducting HJ region at $V'_{GS} = 0.6$ V for GC $= 0, 1/3,$ and 1 are shown in (a)–(c), respectively, and the corresponding current flux plots are shown in (d)–(f). The dotted boxes and dash arrows represent the quantum states and BTB tunneling processes, respectively. The positions of the gate are illustrated on top of (a)–(c) for clarity, and the numbers in (d)–(f) represent the tunneling length in [nm]. The colorbar beside (c) indicates the LDOS values with a unit of $[\times 10^{23}\ \mathrm{cm}^{-2} \cdot \mathrm{eV}^{-1}]$ and applies to (a)–(c), whereas the colorbar beside (f) represents the current flux in [A/eV] and applies to (d)–(f). The current densities (J) and band diagrams at $V'_{GS} = 0$ V are plotted in (g) and (h), respectively, for different GC. The legend in (g) applies to both (g) and (h). The channel–drain interface at $x = 20$ nm is not shown in (h).

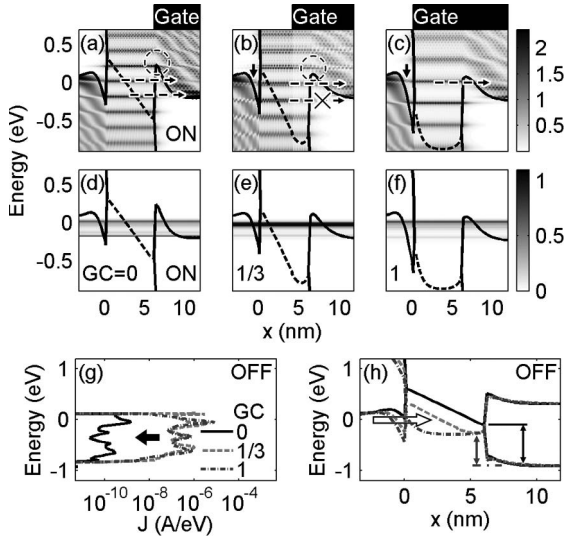

Fig. 8. LDOS of a GNR TFET with the semimetallic HJ region at $V'_{GS} = 0.6$ V for GC $= 0, 1/3,$ and 1 are shown in (a)–(c), respectively, and the corresponding current flux plots are shown in (d)–(f). The dash arrows represent tunneling processes across the triangle barrier. The positions of the gate are illustrated on top of (a)–(c) for clarity. The colorbar beside (c) indicates the LDOS values with a unit of $[\times 10^{23}\ \mathrm{cm}^{-2} \cdot \mathrm{eV}^{-1}]$ and applies to (a)–(c), whereas the colorbar beside (f) represents the current flux in [A/eV] and applies to (d)–(f). The dash lines in the semimetallic HJ region give an approximated value to the Fermi level in (a)–(f). The current densities (J) and band diagrams at $V'_{GS} = 0$ V are plotted in (g) and (h), respectively, for different GC. The legend in (g) applies to both (g) and (h). The channel–drain interface at $x = 20$ nm is not shown in (h).

changes from 0 to 1/3 and remains in the range of 10^{-5} μA for GC $>$ 1/3. The end result is a large $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ (about 10^8) at GC $= 0$ that drops to about 10^5 as GC increases, cf. Fig. 6(d).

We will first examine the semiconducting case, and the LDOS plots for different GC at the ON-state are shown in Fig. 7(a)–(c). The corresponding current flux plots in Fig. 7(d)–(f) help us in understanding the observed variation in I_{ON}, as shown in Fig. 6(a) and (b). For GC $= 0$, because the potential at the HJ region is not directly influenced by the gate, at the ON-state, BTB tunneling occurs between the HJ region and the gate-covered channel, cf. dash arrow in Fig. 7(a) and the dark band in Fig. 7(d). It is interesting to note that the first QS in the HJ region, which is indicated by the solid arrow in Fig. 7(a), does not contribute to I_{ON} as there are no carriers in the source region to populate it. At GC $= 1/3$, there are two factors that contribute to the larger I_{ON}: First, there are now two QSs [as indicated by dashed arrows in Fig. 7(b)] in the HJ region, which assist in BTB tunneling. Second, their BTB tunneling lengths become shorter [at 1.32 and 1.12 nm, respectively, as shown in Fig. 7(e)]. Finally, at GC $= 1$, BTB tunneling occurs between the source and the HJ region, and, similar to the case of GC $= 0$, the first QS in the HJ region is not a major contributor to I_{ON} but for a different reason: the energy level of the first QS falls below the conduction band edge of the channel on the right, and the carriers have to tunnel across the bandgap of the channel to reach the drain region, cf. dash circle in Fig. 7(c). Apart from being influenced by the changes in the QS as GC increases, I_{ON} is also influenced by the changes in the tunneling length of the BTB tunneling process as GC increases, as shown in Fig. 7(d)–(f). In particular, the tunneling length is shortest when the gate edge is in the HJ region [cf. GC $= 1/3$ in Fig. 7(e)], and this setup led to a larger tunneling rate and hence a larger I_{ON}. We note that the shortening of the tunneling length in the HJ region under a partially covered gate is driven by gate electrostatic alone and independent of the bandgaps, and hence, this observation is expected to be applicable to all HJ TFETs.

We now turn to the effects of GC on the OFF-state current density, as shown in Fig. 7(g), and the corresponding band bending, as shown in Fig. 7(h). For the OFF-state, there is a sharp peak in the current density near the source chemical potential for GC $= 1$, cf. dash circle in Fig. 7(g). This is due to an initial BTB tunneling between the source and the HJ region [cf. dash arrow in Fig. 7(h) for GC $= 1$], which is absent for other GC and contributes to the much higher I_{OFF}. On the other hand, the current density for GC $= 0$ exhibits a much lower peak near the drain chemical potential, which is indicated by the solid arrow in Fig. 7(g). This is related to the barrier height increase at the HJ–channel interface $(x = 6$ nm) experienced by the tunneling carriers from the HJ region to the drain across the channel region, as shown in Fig. 7(h). This is unique to GC $= 0$, and hence, I_{OFF} is much lower than other GC. For all other GC, I_{OFF} are expected to be similar and within that of GC $= 0$ and 1 cases.

We next examine the semimetallic HJ case and compare the corresponding observations, as shown in Fig. 8, to those of the semiconducting case. Although there seems to be little variation in I_{ON} for the different GC, as shown in Fig. 6(c) and (d), diverse mechanisms of carrier transport are at play for the different GC in the semimetallic case. For GC $= 0$, the QS in the HJ region majorly contributes to I_{ON}, whereas for

GC = 1/3, the lower energy QS has minor contribution as it is in the energy gap of the channel, cf. dash arrows in Fig. 8(a) and (b), and the corresponding dark bands in Fig. 8(d) and (e), respectively. Therefore, one should expect that $I_{\rm ON}$ for GC = 0 would be larger than that for GC = 1/3, which is inconsistent with the observation in Fig. 6(d). A more detailed examination of the band diagrams in Fig. 8(a) and (b) reveals that the height of the triangular barrier for the tunneling current is lowered due to the larger influence of the gate voltage as GC changes from 0 to 1/3, highlighted by dash circles, resulting in a slightly higher tunneling rate and $I_{\rm ON}$, consistent with the trend of $I_{\rm ON}$ in Fig. 6(d). However, as GC further increases, the enhancement in the tunneling current from the lowering of the triangular barrier is offset by the increase in the tunneling length for carriers going from the source to the HJ region, cf. solid arrows in Fig. 8(b) and (c). A superposition of these two factors results in the minimal variation in $I_{\rm ON}$ as GC varies. On the other hand, $I_{\rm OFF}$ is abnormally low for GC = 0, and it is observed that its OFF-state current density is four orders of magnitude lower than other GC, as shown in Fig. 8(g). This can be explained by the observation that, except for GC = 0, the carriers from the valence band of the source travel to the conduction bands of the HJ region, cf. empty arrow in Fig. 8(h), before tunneling across the bandgap of the channel. In addition, in the GC $>$ 0 cases, the carriers in the valence band of the HJ region experience a lower tunneling barrier at the HJ–channel interface ($x = 6$ nm) than those in GC = 0, as shown in Fig. 8(h). These mechanisms result in a much lower $I_{\rm OFF}$ for the semimetallic HJ case when GC = 0.

Overall, the semimetallic case provides a larger and more consistent $I_{\rm ON}$ than the semiconducting case for all GC. At GC = 0, the semimetallic case has a better performance with a slightly larger $I_{\rm ON}$ and $I_{\rm ON}/I_{\rm OFF}$ ratio compared with that of the semiconductor case. However, for GC $>$ 0, the semiconductor case has a better performance in $I_{\rm ON}/I_{\rm OFF}$ due to its lower $I_{\rm OFF}$ (at about three orders of magnitude lower) compared with that of the semimetallic case, and this would usually be the case in realistic devices due to the difficulty faced in having an exact alignment of the gate edge to the source–HJ interface.

Finally, we note that, while only a particular GNR width is considered here for the channel region, a wider GNR can be used to increase the total current due to a smaller E_G, similar to the case of uniform-width devices [36]. Furthermore, in the current study of the ballistic performance of GNR HJ TFETs, scattering processes such as line-edge roughness scattering and phonon scattering are not included. It is found that line-edge roughness degrades the device performance of uniform-width GNR TFETs [23], [24], whereas elastic phonon scattering enhances the BTB tunneling currents [34]. The interactions between these scattering processes and the HJ region will need to be studied before the successful implementation of GNR HJ TFETs.

IV. Conclusion

In conclusion, we have studied the I–V characteristics of GNR HJ TFETs with semiconducting and semimetallic HJ regions embedded in the channel with varying GC. It is demonstrated that an effective modulation of the bands in the HJ region by varying its length and width allows optimization of the device performance. As the length of the HJ region increases, $I_{\rm OFF}$ increases due to the lowering of the QS in a widening HJ region to the source chemical potential and hence facilitating OFF-state tunneling. On the other hand, $I_{\rm ON}$ decreases with the HJ length due to the formation of a barrier blocking a direct source to channel tunneling current flow. The overall result is a lowering of the $I_{\rm ON}/I_{\rm OFF}$ ratio as a function of the HJ length. On the other hand, $E_{G-{\rm HJ}}$ increases when the width of the HJ region decreases, resulting in an overall decrease in current. Compared with the semimetallic case, the semiconducting HJ TFET has more flexibility in changing the device performance by varying GC and the energy bandgap in the HJ region. These physical insights may provide a path for enhancing the device performance and facilitating the development of HJ TFETs.

References

[1] A. H. Castro Neto, F. Guinea, R. Peres, K. S. Novoselov, and A. K. Geim, "The electronic properties of graphene," *Rev. Mod. Phys.*, vol. 81, no. 1, pp. 109–162, Jan. 2009.

[2] N. Stander, B. Huard, and D. Goldhaber-Gordon, "Evidence for Klein tunneling in graphene $p-n$ junctions," *Phys. Rev. Lett.*, vol. 102, no. 2, pp. 026807-1–026807-4, Jan. 2009.

[3] C. L. Kane and E. J. Mele, "Quantum spin Hall effect in graphene," *Phys. Rev. Lett.*, vol. 95, no. 22, pp. 226801-1–226801-4, Nov. 2005.

[4] G. M. Rutter, J. N. Crain, N. P. Guisinger, T. Li, P. N. First1, and J. A. Stroscio, "Scattering and interference in epitaxial graphene," *Science*, vol. 317, no. 5835, pp. 219–222, Jul. 2007.

[5] X. Li, X. Wang, L. Zhang, S. Lee, and H. Dai, "Chemically derived, ultrasmooth graphene nanoribbon semiconductors," *Science*, vol. 319, no. 5867, pp. 1229–1232, Feb. 2008.

[6] X. Wang, Y. Ouyang, X. Li, H. Wang, J. Guo, and H. Dai, "Room-temperature all-semiconducting sub-10-nm graphene nanoribbon field effect transistors," *Phys. Rev. Lett.*, vol. 100, no. 20, pp. 206803-1–206803-4, May 2008.

[7] M. C. Lemme, T. J. Echtermeyer, M. Baus, and H. Kurz, "A graphene field-effect device," *IEEE Electron Device Lett.*, vol. 28, no. 4, pp. 282–284, Apr. 2007.

[8] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, and A. A. Firsov, "Electric field effect in atomically thin carbon films," *Science*, vol. 306, no. 5696, pp. 666–669, Oct. 2004.

[9] Y. Ouyang, P. Campbell, and J. Guo, "Analysis of ballistic monolayer and bilayer graphene field-effect transistors," *Appl. Phys. Lett.*, vol. 92, no. 6, pp. 063120-1–063120-1, Feb. 2008.

[10] Y. J. Shin, G. Kalon, J. Son, J. H. Kwon, J. Niu, C. S. Bhatia, G. Liang, and H. Yang, "Tunneling characteristics of graphene," *Appl. Phys. Lett.*, vol. 97, no. 6, pp. 252102-1–252102-3, Dec. 2010.

[11] T. Sohier and B. Yu, "Ultralow-voltage design of graphene PN junction quantum reflective switch transistor," *Appl. Phys. Lett.*, vol. 98, no. 21, pp. 213104-1–213104-3, May 2011.

[12] V. V. Cheianov, V. Fal'ko, and B. L. Altshuler, "The focusing of electron flow and a Veselago lens in graphene p-n junctions," *Science*, vol. 315, no. 5816, pp. 1252–1255, Mar. 2007.

[13] A. Qaiumzadeh and R. Asgari, "The effect of sublattice symmetry breaking on the electronic properties of doped graphene," *New J. Phys.*, vol. 11, no. 9, p. 095023, May 2009.

[14] D. W Boukhvalov and M. I. Katsnelson, "Chemical functionalization of graphene," *J. Phys., Condens. Matter*, vol. 21, no. 34, p. 344 205, Aug. 2009.

[15] Y.-W. Son, M. L. Cohen, and S. G. Louie, "Energy gaps in graphene nanoribbons," *Phys. Rev. Lett.*, vol. 97, no. 21, p. 216 803, Nov. 2006.

[16] M. Ezawa, "Peculiar width dependence of the electronic properties of carbon nanoribbon," *Phys. Rev. B*, vol. 73, no. 4, p. 045432, Jan. 2006.

[17] C. Metzger, S. Remi, M. Liu, S. V. Kusminskiy, A. H. Castro Neto, A. K. Swan, and B. B. Goldberg, "Biaxial strain in graphene adhered to shallow depressions," *Nano Lett.*, vol. 10, no. 1, pp. 6–10, Jan. 2010.

[18] Y.-W. Son, M. L. Cohen, and S. G. Louie, "Half-metallic graphene nanoribbon," *Nature*, vol. 444, no. 7117, pp. 347–349, Nov. 2006.

[19] L. Tapaszto, G. Dobrik, P. Lambin, and L. P. Biro, "Tailoring the atomic structure of graphene nanoribbons by scanning tunnelling microscope lithography," *Nat. Nanotechnol.*, vol. 3, no. 7, pp. 397–401, Jul. 2008.
[20] A. Jarvey, J. Guo, Q. Wang, M. Lundstrom, and H. J. Dai, "Ballistic carbon nanotube field-effect transistors," *Nature*, vol. 424, no. 6949, pp. 654–657, Aug. 2003.
[21] J. Appenzeller, Y.-M. Lin, J. Knoch, and P. Avouris, "Band-to-band tunneling in carbon nanotube field effect transistors," *Phys. Rev. Lett.*, vol. 93, no. 19, p. 196 805, Nov. 2004.
[22] S. O. Koswatta, M. S. Lundstrom, and D. E. Nikonov, "Band-to-band tunneling in a carbon nanotube metal–oxide–semiconductor field-effect transistor is dominated by phonon-assisted tunneling," *Nano Lett.*, vol. 7, no. 5, pp. 1160–1164, Feb. 2007.
[23] M. Luisier and G. Klimeck, "Performance analysis of statistical samples of graphene nanoribbon tunneling transistors with line edge roughness," *Appl. Phys. Lett.*, vol. 94, no. 22, pp. 223505-1–223505-3, Jun. 2009.
[24] Y. Yoon and J. Guo, "Effect of edge roughness in graphene nanoribbon transistors," *Appl. Phys. Lett.*, vol. 91, no. 7, pp. 073103-1–073103-3, Aug. 2007.
[25] G. Fiori and G. Iannaccone, "Simulation of graphene nanoribbon field-effect transistors," *IEEE Electron Device Lett.*, vol. 28, no. 8, pp. 760–762, Aug. 2007.
[26] Q. Zhang, T. Fang, H. Xing, A. Seabaugh, and D. Jena, "Graphene nanoribbon tunnel transistors," *IEEE Electron Device Lett.*, vol. 29, no. 12, pp. 1344–1346, Dec. 2008.
[27] Q. Zhang, Y. Lu, H. G. Xing, S. J. Koester, and S. O. Koswatta, "Scalability of atomic-thin-body (ATB) transistors based on graphene nanoribbons," *IEEE Electron Device Lett.*, vol. 31, no. 6, pp. 531–533, Jun. 2010.
[28] D. Jena, T. Fang, Q. Zhang, and H. L. Xing, "Zener tunneling in semiconducting nanotube and graphene nanoribbon p-n junctions," *Appl. Phys. Lett.*, vol. 93, no. 11, pp. 112106-1–112106-3, Sep. 2008.
[29] B. Obradovic, R. Kotlyar, F. Heinz, P. Matagne, T. Rakshit, D. Nikonov, M. D. Giles, and M. A. Stettler, "Analysis of graphene nanoribbons as a channel material for field-effect transistors," *Appl. Phys. Lett.*, vol. 88, no. 14, pp. 142102-1–142102-3, Apr. 2006.
[30] G.-C. Liang, N. Neophytos, D. Nikonov, and M. Lundstrom, "Performance projections for ballistic graphene nanoribbon field-effect transistors," *IEEE Trans. Electron Devices*, vol. 54, no. 4, pp. 677–682, Apr. 2007.
[31] W. Y. Choi, B.-G. Park, J. D. Lee, and T.-J. K. Liu, "Tunneling field-effect transistors (TFETs) with subthreshold swing (SS) less than 60 mV/dec," *IEEE Electron Device Lett.*, vol. 28, no. 8, pp. 743–745, Aug. 2007.
[32] Y. Ouyang, Y. Yoon, and J. Guo, "Scaling behaviors of graphene nanoribbon field-effect transistors: A three-dimensional quantum simulation study," *IEEE Trans. Electron Devices*, vol. 54, no. 9, pp. 2223–2231, Sep. 2007.
[33] P. Zhao, J. Chauhan, and J. Guo, "Computational study of tunneling transistor based on graphene nanoribbon," *Nano Lett.*, vol. 9, no. 2, pp. 684–688, Jan. 2009.
[34] S. O. Koswatta, M. S. Lundstrom, and D. E. Nikonov, "Performance comparison between p-i-n tunneling transistors and conventional MOSFETs," *IEEE Trans. Electron Devices*, vol. 56, no. 3, pp. 456–465, May 2009.
[35] S.-K. Chin, D. W. Seah, K.-T. Lam, G. S. Samudra, and G. C. Liang, "Device characteristics and physics of ballistic graphene nanoribbon tunneling FET," *IEEE Trans. Electron Device*, vol. 57, no. 11, pp. 3144–3152, Nov. 2010.
[36] K.-T. Lam, S. K. Chin, D. W. Seah, S. Bala Kumar, and G. Liang, "Effect of ribbon width and doping concentration on device performance of graphene nanoribbon tunneling field-effect transistors," *Jpn. J. Appl. Phys.*, vol. 49, no. 4, pp. 04DJ10-1–04DJ10-5, Apr. 2010.
[37] K.-T. Lam, D. W. Seah, S.-K. Chin, S. B. Kumar, G. Samudra, Y.-C. Yeo, and G. C. Liang, "A simulation study of graphene nanoribbon tunneling FET with heterojunction channel," *IEEE Electron Device Lett.*, vol. 31, no. 6, pp. 555–557, Jun. 2010.
[38] Y. Yoon and S. Salahuddin, "Barrier-free tunneling in a carbon heterojunction transistor," *Appl. Phys. Lett.*, vol. 97, no. 3, pp. 033102-1–033102-3, Jul. 2010.
[39] Y. Yoon, S. H. Kim, and S. Salahuddin, "Performance analysis of carbon-based tunnel field-effect transistors for high frequency and ultralow power applications," *Appl. Phys. Lett.*, vol. 97, no. 23, pp. 233504-1–233504-3, Dec. 2010.
[40] S. Datta, *Quantum Transport: Atom to Transistor*. New York: Cambridge Univ. Press, 2005, ch. 11, pp. 305–307.
[41] M. P. L. Sancho, J. M. L. Sancho, and J. Rubio, "Highly convergent schemes for the calculation of bulk and surface green functions," *J. Phys. F, Metal Phys.*, vol. 15, no. 4, pp. 851–858, Apr. 1985.
[42] S. M. Sze, *Semiconductor Devices: Physics and Technology*, 2nd ed. New York: Wiley, 2002, ch. 3, pp. 73–75.
[43] S.-K. Chin, K.-T. Lam, D. Seah, and G. Liang, "Quantum transport simulations of graphene nanoribbon devices using Dirac equation calibrated with tight-binding π-bond model," *Nanoresearch Lett.*, vol. 7, p. 114, Feb. 2012, doi: 10.1186/1556-276X-7-114.
[44] L. Brey and H. A. Fertig, "Electronic states of graphene nanoribbons studied with the Dirac equation," *Phys. Rev. B*, vol. 73, no. 23, p. 235 411, Jun. 2006.
[45] Z. Ren, Nanoscale MOSFETs: Physics, Simulation and Design, 2006. [Online]. Available: http://nanohub.org/resources/1917
[46] E. H. Hwang, S. Adam, and S. Das Sarma, "Carrier transport in two-dimensional graphene layers," *Phys. Rev. Lett.*, vol. 98, no. 18, p. 186 806, May 2007.
[47] K. W.-K. Shung, "Dielectric function and plasmon structure of stage-1 intercalated graphite," *Phys. Rev. B*, vol. 34, no. 2, pp. 979–993, Jul. 1986.

Haixia Da received the M.S. and Ph.D. degrees in physics from Soochow University, Suzhou, China, in 2005 and 2008, respectively.

Currently, she is a Postdoctoral Research Fellow with the Department of Electrical and Computer Engineering, National University of Singapore, Singapore. Her research interests include modeling and exploring the physics of graphene nanoribbon devices. She has also investigated the transport properties of molecular devices. Furthermore, she also works on first-principles calculations of the electronic and magnetic properties in low-dimensional systems.

Kai-Tak Lam (S'07) received the B.Eng. degree in electrical and computer engineering from National University of Singapore, Singapore, in 2006, where he has been working toward the Ph.D. degree in electrical and computer engineering since 2007.

His research focuses on computational modeling and simulations of carrier transport in carbon-based nanodevices, for example, the resonant tunneling diodes and the tunneling field-effect transistors. He has also investigated the fringing field effect on the carrier transport in graphene nanoribbon tunneling field-effect transistors and is currently working on the carrier scattering investigations on the graphene nanoribbon devices.

G. Samudra (M'87) received the Ph.D. degree from Purdue University, West Lafayette, IN, in 1985.

He is currently an Associate Professor with the Silicon Nano Device Laboratory, Department of Electrical and Computer Engineering, National University of Singapore (NUS), Singapore, and has been teaching for about 19 years. He was a Visiting Professor with the Massachusetts Institute of Technology, Cambridge, in 2001. Before joining NUS, he was with Texas Instruments Incorporated for three years, where he worked on the development of technology computer-aided design tools linking the device and the circuit simulator and defining 3-D structures for simulation. At NUS, he is involved in research projects in the area of simulation and novel devices. He is the author of 200 technical papers published in journals and conference proceedings.

Sai-Kong Chin received the Ph.D. degree in theoretical physics from the University of Manchester, Manchester, U.K., in 1997.

He is currently with the Institute of High Performance Computing, Agency for Science, Technology and Research (A*STAR), Singapore, as a Senior Research Engineer in the Materials Science and Engineering Department. His current research interests include quantum simulations of nanostructures and devices.

Gengchiau Liang (S'05–M'07) received the B.S. and M.S. degrees in physics from National Tsinghua University, Hsinchu, Taiwan, in 1995 and 1997, respectively, and the Ph.D. degree in electrical and computer engineering from Purdue University, West Lafayette, IN, in 2005.

He was a Postdoctoral Research Associate in electrical engineering with Purdue University, and, currently, he is an Assistant Professor with the Department of Electrical and Computer Engineering, National University of Singapore, Singapore. His research interests include modeling and exploring the physics of nanoscale electronic devices, including molecular, carbon nanotube/ribbon, and nanowire devices. Recently, he has focused on investigating thermoelectric properties and their applications on the energy-harvesting devices. Furthermore, he also works on developing the novel functional devices for low-power consumption switches.