A CMOS High-Voltage Transmitter IC for Ultrasound Medical Imaging Applications

Hyouk-Kyu Cha, *Member, IEEE*, Dongning Zhao, Jia Hao Cheong, Bin Guo, Hongbin Yu, and Minkyu Je, *Member, IEEE*

***Abstract*—A high-voltage (HV) transmitter integrated circuit for ultrasound medical imaging applications is implemented using 0.18-μm bipolar/CMOS/DMOS technology. The proposed HV transmitter achieves high integration by only employing standard CMOS transistors in a stacked configuration with dynamic gate biasing circuit while successfully driving the capacitive micromachined ultrasound transducer device immersed in an oil environment without breakdown reliability issues. The HV transmitter including the output driver and the voltage level shifters generates over 10-V_{p-p} pulses at 1.25-MHz frequency and occupies only 0.022 mm^2 of core die area.**

***Index Terms*—Capacitive micromachined ultrasound transducer (CMUT), dynamic gate biasing, high-voltage (HV) transmitter, level shifter, output driver, ultrasound medical imaging.**

I. Introduction

In RECENT years, the ultrasound imaging has gained much interest in the medical field due to its less-harmful characteristic to the human body in comparison with other well-known methods such as magnetic resonance imaging, computed tomography, and X-rays. In addition, the emergence of the capacitive micromachined ultrasound transducer (CMUT) device technology [1] during the last decade has propelled the interest even further. In comparison with its piezoelectric counterpart, the CMUT provides the advantages of wider operational bandwidth, simpler fabrication for large array implementations, and more ease of integration with the front-end integrated circuits (ICs) due to compatibility with the standard CMOS process. Most recently, 2-D CMUT arrays with integrated front-end ICs have been developed for 3-D ultrasound volumetric imaging for improved benefits such as higher resolution and signal-to-noise ratio (SNR) [2].

Fig. 1 shows a typical ultrasound system block diagram for medical imaging applications. The ultrasound system consists of a transducer array, an interface transceiver comprised of a high-voltage (HV) transmitter and a low-noise receiver, and image/signal processing blocks for image construction. The analog front end of the transceiver plays a critical role in deciding the overall system performance such as the sensitivity and the SNR of the ultrasound system [3], [4].

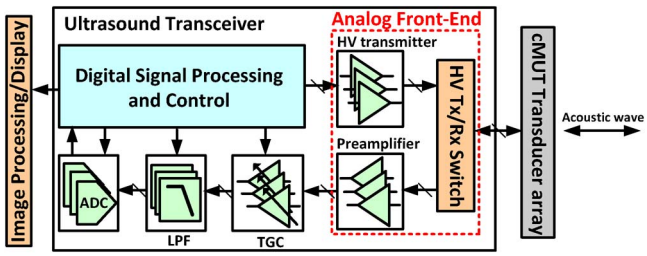

Fig. 1. Block diagram of a typical ultrasound medical imaging system.

In order to support large-size 2-D arrays, a large number of transducer elements are required, which then leads to an increase in the number of closely packed flip-chip-bonded interfacing front-end IC cells, posing significant integration issues due to the limited die area available for each cell. One of the main issues is the area-hungry HV transmitter in the interfacing analog front-end IC. The HV transmitter usually utilizes large-size HV double-diffused MOS (DMOS) transistors [2], [5], [6] to generate HV output pulse signals to drive the CMUT to produce large acoustic pressure while maintaining the reliability to prevent possible device junction breakdown.

In this brief, a highly integrated HV transmitter utilizing standard CMOS transistors targeted for ultrasound medical imaging in a highly integrated needle device for obstetrics and gynecology applications is presented. Both the HV output pulse driver and the level shifter adopts the proposed multiple-stacked architecture with dynamic gate biasing circuit in order to generate over 10-V_{p-p} pulse signal at 1.25-MHz frequency while driving the CMUT device immersed in an oil environment. A 10-V drive voltage, which is lower than typical ultrasound applications, is chosen in this work for several reasons: 1) A CMUT device with a thin membrane and low collapse voltage is to be used for integration with the developed IC. 2) The resulting generated acoustic pressure meets the application requirements. 3) The amount of dynamic power consumption during operation has to be minimized considering tissue heating as the needle is to be inserted into the human tissue. Section II briefly addresses the transmitter architecture, while Section III describes the circuit design in detail. Section IV presents the experimental results followed by the conclusions in Section V.

Manuscript received August 19, 2012; revised November 13, 2012 and December 26, 2012; accepted March 24, 2013. Date of publication April 25, 2013; date of current version June 12, 2013. This work supported by the Science and Engineering Research Council of the Agency for Science, Technology, and Research (A*STAR), Singapore, under Grant 102 148 0005, Grant 102 148 0007, and Grant 102 148 0008. This brief was recommended by Associate Editor G. Yuan.

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Digital Object Identifier 10.1109/TCSII.2013.2258260

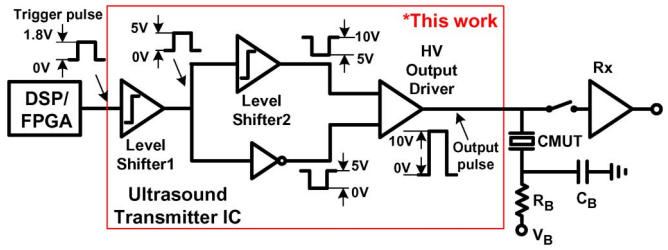


Fig. 2. Architecture of HV ultrasound transmitter.

II. Architecture of HV Transmitter

The overall architecture of the HV ultrasound transmitter is shown in Fig. 2. The architecture consists of a level shifter, which converts the external digital-signal-processor/field-programmable-gate-array generated 1.8-V_{p-p} input trigger signal to a 5-V_{p-p} pulse signal. Then, the 5-V_{p-p} signal is divided into two separate paths. The upper path contains a second level shifter and a tapered buffer to convert the signal to swing between 5 and 10 V in order to drive the gate of the PMOS transistor of the output driver. The lower path, on the other hand, goes through inverter-based buffers to drive the gate of the NMOS transistor of the output driver. The output driver is followed by the CMUT element where the CMUT is driven with a 10-V_{p-p} HV pulse so that an ultrasound signal with sufficient acoustic pressure is generated for propagation through the acoustic medium. The pulsewidth, the period, and the required amount of generated acoustic pressure, which relates to the maximum voltage of the output pulse signal, are decided in the system level depending on the specific medical imaging application, as well as the device characteristics of the following transducer. The other terminal of the CMUT device is connected to a dc bias voltage through a large bias resistor R_B and a bypass ac capacitor C_B, for biasing the CMUT near the breakdown voltage for high transmit efficiency. The output-driver and CMUT interface is also connected to the receiver analog front end, which consists of a HV isolation switch and a low-noise preamplifier to amplify the incoming weak electrical current signal converted from the reflected ultrasound signal, so that it can be processed in the following stages for image construction. This work presents the HV transmitter part of the overall ultrasound analog transceiver front end.

III. Circuit Design

A. Previous HV Transmitter

Fig. 3 shows the previously developed HV transmitter [5], [6], which consists of a level shifter and an output driver to drive the following transducer with a large voltage swing in order to generate sufficiently high acoustic pressure signal. In order to prevent the junction breakdown of the regular MOS transistors during the HV operation, special transistors known as DMOS transistors, which can sustain a high drain-to-source voltage, are used in both the level shifter and the output driver, and hence, reliability in the circuit operation is maintained. The disadvantage of these DMOS transistors is the added process cost, the increased layout size, and the parasitic capacitance.

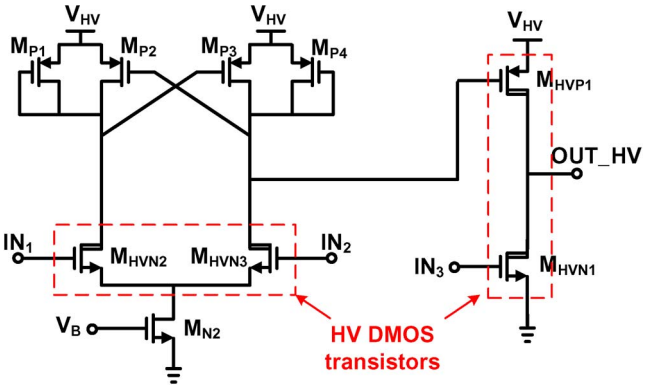


Fig. 3. Simplified schematic of the previous HV transmitter.

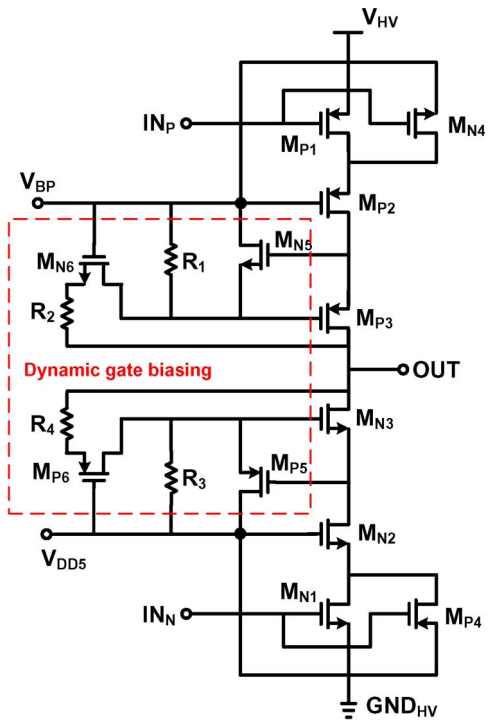


Fig. 4. Schematic of the proposed HV output driver.

In addition, the device ON-resistance of these transistors is larger than that of regular CMOS transistors, and the sizing has to be sufficiently large in order to drive the following CMUT element to an HV at megahertz frequencies. As more ultrasound systems for medical imaging applications require high-density 2-D arrays for improved system performance, it is inevitable that the analog front-end IC provides higher integration to minimize the overall die area and lower the manufacturing cost.

B. Proposed HV Transmitter

As shown in Fig. 2, in the previous section, the proposed ultrasound transmitter IC consists of three stages. The key part in the transmitter chain is the push–pull output driver, which excites the following CMUT with a HV pulse signal to produce a large acoustic pressure signal. Fig. 4 shows the schematic of the proposed HV output driver. In comparison with the output

driver stage in the previous HV transmitter, all the HV DMOS transistors M_{HVN1} and M_{HVP1} in Fig. 3 are replaced with 5-V standard CMOS transistors. The voltage capability of thin and thick oxide transistors readily provided by the process is extended through stacking [7], [8]. Although two stacks of 5-V transistors can theoretically support 10-V drain-to-source voltage, three stacks of NMOS transistors M_{N1}, M_{N2}, and M_{N3}, and PMOS transistors M_{P1}, M_{P2}, and M_{P3} are used in this version to support over 10-V$_{p-p}$ output swing with margin to operate without oxide or junction breakdown reliability issues for all different process, voltage, and temperature corners. To make the smooth push–pull operation possible, dynamic gate biasing circuit is utilized to correctly bias the gate of the stacked transistors during transitions and also limits the internal nodes to be within the allowable voltage range. The dynamic gate biasing circuit, consisting of R_1, R_2, R_3, and R_4 resistors, and M_{N5}, M_{N6}, M_{P5}, and M_{P6} transistors, is a design improved from the circuit structure in [9] with reduced number of passive components and overall complexity. For our design, as the operation frequency is lower and the sizing of the transistors is smaller, the parasitic gate–drain capacitance, which causes the overshoot during ON–OFF transitions, was not critical, and therefore, the area-consuming capacitors and resistors were removed to minimize the overall area after verifying with an extensive amount of corner simulations. Also, the addition of M_{P4} and M_{N4} transistors helps in quickly defining the nodes during transitions.

For the operation analysis of the output driver, two operation state transitions are considered for the NMOS output part.

When IN$_N$ becomes logic "high" (a low-to-high input transition from 0 to 5 V), this will turn on M_{N1}, which will cause the source node of M_{N2} to become discharged, and turn on M_{N2} as the gate of M_{N2} is constantly biased at V_{DD5}. As the drain of M_{N2} becomes discharged, this turns on M_{P5} and causes the gate of M_{N3} to be shorted to V_{DD5}, also turning on M_{N3}. The voltage at the output node is discharged and becomes equal to $\mathrm{GND_{HV}} + V_{DS\_\mathrm{MN1,2,3}}$, where $V_{DS\_\mathrm{MN1,2,3}}$ is equal to the voltage drop due to the dynamic current flowing through the output drain terminals multiplied by the combined R_{ON} resistance of M_{N1}, M_{N2}, and M_{N3}. The size ratio (W/L) of the output transistors is relatively large in order to reduce the ON-resistance to minimize the voltage drop during the ON operation. However, the area and the parasitic capacitance, which results as a tradeoff is also considered, which decides the overall size. At this state, both M_{P4} and M_{P6} are OFF as the source–gate voltage is nearly equal and is thus at cutoff.

When IN$_N$ becomes logic "low" (a high-to-low input transition), this will turn off M_{N1} but turn on M_{P4}, which will cause both the gate and source nodes of M_{N2} to be biased at V_{DD5}, which turns off M_{N2}. Now, as the output node makes a transition from "low" to "high," this triggers M_{P6} to turn on. Then, the gate voltage of M_{N3} is decided by the resistive division of R_4, $R_{\mathrm{ON\_MP6}}$, and R_3 resistors between the output node and the bias voltage of M_{N2}, which is at V_{DD5}.

During the push–pull operation, the HV output voltage, which can exceed over 10 V$_{p-p}$, is distributed among drain-to-source terminals of the stacked transistors. In addition, as the drain-to-body junction breakdown voltage is over 14 V, no reliability problems exist. The operation for the PMOS part is identical to the NMOS part, except that it is complementary.

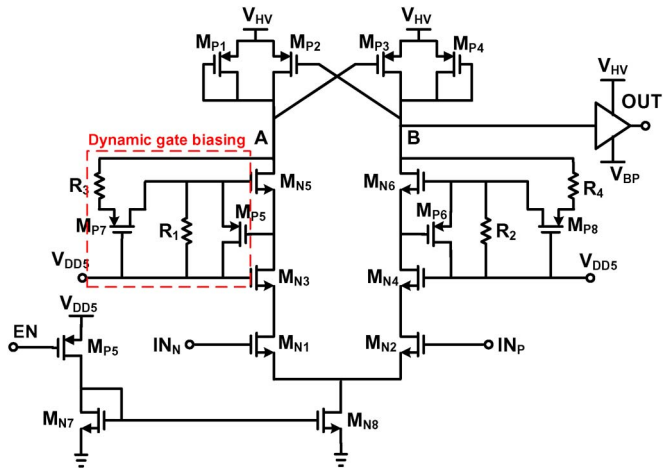


Fig. 5. Schematic of the proposed 5- to 10-V level shifter.

Fig. 5 shows the second level shifter and the tapered buffer used to convert a 0- to 5-V swinging pulse to a 5- to 10-V pulse to drive the PMOS gate of the output driver. Similar to the output driver, all the transistors used are standard thin-oxide 1.8-V or thick-oxide 5-V CMOS transistors provided by the process. The gate of M_{N1} (IN$_N$) is driven by a 5-V$_{p-p}$ pulse signal, while the gate of M_{N2} (IN$_P$) is driven by the inverted 5-V$_{p-p}$ pulse. When IN$_N$ is logic "high," this will turn on M_{N1}, which will cause the source node of M_{N3} to become discharged and turn on M_{N3} as the gate of M_{N3} is constantly biased at V_{DD5}. As the drain of M_{N3} becomes discharged, this turns on M_{P5} and causes the gate of M_{N5} to be shorted to V_{DD5}, also turning on M_{N5}. The voltage of "A" node becomes $V_{\mathrm{HV}} - V_{DS\_\mathrm{MP1}}$, which turns on M_{P3}, and node "B" is shorted to V_{HV}. Both the "A" and "B" nodes make transitions between V_{HV} and $V_{\mathrm{HV}} - V_{DS\_\mathrm{MP1,4}}$, in which $V_{DS\_\mathrm{MP1,4}}$ is decided to be around 5 V controlled by the sizing of the $M_{P1,4}$ transistors. The following tapered buffer adjusts the output signal to swing between V_{HV} and V_{BP}, where V_{BP} is controlled to be approximately a half of V_{HV}.

The first-stage level shifter in Fig. 2 is a conventional static level shifter [10] used to convert a 1.8-V$_{p-p}$ signal to 5-V$_{p-p}$ signal.

Fig. 6 shows the transient simulation plot in which a 1.8-V$_{p-p}$ 384-ns-pulsewidth input trigger signal is applied to the first level-shifter input and the 10-V$_{p-p}$ pulse signal results at the output of the driver with small delay. All the internal nodes meet the process limits for all simulation corners. The load condition at the output driver in this simulation is an equivalent electrical CMUT model with a parallel capacitance of 10 pF.

A special attention is given in the layout stage to isolate the HV operating circuits and the regular voltage parts. Also, wide top metals are used to route the HV supply, the HV ground, and the output nodes from the core to the pads to minimize the parasitic resistance and support high dynamic current through this path. In comparison with previous HV transmitter designs using DMOS devices, the core area including the output driver and the two level shifters has been dramatically reduced.

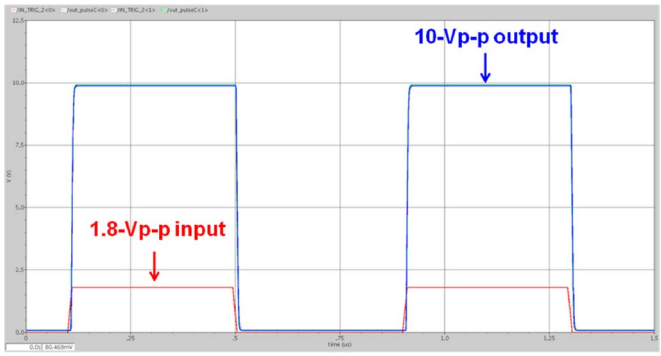


Fig. 6. Transient simulation plot capture for input trigger versus HV output pulse.

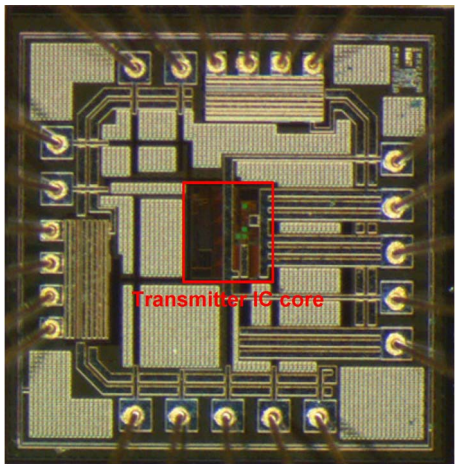


Fig. 7. Chip microphotograph of the implemented transmitter IC.

IV. Experimental Results

A. Transmitter IC Characterization

The HV ultrasound transmitter is fabricated in one-poly six-metal (1P 6M) 0.18-μm bipolar/CMOS/DMOS (BCD) process supporting up to 30 V of drain-to-source voltage and 5-V gate-to-source voltage for DMOS devices. The 1.8- and 5/6-V standard CMOS devices are also supported. No HV DMOS devices were utilized in the design for the proposed HV transmitter. The chip microphotograph is shown in Fig. 7, where the total chip area of the core is 0.022 mm^2. All the pads except the HV supply and output pads include electrostatic-discharge circuits using diode pairs. Fig. 8 shows the measured capture of the 1.8-V_{p-p} input trigger pulse versus the output 9.8-V_{p-p} pulse signal at a frequency of 1.25 MHz driving a 15-pF capacitive load at the output. The output signal rise and fall times are measured to be 40–50 ns, while the input–output delay time is 22.5 ns. The external input trigger signal is provided by an arbitrary waveform generator. Up to 13 V_{p-p} of output voltage pulse is generated without issues. Table I summarizes the measured transmitter IC performance.

B. Acoustic Transmission Testing With IC and CMUT

Next, the acoustic transmission experiment is carried out with the transmitter IC and in-house developed CMUT elements with a cell size of 30–90 μm, a gap size of 100 nm, and a membrane thickness of 3 μm. CMUT samples with a center frequency at a few megahertz are used for the testing. Fig. 9 shows the cross-sectional and scanning electron microscope (SEM) images of the fabricated CMUT. The block diagram and the photo of the acoustic transmit testing setup with the transmitter IC and the fabricated CMUT sample is shown in Fig. 10. The CMUT sample is mounted on a separate PCB and is connected to the transmitter IC through wire connection. The CMUT-mounted PCB is placed in a glass container filled with vegetable oil to mimic underwater environment, while the IC mounted board is placed outside. A hydrophone is placed at a close distance of a few millimeters from the CMUT to measure the resulting transmitted acoustic pressure and convert to a voltage signal. The external arbitrary waveform generator is again used to generate 1.8-V_{p-p} input pulse and is amplified to a 10-V_{p-p} pulse signal by the transmitter IC to drive the CMUT at the output. The CMUT converts the electrical signal to an acoustic pressure signal corresponding to the amount of applied voltage. A 10-V dc bias voltage is applied to the top electrode of the CMUT for the testing. Fig. 11 shows the

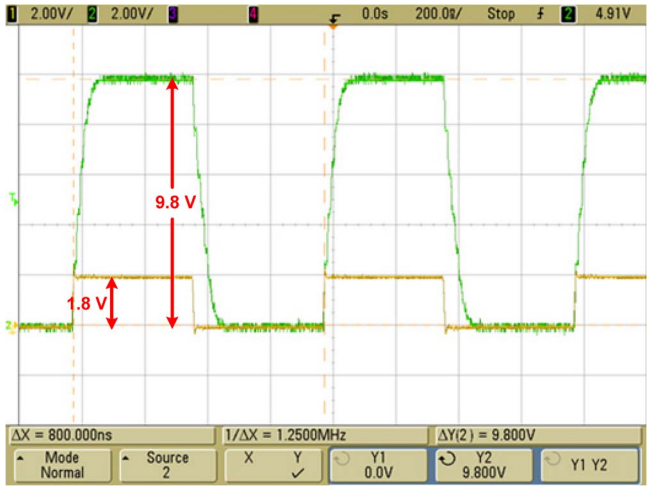


Fig. 8. Measured input trigger pulse versus HV output pulse.

TABLE I
Performance Comparison of Proposed HV Transmitter IC

Parameter	This work	[5]	[6]
Blocks	level-shifter, HV output driver	level-shifter, HV output driver	DC-DC, level-shifter , HV output driver
Input voltage	1.8 V	1.8 V	5 V
Output voltage	9.8-12.8 V	30 V	59 V
Operation frequency	1.25 MHz	35 MHz	5 MHz
Input-Output delay	22.5 ns	< 20 ns	-
Rise/Fall time	40-50 ns	< 5 ns	69/58 ns
Output load	15 pF	40 pF	20 pF
Power consumption	19.9 mA dynamic/ 0.43 mA static (simulated)	300 mA dynamic/ 28 mA static (simulated)	200 mA dynamic (simulated)
Chip area	0.022 mm^2	0.336 mm^2	4.25 mm^2
Process technology	0.18µm BCD (only CMOS used)	0.18µm BCD	0.8µm CMOS/ DMOS

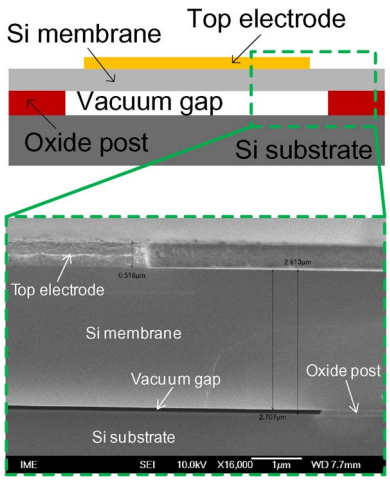
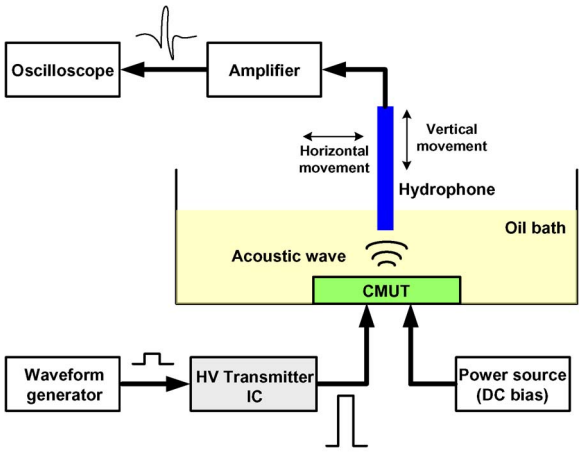


Fig. 9. (Top) Cross-sectional diagram and (bottom) SEM image of the developed CMUT sample for cotesting with the HV transmitter IC.



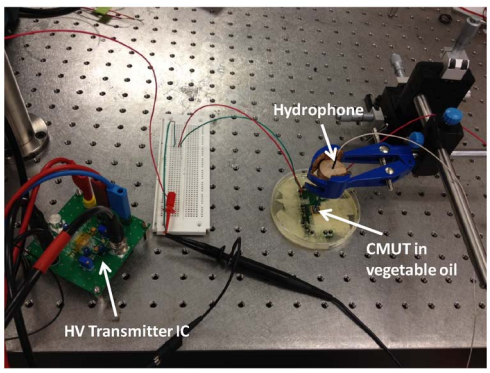


Fig. 10. Acoustic transmission testing setup for implemented transmitter IC and fabricated CMUT sample.

signal converted from the acoustic pressure to the voltage at the hydrophone output. The high amplitude signal before 5 μs in the figure is from crosstalk with the transmitted HV signal. The received voltage signal can be clearly observed after a certain delay. Additional acoustic testing with input signals of different pulsewidths and various dc bias voltages applied to the CMUT have been carried out to confirm the correct operation of the HV transmitter IC. Results demonstrate a successful operation of the HV transmitter IC consisting of stacked standard CMOS transistors for ultrasound medical imaging applications.

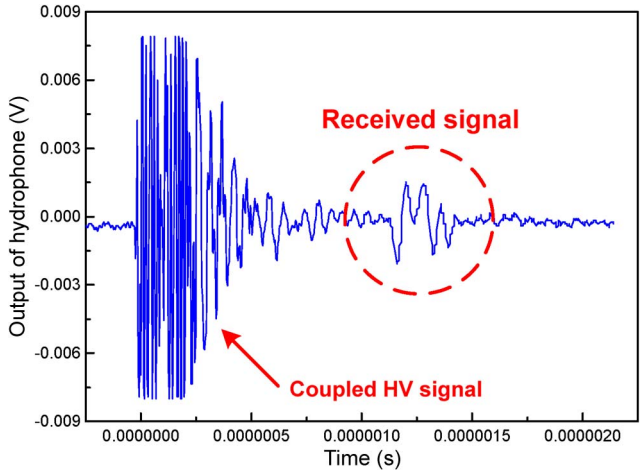


Fig. 11. Measured hydrophone output voltage signal in oil.

V. Conclusion

A HV ultrasound transmitter IC for multiarray medical imaging applications has been implemented using the HV 0.18-μm BCD process. The HV transmitter, which includes the proposed output driver and level shifter, achieves over 10-V_{p-p} output pulse signal with robust reliability while only utilizing stacked standard CMOS transistors for high integration and low cost. A successful demonstration has been done for acoustic testing in an oil environment using the proposed HV transmitter IC and the developed CMUT sample. For applications requiring a higher transmitted acoustic pressure, additional stacks can be simply added to the proposed design with dynamic bias circuits to sustain a higher voltage to excite the following transducer.

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