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A low power-delay-product and robust Isolated-DICE based SEU-tolerant latch circuit design

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ABSTRACT

Soft-error interference is a crucial design challenge in the advanced CMOS VLSI circuit designs. In this paper, we proposed a SEU Isolating DICE latch (Iso-DICE) design by combing the new proposed soft-error isolating technique and the inter-latching technique used in the DICE (Calin et al., 1996 [1]) design. To further enhance SEU-tolerance of DICE design, we keep the storage node pairs having the ability to recover the SEU fault occurring in each other pair but also avoid the storage node to be affected by each other. To mitigate the interference effect between dual storage node pairs, we use the isolation mechanism to resist high energy particle strikes instead of the original interlocking design method. Through isolating the output nodes and the internal circuit nodes, the Iso-DICE latch can possess more superior SEU-tolerance as compared with the DICE design (Calin et al., 1996 [1]). As compared with the FERST design (Fazeli, 2009 [2]) which performs with the same superior SEU-tolerance, the proposed Iso-DICE latch consumes 50% less power with only 45% of power delay product in TSMC 90 nm CMOS technology. Under 22 nm PTM model, the proposed Iso-DICE latch can also perform with 11% power delay product saving as compared with the FERST design (Fazeli, 2009 [2]) that performs with the same superior SEU-tolerance.

1. Introduction

With the progress of semiconductor process, digital circuits are becoming more susceptible to noise due to reduced working supply voltage and increased transistor density. In the advanced VLSI environment, the circuits are more easily affected by alpha particles, cosmic rays, and heat particles to cause errors, which are all summarized as soft errors [3–8]. The advancement in nano-scale CMOS technology allows increase in circuit density and improvement in performance while reducing cost. However, the enhancements in reducing transistor size and supply voltage cause decrease in the parasitic capacitance of the circuit internal node which results in the reduction of the critical charge (critical charge is the minimum charge required for maintaining the correct logic state). Consequently, the reliability of circuits against soft errors lowers and low-energy alpha particles or cosmic rays can easily cause interference in circuit internal nodes, which results in instantaneous voltage transient error [3–8].

Soft errors can be categorized into two classes according to the different locations of occurrence: (1) single event transients (SETs) which occur in combinational circuits, and (2) single event upsets (SEUs) which occur in storage elements, latches, or register nodes when the logic state of circuits changes undesirably. Due to the WOV (Windows of Vulnerability) of sequential circuits is longer than combinational circuits, sequential circuits are usually more susceptible to particle strikes than combinational circuits [9], [10]. As illustrated in Fig. 1, the SEU dominates around 90% of soft-error occurrence in modern VLSI circuits [10]. Moreover, the WOV of latch circuits is much longer than that in the flip-flop circuits. Therefore, most recent researches focus on devising robust schemes for latches. In this paper, we will further present a robust latch design that not only performs with superior soft-error resistant capability but also with lower power delay product (PDP).

In the existing literature designs, a variety of methods have been used to increase the SEU tolerance capability of latch circuits, such as: (1) interlock circuits with a redundant feedback path, such as Dual Interlocked Storage Cell (DICE) [1]; (2) strengthening equivalent capacitance for those internal nodes which have low critical charge, such as Schmitt Trigger latch (ST) [11]; (3) increasing the number of nodes to have the same electrical potential, such

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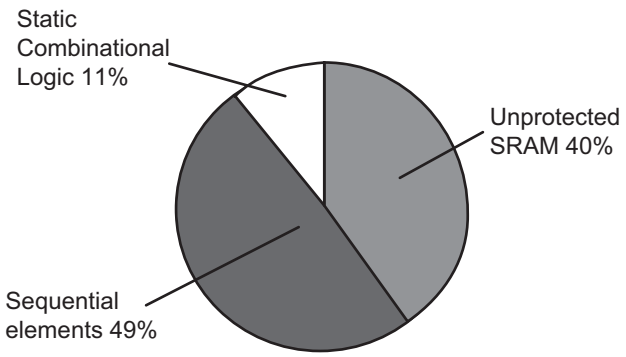

Fig. 1. Statistical analysis of soft-error occurrence distribution in modern VLSI circuits [10].

as SEU-A design [12]; (4) latches capable of filtering and masking SEUs, such as feedback redundant SEU-tolerant latch (FERST) [2]; and (5) constructing redundancy circuits together with a voting circuit to determine the valid output, such as Triple-Modular Redundancy (TMR) [13–15].

Among these SEU-tolerant approaches, DICE design can provide good SEU tolerance with less hardware cost and FERST design can provide even superior SEU-tolerance. TMR can also provide superior and nearly perfect SEU-tolerance; however, it is always criticized for its hardware complexity since it requires three times the circuit area. Therefore, in this paper we proposed a new SEU-tolerant latch that can provide superior SEU-tolerance as FERST latch but with much lower PDP.

Our proposed design is based on DICE architecture because of its advantages of simplicity. To further enhance the SEU-tolerance of DICE latch, we proposed an isolating technique which is capable of masking soft-error between DICE circuit's internal and output nodes. The proposed Iso-DICE latch can have both the DICE latch's capability of masking SEUs by cross-coupled inter-latching and the FERST latch circuit's isolation concept of having more than two storage points. Therefore, the Iso-DICE latch can have a higher SEU tolerance with a smaller power-delay-product while efficiently preventing output nodes from being affected by the SEU in the internal nodes of latch circuit.

In order to evaluate the SEU tolerant capability of each latch, some simulation experiments are carried out by means of HSPICE with TSMC 90 nm CMOS technology model, 65 nm, 45 nm, 32 nm, and 22 nm predictive technology model [33]. To confirm the consistency of comparison results, we use a variety of benchmark circuits and simulate them for particle attacks with different striking energy for performance evaluation.

The remaining concept of the paper is organized as follows. Section 2 briefly introduces the previous designs. Section 3 presents the proposed SEU-tolerant latch, describes its circuit operation, and its SEU-isolation mechanism. Section 4 demonstrates the performance comparison results. Finally, a conclusion is made in Section 5.

2. Previous works

Fig. 2 shows a convectional latch with a feedback path to keep the stored logic value. The feed forward signal transmission path is constructed of one transmission gate and two inverters. The storage feedback path is constructed of one transmission gate and one inverter. When the clk signal is '1', TG1 turns on and TG2 turns off. The input value is directly propagated from D to Q. When the clk signal is '0', TG1 turns off and TG2 turns on. Thus, the storage logic state is kept unperturbed. However, when the circuit is in latching mode, transient voltage caused by unexpected

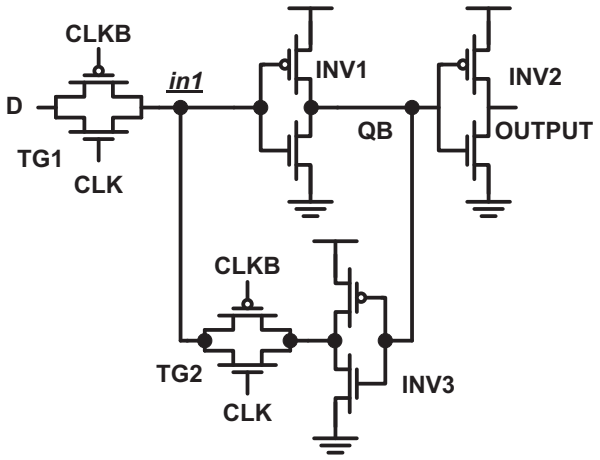

Fig. 2. Convectional latch.

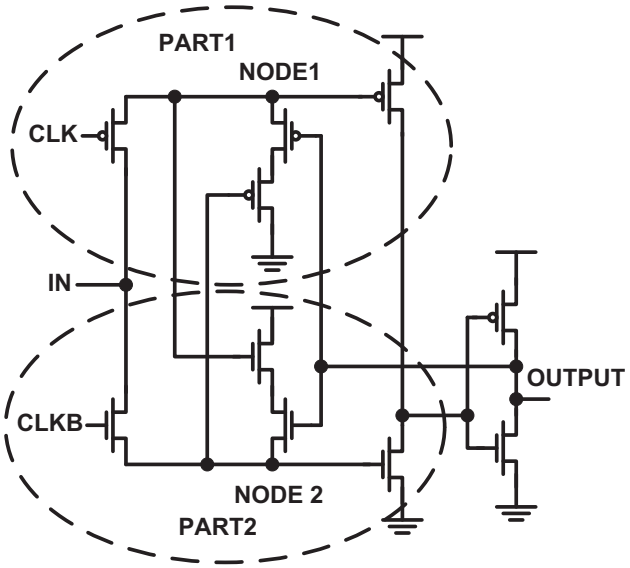

Fig. 3. SEU-A latch [12].

ionizing particles with high energy may cause a SEU. The internal node in 1 has the minimum critical charge and is the node most likely to flip. The advantage of this latch is its simplicity. However, the drawback is that it is highly susceptible to SEU.

The ST latch uses the Schmitt trigger to replace INV1 of Fig. 2 to raise the critical charge of node in 1, thus enabling the conventional latch to have a higher SEU tolerance capability with its hysteresis property. However, the drawback of the ST latch is that the use of Schmitt trigger will cause extra propagation delay and the transient voltage caused by soft-error still has the chance to cause a faulty output if the particle energy is high enough.

Alternatively, the SEU-A latch [12] enhances its capability of masking SEUs by increasing the number of nodes that have the same electrical potential. As shown in Fig. 3, the circuit can be categorized into two main parts: part 1 is constructed solely by PMOS; part 2 is constructed of only NMOS. Node 1, node 2, and the output node have identical stored value which enables them to resist a particle strike jointly. However, they can only resist SEU jointly to raise the critical charge, which still cannot avoid causing a faulty output when the particle energy is higher. Moreover, the two logic values stored in node 1 and node 2 all are weak logic with non-full swing signals, which will lead to operating speed degradation and occurrence of short circuit current.

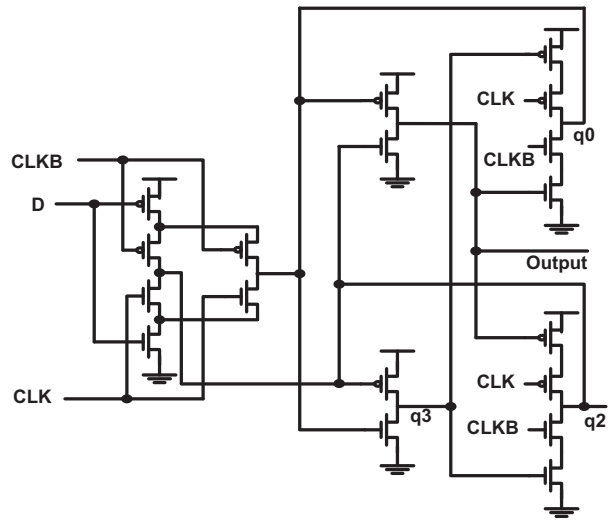

Fig. 4. DICE latch [1].

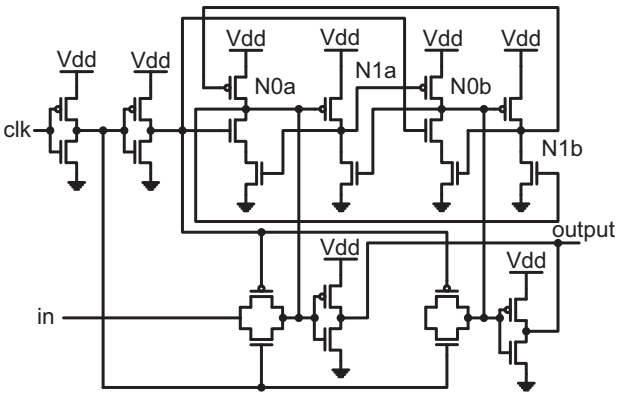

Fig. 5. Inter-DICE latch [16].

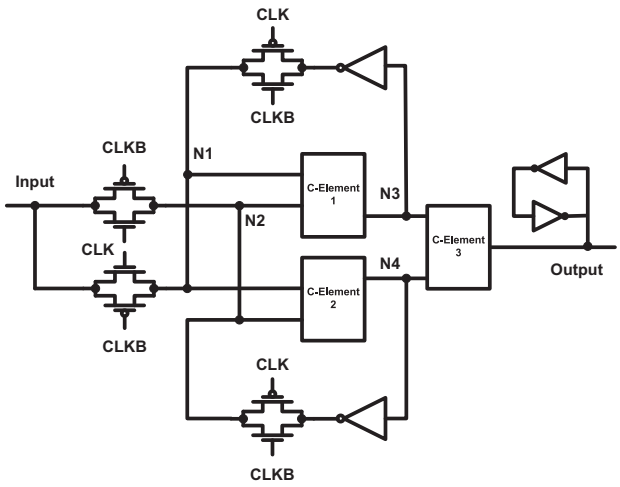

Fig. 6. FERST latch [2].

The DICE latch [1] is a well-known SEU-tolerant design because of its superior soft-error tolerance ability. When compared with other existing SEU-tolerant latch circuits for the weakest internal nodes, the DICE latch has a relatively higher critical charge during ionized particle strikes. Fig. 4 illustrates the schematic of the DICE latch. The basic structure of the DICE latch includes two cross-coupled latches, which are designed to inter-lock each other to a stable logic state. The advantage of the DICE latch is that it has two stored logic value pairs, which are stored in q0, q1, and q2, q3. When a charge particle hits any single internal node, the node can easily be recovered by the other three nodes. Therefore, DICE latch can perform with better restoring capability. Even when upset faults occur on a storage node and its complementary node (e.g. $q3{:}0\rightarrow1$; $q2{:}1\rightarrow0$), the logic values stored in the other two storage nodes ($q1=0; q0=1$) will remain correct. However, in ST and SEU-A designs, if the ionized particle carries energy which is high enough, a SEU fault may still occur.

Inter-DICE latch design [16] enhances the SEU-tolerance by duplicating the signal transmission paths, which provides even superior SEU-tolerance than the DICE latch design. As illustrated in Fig. 5, the Inter-DICE latch utilizes four nodes N0a, N1a, N0b, and N1b, to store the internal logic state of latch circuit, respectively. The input signal is transmitted through a transmission gate and an inverter respectively. The standard latch stores one bit logic value in the form of logic '1' or logic '0'. The Inter-DICE latch design stores two bit values and are coded as logic '01' or logic '10'. Suppose that the valid logic state '01' in N0a and N1a is flipped by an ionized particle and is changed to logic '11'. The logic state '11' is only a temporary state since such soft-error in N0a cannot propagate to other storage nodes of N1a, N0b, and N1b, and the internal node N1b can still be preserved as logic '1' to drain away noise charge.

Basically, both DICE and Inter-DICE designs are designed to protect the latch circuits by using dual-interlocking mechanism. Inter-DICE design duplicates the storage nodes to provide higher critical charge for each internal node of latch circuit. Therefore, Inter-DICE design can provide higher SEU-tolerance than DICE design. However, Inter-DICE design still cannot isolate the SEU interference completely since the soft-error can still propagate from N0a to output once the charge energy of the attacking ionized particle is high enough.

Fig. 6 shows the FERST design [2] which exploits three C-elements and two parallel latches to mask the propagation of soft-error faults. As shown in Fig. 7, the C-element [2], [17], [18] has a unique property where the output node updates its logic state only when the two input signals are identical. If the two inputs are different, the output remains at its previous state. The FERST circuit uses three different C-elements to isolate the SEUs. For example, the C-elements 1 and 2 are used to prevent the transient fault of node N1 and N2 to propagate to the output. C-element 3 protects the output from the transient fault that occurs in nodes N3 and N4. When a charge hits any node, FERST latch can completely mask SEUs to prevent probable SEU faults on the output signal. The advantage of FERST latch is its superior SEU-tolerance; however, its drawbacks are large power-delay-product and complicated hardware overhead.

Among the existing designs, the DICE latch can resist SEUs with lower hardware cost in terms of transistor count. However, DICE design still need to pay heavy hardware overhead to achieve superior SEU-tolerance since its transistor size should be increased to meet the demand for soft error resistance. FERST latch can provide superior SEU-tolerance. Although FERST design itself takes heavy hardware overhead in terms of transistor count, it can achieve excellent soft error resistance with much smaller transistor size because its soft error tolerance mechanism is to block the transmission of soft error in architecture level. Generally speaking, the performance overhead in terms of power-delay product in the FERST design is lower than that in the DICE design while they achieve the same superior soft-error tolerance. In this paper, we will further present a SEU-tolerant latch with the same superior SEU-tolerant ability as FERST design but performs with lower PDP, which will be discussed in detail in the next section.

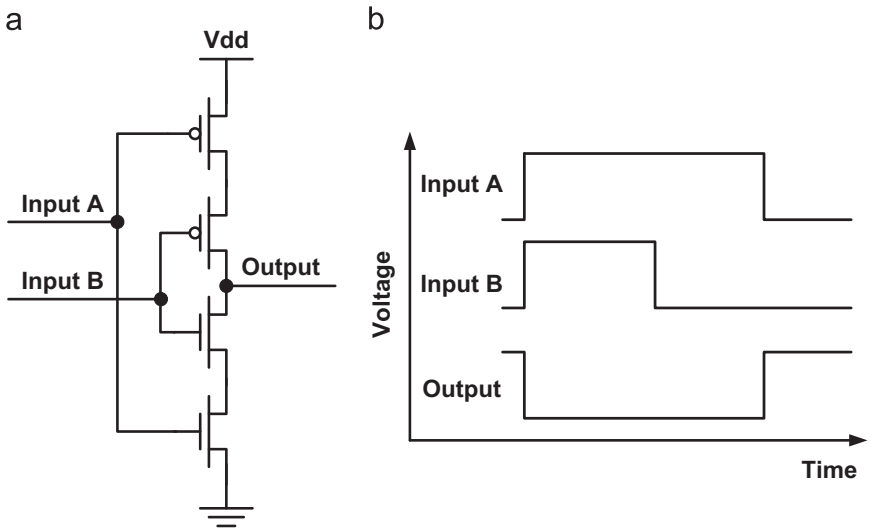

Fig. 7. (a) C-element, (b)Sample input/output of the C-element.

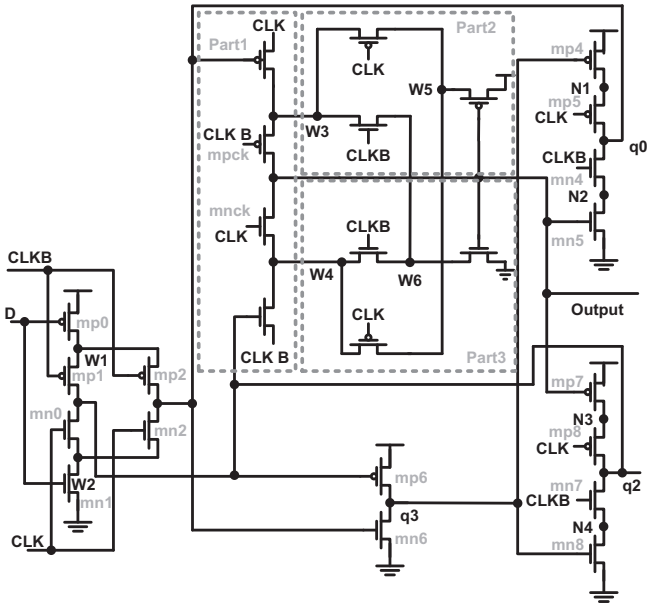

Fig. 8. The Proposed Iso-DICE latch.

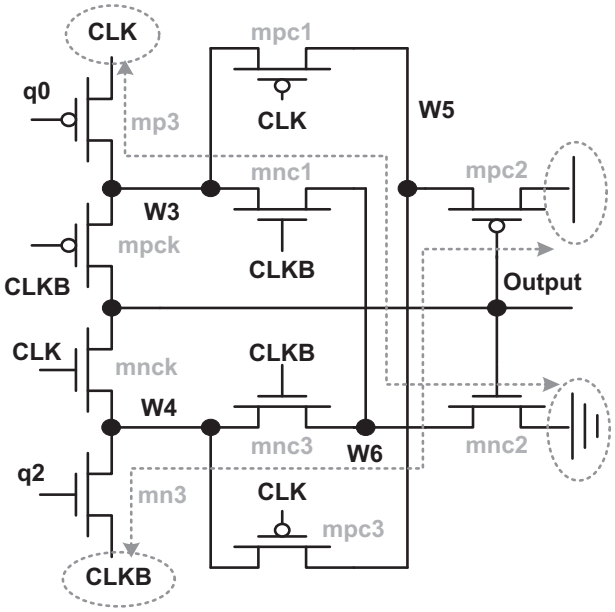

Fig. 9. The steady current path can be removed and the SEU interference can be avoided in the latching mode of the proposed Iso-DICE latch.

3. Improved SEU-tolerant latch circuit

DICE and FERST are two state-of-art literature designs. In this paper we propose a new SEU-tolerant latch design based on DICE design and further enhancing its SEU-tolerance. To further enhance the SEU-tolerance of DICE design, we must provide the storage node pairs with the ability to recover the SEU fault occurring in one another and also avoid the storage nodes to be affected by each other. To mitigate the interference effect between dual storage node pairs, we use the isolation mechanism to resist high energy particle strike instead of the original interlocking design method. The isolation mechanism is built to isolate the output node q1 apart from q0 and q2, which can cut off the signal propagation path in the latching mode to isolate SEU interference. This isolation mechanism can make the original DICE latch more robust.

As shown in Fig. 8, the proposed Iso-DICE latch is designed based on the DICE latch design and added with isolation mechanism. As illustrated in Fig. 8, it is a positive level sensitive latch and its isolation mechanism is constructed by part 1, part 2, and part 3. The two additional MOS transistors, mpck and mnck, are utilized to isolate node q1 apart from the output node to maintain its stored logic state. When CLK=0 and CLKB=1, the signal transmission paths from w3 and w4 to q1 are broken off. In this way, the logic state in the output node q1 can be protected and the impact of soft errors in the latch circuit can be suppressed.

A feedback circuit is also utilized to maintain the logic state in w3 and w4. As a result, the high impedance and the floating situation in nodes of w3 and w4 can all be avoided. In order to enhance the ability to resist soft errors and avoid the single event upset from destroying the isolation mechanism, we set the logic state of w3 and w4 to be the inverse of q1 through this feedback circuit. In the latching mode, when output q1 is at logic '1', mpc2 becomes off, mnc2 becomes on, and the nodes w3 and w4 are connected to the ground voltage level of VSS. Even when a SEU from logic '0' to logic '1' occurs in w3 and w4, the voltage of the output node is not affected. In the same way as output q1 is logic

'0' in the latching mode, mnc2 becomes off, mpc2 becomes on, and the nodes w3 and w4 are connected to the supply voltage level of VDD instead. Once a SEU from logic '1' to logic '0' occurs in w3 and w4, the voltage of the output node is not affected, too.

Moreover, in part 1 of the circuit, we connect the source terminals of mp3 and mn3 to CLK and CLKB respectively, which can prevent the latch from steady leakage during the latching mode. As illustrated in Fig. 9, in the latching mode if the logic state stored in q1 is '1', the transistors mnc2, mnc1, and mp3 all are on. The logic states of w3 and w6 all are '0', and the logic state of CLK is also '0' in the latching mode. As a result, the voltage level in the conducting path through CLK to w3 to w6 and VSS are all the same. Therefore, there will be no steady current path existing. Similarly, in the latching mode if the logic state stored in q1 is '0', the transistors mpc2, mpc3, and mn3 all are on. The logic states of w4 and w5 all are '1', and the logic state of CLKB is also '1' in the latching mode. The voltage level in the conducting path through CLKB to w4 to w5 and VDD are all the same. Therefore, there will be no steady current path existing in the situation as q1 is '0', too. So, we can successfully prevent SEU's occurring in any internal node from changing the logic state of the output node of the latch.

The operation of proposed SEU-tolerant latch can be separated into two modes: transparent mode and latching mode. As CLK is '1', the latch is in the transparent mode; when CLK is '0', the latch is in the latching mode. As shown in Fig. 8, when the latch is in the transparent mode, mp5, mp4, mp8, and mp7 are off, which can save power consumption. The input D is inverted and propagated to two storage points of q0 and q2. In the transparent mode, mpck and mnck are on, and mpc1, mnc1, mpc3, and mnc3 are off. At the same time, the redundant feedback paths of part 2 and part 3 are off and part 1 is controlled by q0 and q2. As a result, the latch output terminal q1 is the inverse of q0 and q2. Since both q0 and q2 are the inverse signals of the input D, the output signal of q1 is in the same phase as that of input signal D. In such situation, the circuit operation and its logic function is similar to the DICE latch. When the clock signal is '0', the input D is isolated by mp1, mn0, mp2, and mn2, and the latch falls into latching mode; mp5, mp4, mp8, and mp7 are on and q0, q2, and q3 are latched into a steady state. At the same time, mpck and mnck are off to isolate q0 and q2 from q1; and also mpc1, mnc1, mpc3, and mnc3 are on to activate the redundant feedback function.

Generally speaking, the function of Iso-DICE latch and DICE latch is similar in the transparent mode. However, when the latch is in its latching mode, DICE latch may suffer from soft error interference if the particle energy is high enough. As for the latching mode of the proposed Iso-DICE latch, we can still resist high energy particle strikes because we construct the isolation mechanism between q1 and q0, q2. In the proposed Iso-DICE latch design, the circuit of part1 behaves as a CLK/CLKB controlled inverter, which can isolate the output node q1 apart from q0 and q2 and protect it from being affected by faults occurring in the input node. The circuit of part 2 and part 3 are adopted to solve the floating problem of w3 and w4 and to preset the logic state of w3 and w4 to be the complementary logic state of the output terminal q1. As illustrated in Fig. 10, even when the logic state in nodes w3 and w4 is flipped by an ionized particle, a SEU just lets the logic level in nodes w3 and w4 flip into the same logic level as q1. Consequently, if any SEU occurs in the internal nodes of our proposed Iso-DICE latch, the output node q1 can always retain its stored logic value. The isolation mechanism constructed by circuits of part 1, part 2, and part 3 enables the latch's output node to have high SEU tolerance when an ionized particle hits the proposed Iso-DICE latch.

Because of the isolation property, the proposed Iso-DICE latch not only can resist single particle strike, but can also tolerate multiple soft error upsets. Moreover, the isolation mechanism in

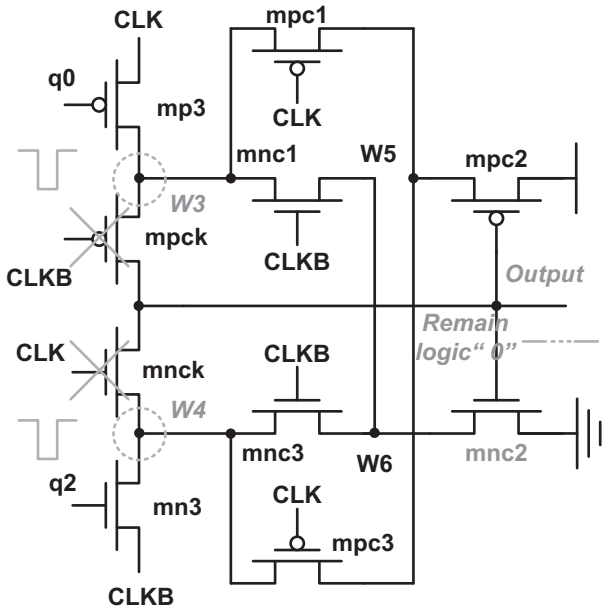

Fig. 10. Multi-SEU tolerance in the Proposed Iso-DICE latch.

the proposed Iso-DICE design is not constructed by conventional C-element. The output node in the proposed Iso-DICE latch is only wired to two drain/source connected transistors, where their gate terminals are controlled by robust CLK and CLKB signals, respectively. Therefore, the proposed Iso-DICE latch can tolerate multiple node soft-error upsets with arbitrary combinations. In the previous popular used C-element based soft-error isolation designs, they cannot tolerate two soft-errors occur at the same time on both C-element input nodes. The proposed Iso-DICE design can avoid such issue and tolerate multiple soft-errors occurring at the same time. When multiple particle strikes occur in the Iso-DICE latch, it is capable of preventing faults of the surrounding internal nodes to propagate to the output node q1 by turning-off the transistors mpck and mnck. Therefore, the output terminal can be reliable and the stored logic value would not be affected by multiple SEUs. Even though the DICE latch and the FERST latch are robust against single particle strike and have partial multiple nodes SEU-tolerant ability to tolerate a subset of multiple nodes upsets; however, faults may still occur in the output when particle strikes occur in more than one internal node in some cases. As illustrated in Fig. 11, an output fault will occur as SEU occurs in both q0 and q2 at the same time of the DICE latch. An output fault will also occur as SEU occurs in both nodes N1 and N2 or both nodes N3 and N4 at the same time of the FERST latch. However, the proposed Iso-DICE latch can mitigate multiple SEUs to ensure the correctness of output logic state, even if SEU occurs in both the internal nodes of w3 and w4 at the same time.

In addition to providing superior SEU-tolerant ability, the proposed Iso-DICE latch can perform with lower PDP. The key reason to achieve such superior property is the adoption of isolation mechanism. In terms of power consumption comparison, the DICE latch, the FERST latch, and the Iso-DICE latch all have no static power consumption. The FERST latch has a greater number of switching transistors corresponding to the input transition and it also consumes larger short circuit power. However, the DICE latch and the Iso-DICE latch cut down the probable short circuit leakage current path by turning-off mp5, mn4, mp6, and mn7 when the clock signal is '1'. Thus the DICE latch and the proposed Iso-DICE latch are able to consume lower dynamic power and lower short circuit power than the FERST latch. In regard of circuit operation delay time in the latch circuits, the difference comes

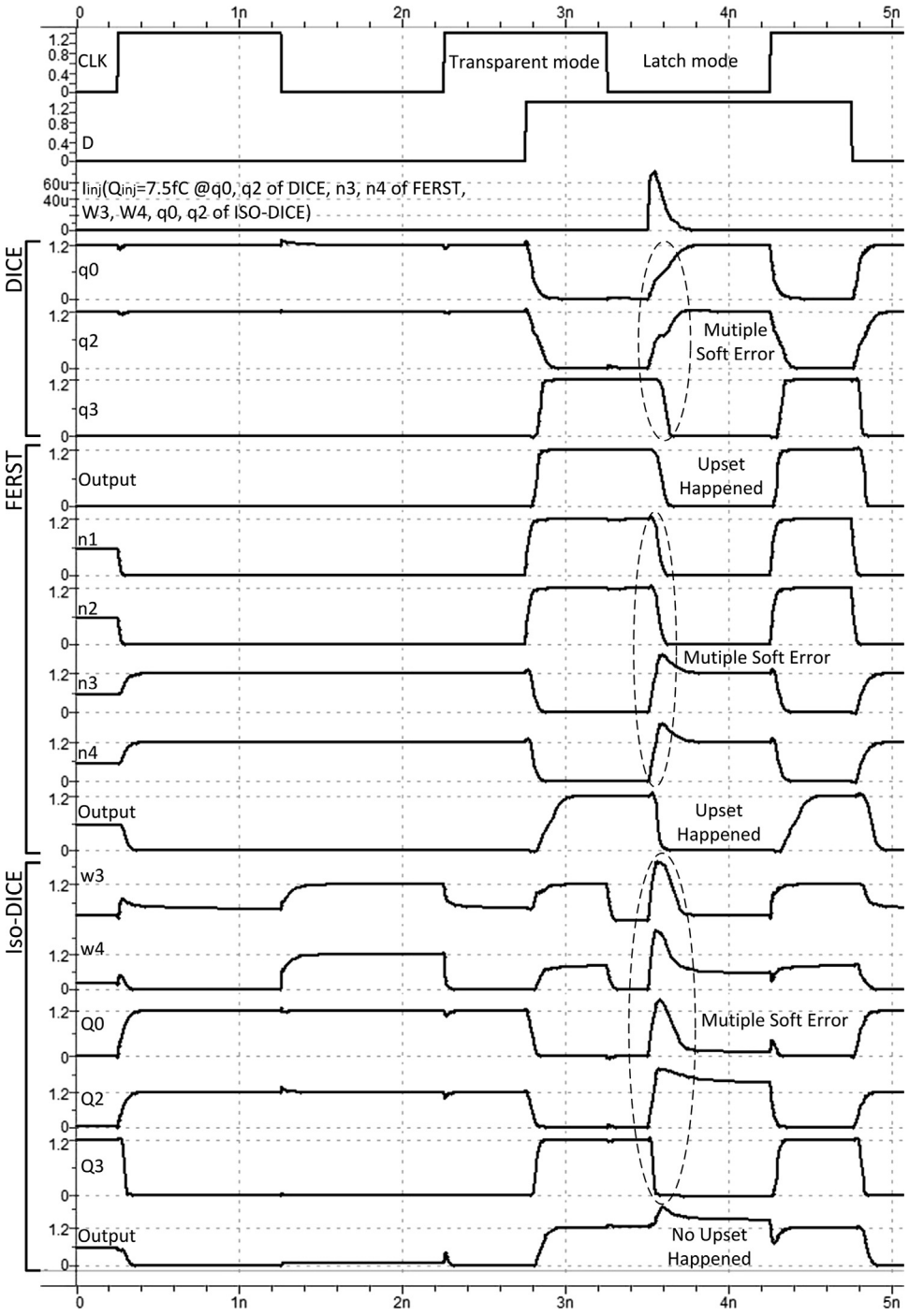

Fig. 11. Testing results for Multi-SEUs in various latch designs.

because of signal transition stages and the number of cascaded MOS transistors causing the FERST latch to have a longer delay time than that of the DICE latch. The proposed Iso-DICE latch also has longer delay time compared with the DICE latch due to the extra added MOS transistors applied to isolate soft errors. However, the proposed Iso-DICE design can resist SEU interference through isolation mechanism, which need not increase the transistors' size to raise their critical charge. Therefore, under the same situation with superior SEU-tolerance, our proposed Iso-DICE design can perform with lowest PDP as compared with the state-of-art of DICE [1] and FERST [2] designs.

4. Simulations and experimental results

In the paper, we analyze and evaluate the soft error tolerance of latches in three ways. First, we assess the ability of a latch to protect itself against the SEUs. We utilize a controllable current source to model a particle strike in the latch circuit [1], [11], [19], [20]. The SEU-tolerant ability of each node of latch circuit is evaluated by calculating the critical charge of each internal node. Monte Carlo simulation, invoking the law of large numbers, is then used to compare the SEU immunity among different types of latches by counting the probability of a bit flip in the latch because

of a particle strike in the node. Second, we apply these latch circuits on a variety of benchmark circuits and evaluate their soft error rate (SER) improvements individually. Third, we evaluate the soft error tolerance of DICE latch, FERST latch, and the proposed Iso-DICE latch while encountering parameter variations, SEU occurring under various timing, and multiple nodes soft error upsets.

According to [7], [21], SER can be evaluated from the following equation:

$$SER \propto N_{flux} \times CS \times e^{(-Q_{critical}/Q_s)} \quad (1)$$

where N_{flux} denotes the total neutron flux, CS is the area of cross section of a node, Q_s is the charge collection efficiency of a particle strike on the device (depends strongly on doping profile) and $Q_{critical}$ is the critical charge, which is proportional to the power supply voltage and cross section node capacitance. Eq. (1) shows that SER is exponentially dependent on Q_{critical}, which is a key factor to influence the soft error immunity of internal nodes. A soft error occurs if the energy of striking particle exceeds the critical charge of a circuit internal node. Hence, we first analyze the SEU-tolerant ability of different latch circuits by analyzing the critical charge of each internal node and infer the most susceptible node in each design. Soft error tolerance of individual latch circuits is quantitatively evaluated and compared by applying statistical Monte Carlo analysis method. Further, we analyze the SER reduction in a practical system by utilizing various latch circuits on different benchmark circuits.

All these analysis approaches use critical charge as a key evaluation basis to measure or compare the soft error immunity of each internal node, each latch circuit, and SER improvement in each benchmark circuit. The critical charge required for a soft-error induced upset of each internal node can be figured out from the following equation:

$$I_{inj}(t) = \frac{Q_{coll}}{\tau_\alpha - \tau_\beta}(e^{-t/\tau_\alpha} - e^{-t/\tau_\beta}) \quad (2)$$

where $I_{inj}(t)$ is the current induced as α-particle hits on the diffusion region and can be modeled as a double exponential current pulse [22], Q_{coll} represents the striking particle charge, τ_α represents the collection time-constant of the junction, and τ_β accounts for the ion-track establishment time constant. In literatures [9], [23], τ_α and τ_β were chosen 164 ps and 50 ps based on the experience presented in [24]. However, these values will shrink as fabrication technologies scale down [25]. Therefore, we take τ_α and τ_β with 50 ps and 15 ps respectively depending on the trend predicted in [25] to make it much closer to the case in ultra-deep submicron semiconductor technology. Adopting the method proposed in [25], we incorporate the pulsed current source to model the current response $I_{inj}(t)$ resulting from collision of α-particles at each node under test. When the injected current charge is high enough to cause a flip of logic level in the output of latch circuit, which results in the output voltage varies over one-half the VDD supply, the injected upset charge Q_{coll} is then defined as critical charge Q_{crit}. Repeating the same experiment and calculation procedure, we can measure the critical charge of all circuit nodes. During the simulation procedure, the latches included an inverter at the output, where its PMOS is twice the minimum size and its NMOS is of minimum size, for fan-out consideration.

We capsule the critical charge analysis results for each latch internal node under TSMC 90 nm CMOS technology process in Table 1. If the internal node is robust enough and the output logic state is not affected by a particle strike even in the case of high charge energy, the critical charge of such node is marked as "∞". The critical charge analysis results show that all critical charge quantities are raised obviously while the soft-error-tolerant mechanism is constructed in latch circuits. The critical charge quantity of all the internal nodes in FERST and Iso-DICE designs is approaching infinity, and the critical charge quantity of half of the nodes in Inter-DICE design is also near infinity. FERST and Iso-DICE can perform with superior SEU immunity since the isolation mechanism is constructed to isolate the interference in the internal nodes away from the output node, which can help the output maintain its stored logic state. As for the Inter-DICE design, it can also resist the influence of α-particles with excellent resilience. However, there is no isolating mechanism between output node and internal nodes in the Inter-DICE design. Hence, the critical charge of only half of the internal nodes can approach infinity. In contrast with the traditional latch, the critical charge in the internal nodes and SEU-tolerant ability of the Inter-DICE latch can certainly be enhanced significantly. However, as compared to FERST and Iso-DICE such kinds of soft-error masking design, Inter-DICE inherently cannot provide the same excellent critical charge performance.

Table 1
Critical charge, area weighting and POF of the internal nodes for each latch under TSMC 90 nm CMOS technology process.

Convectional	node	Qb		nq	
	w	0.10		0.20	
	Qcirt	6.50		5.10	
	E	71%		78%	
DICE	node	Q0	Q2	Q3	
	w	0.05	0.10	0.10	
	Qcirt	→∞	15.20	18.30	
	E	0%	23%	7%	
Inter-DICE	node	N0a	N0b	N1a	N1b
	w	0.10	0.10	0.10	0.10
	Qcirt	32.80	32.70	→∞	→∞
	E	0%	0%	0%	0%
FERST	node	N1	N2	N3	N4
	w	0.08	0.08	0.04	0.04
	Qcirt	→∞	→∞	→∞	→→∞
	E	0%	0%	0%	0%
ISODICE	node	Q0	Q2	Q3	
	w	0.08	0.08	0.04	
	Qcirt	→∞	→∞	→∞	
	E	0%	0%	0%	

Table 2
POF and POF improvement of the SEU-tolerant latches performed by using Monte Carol analysis under TSMC 90 nm CMOS technology process.

	Conventional %	**DICE %**	**FERST %**	**Inter-DICE %**	**Iso-DICE %**
POF	22.7	3.35	0	0	0
POF improvement	–	**85.00**	**100.00**	**100.00**	**100.00**

The Monte Carlo analysis results for various latch circuits are shown in Table 2. The purpose of Monte Carlo simulation is to compare and quantify the soft error tolerance ability of each latch. Through Monte Carlo simulation, each circuit is simulated 100 times for ionized particle strike in each internal storage node. By taking the statistic results of flip times into the Eq. (2), we can obtain the Probability of Failure (POF) of each latch, where POF is widely used to evaluate the average soft error occurrence probability of each latch [26].

$$POF = \sum_{i=1}^{n} w_i E_i \quad (3)$$

$$w_i = \frac{\text{Area}_i}{\text{Area}_{\text{total}}}, \quad E_i = \frac{\text{numberofflips}}{\text{numberofinjections}} \times 100\% \quad (4)$$

As shown in Eq. (3), the definition of POF is the summation of logic state flip probability in each node times by its area weighting [2]. Here w_i is the occupied diffusion area weighting by the node i, where Area_i is the occupied silicon area of each internal node and $\text{Area}_{\text{total}}$ is the total area of latch circuitry. E_i represents the probability of a bit flips in the latch because of a particle strike in the node i.

In conventional CMOS circuits, it needs 100fC [27] charge energy to cause an output logic level flip. However, in advanced nano-scale CMOS technology process, the critical charge of a storage cell of SRAM under the 90 nm CMOS process is about 1.46fC [8]. In general, the critical charge is significantly lowered in the advanced VLSI design and all the circuit nodes are much more susceptible to soft-error. In order to evaluate the SEU immunity of each latch circuit and distinguish the soft-error tolerance performance of each latch, we first set each injected particle charge to be ranged from 1fC to 20fC with uniform distribution based on the experience and suggestion from literature [28], [29]. To distinguish whether there is a soft-error occurring, we have to check whether the injected particle charge quantity is larger than the critical charge of each internal node or not. If the injected particle charge is larger than the critical charge, a logic level flip will occur in such internal node and the logic level of latch circuit output terminal will also flip. If the injected particle charge is smaller than the critical charge, the particle cannot cause a logic level flip and the latch output can be maintained as its original stored logic state. The higher critical charge in each internal node means the better soft error tolerance ability it has.

The POF analysis results point out that Iso-DICE and FERST both have superior SEU-tolerance and excellent POF improvements. The main reason is that both their internal storage nodes are under well protection and the soft-error propagation paths are properly isolated. FERST uses C-element to get the superior soft-error isolation, and Iso-DICE constructs dual interlocked storage cell with isolation mechanism to achieve excellent soft-error isolation. Under proper isolation between the internal nodes to the output node, when the ionizing particle hits internal nodes of Iso-DICE and FERST, it certainly will not cause a logic level flip in the latch circuit output, which makes the critical charge quantity of internal storage nodes approach infinity. Therefore, the logic state flip probability E_i of each internal node is 0%.

As for DICE and Inter-DICE designs, even though they all have the protection mechanisms against soft error by using cross-coupled interlocking. However, the interlocking mechanism may still be ruined if the ionizing particles striking the circuit have higher charge energy. The interlocking mechanism does not have perfect soft-error isolation ability. Once the interlocking mechanism is destroyed, a soft-error caused by ionized particle will be transferred through the signaling pathway to output terminal, which will lead to logic flip in the latch output node and cause a transient malfunction. The critical charge of each internal node in DICE and Inter-DICE latch is shown in Table 1. Only the critical charge of one internal node (Q3) in DICE latch can be near infinity. The other internal nodes still have a chance to be attacked by charged particles and result in soft error. As for the Inter-DICE design, there are also two nodes (N1a and N1b) whose critical charge can achieve near infinity. The other internal nodes in Inter-DICE may also still have a chance to be attacked by ionizing particles. However, the critical charge in N0a and N0b of Inter-DICE latch is higher than that in Q2 and Q3 of DICE design. Moreover, the critical charge in N0a and N0b is higher than 20fC. Therefore, Inter-DICE latch circuit can also perform with 100% POF improvement to totally eliminate the occurrence of SEU as the ionizing charge energy is lower than 20fC, just like FERST and Iso-DICE design. However, DICE latch can only lower POF to 3.35% and perform with 85% POF improvement as compared with the conventional latch design. It cannot totally eliminate the influence caused from SEU.

After critical charge and POF analysis, we further go to analyze the Soft-Error-Rate (SER) and SER improvement of each latch circuit, which includes the analysis of SER of the latch itself and SER of the whole benchmark system while applying each latch circuit in it. Then we further analyze the improvement range of SER of the benchmark circuit systems in each latch circuit design. The SER analysis basis can be referenced to the literature [30], [31] and the definition of SER can be expressed as

$$SER = \sum_{i=1}^{n} \frac{WOV_i}{T_{CK}} k_i \frac{\alpha}{\beta} e^{-\beta Q_{crit}(i)} \tag{5}$$

where WOV is window-of-vulnerability and stands for the possible window interval during which the latch circuit may be influenced by soft error [32]. T_{CK} is the period of operation clock signal, k_i is the area weighting for each internal node, α and β are process fitting parameters [7]. According to (5), we can also compare the SER improvement between the latches with SEU protection and the traditional unprotected latches. The SER improvement can be computed by following the definition of

$$\text{SER improvement}\% = \frac{\text{SER}_{\text{conventional}} - \text{SER}_{\text{compared}}}{\text{SER}_{\text{conventional}}} \times 100\% \tag{6}$$

During the procedure of computing SER improvement%, there exists a dividing relation between the latch circuit under comparison and the conventional unprotected latch. Some common terms in SER, such as WOV/Tck and α/β, can be eliminated and SER can be simplified to R, which can be expressed as:

$$R = \sum_{i=1}^{n} k_i e^{-\beta Q_{crit}(i)} \tag{7}$$

Here k_i is the internal node's area weighting. The definition of k_i is expressed in (8), which is the same meaning as reference [29] to define W_i in POF. They all stand for the area percentage of each occupied node as compared with the overall area of the latch circuit.

$$k_i = \frac{A_i}{A_{\text{total}}} = w_i \tag{8}$$

By replacing SER with R, SER improvement% defined in Eq. (5) can be re-written as Eq. (9), which can provide us a great convenience during the computation process.

$$\text{SER improvement}\% = \frac{R_{\text{conventional}} - R_{\text{compared}}}{R_{\text{conventional}}} \times 100\% \tag{9}$$

According to the definition of SER improvement% in Eq. (9), we can bring the critical charge Q_{cirt} for each internal node and node's area weighting k_i into Eqs. (8) and (9) to obtain SER improvement percentage of various SEU-tolerant latches. Due to the fact that the exponential factor dominates the performance of SER as defined in Eq. (5), the presence of vulnerable nodes in a latch circuit will become the key that SER cannot continue to be reduced no matter in the latch circuit itself or in the benchmark system. We summarize the SER analysis results of each latch circuit in Table 3.

The soft error tolerance rate analysis of each latch circuit is according to the critical charge for each internal node and summing up all of them based on their corresponding node area weighting. Thereby, the probability of soft-error occurrence of each internal node of latch circuit is evaluated by its critical charge directly, not only to limit the amount of the charge induced by the attacking particles from 1fC to 20fC. In other words, SER or R-value analysis is a more rigorous evaluation index to test the soft-error resistance ability in a latch circuitry as compared to the POF index performed by Monte Carlo simulation. Consequently, the R-value analysis values illustrated in Table 3 are all smaller or equal to the analysis results of POF in Table 2. Especially if there are fragile

nodes, which are more susceptible to soft-error interference, in latch circuit, the difference between these two analyses will be more obvious. We usually take the analysis result of R-value as the worst-case consideration of soft-error tolerance. As the critical charge of internal nodes in FERST and Iso-DICE latches is approaching to infinite, the R-value computational results in the formula (7) will be approximately zero. When compared for R-improvement of FERST and Iso-DICE with that of the conventional unprotected latches, they both have a superior enhancement in SER.

On the contrary, as there are still some fragile nodes existing in the DICE and Inter-DICE latches, their output logical value may still have the chance to be flipped in the case of high energy charged particle strikes. Therefore, they cannot reach the same superior R-improvement as the FERST and Iso-DICE designs. The key factor why their SER value is not reaching the case of ideal SEU-tolerance is because DICE and the Inter-DICE latch cannot completely isolate all soft-error signal propagation paths, so that the critical charge immunity of some of their internal nodes cannot reach near infinity.

Finally, we perform the soft error analysis by utilizing various latch circuits in ISCAS'85 benchmarks. The latch circuits under test are connected to every primary input and primary output of the benchmark circuit. For instance, if the benchmark circuit includes five inputs and five outputs, then 10 latches are required in the entire benchmark system. The corresponding number of each benchmark's inputs and outputs are summarized in Table 4. We apply Eq. (5) to evaluate SER improvements for various latches utilized in different benchmarks. The SER comparison results are capsuled in Table 5 and the SER improvement results are summarized in Table 6. As compared Table 3 with Table 6, we can find out that SER improvement is less effective while applying DICE and Inter-DICE latches in the benchmark circuits. The main reason for the degradation of SER improvement is the increase in the latch area. The area of latch circuit also plays an important role as critical charge in SER mitigation. When we enhance the SEU tolerant ability of a latch by raising its critical charge resistance ability, we usually also increase the circuit complexity and area occupied by the latch. Once the area is increased, the probability for a latch to be struck by a particle is raised and its area weight k_i is raised, too. SER is proportional to the area weight k_i; therefore, the SER improvements would certainly degrade somewhat accordingly. The comparison results for various benchmark circuits are slightly different due to the diversity of the area of the benchmark circuits and the number of latches utilized in the circuits. Table 4 describes the area and corresponding input and output port number of various benchmark circuits.

In the SER or R-value analysis procedure for evaluating a single latch itself, only area weight of each node is considered and the area weight is normalized to the total area of a latch. The SER or R-value analysis results are dominated by the critical charge Q_{cirt} of each node, especially the susceptible node with weak SEU resistance. In the SER analysis procedure for evaluating the SEU-tolerant ability by utilizing various latches in benchmark circuits, area weight k_i of each latch is considered and the area weight is normalized by the total area of each benchmark circuit. Therefore, the SER analysis results in benchmark circuits are not only dominated by the critical charge Q_{cirt} of each latch circuit, but also affected by the size of latch area. The comparison and evaluation results of Tables 3 and 6 may vary due to the consideration of different applications and different area weight; however, the trends and the ranking order for the comparison results in Table 6 are still the same as the evaluation results in Table 3. Both FERST and Iso-DICE latches can perform with superior SEU-tolerant ability in the benchmark testing under soft-error attacking. However, Iso-DICE can perform with lower PDP than FERST does.

Besides soft error mitigation, we also evaluate and compare how much hardware overhead and performance sacrifice we must pay to obtain the enhancement of soft error immunity in various latch circuits. In this paper, performance comparison and analysis

Table 3
SER analysis and SER improvement of the SEU-tolerant latches evaluated by SER equation under TSMC 90 nm CMOS.

	Conventional %	DICE %	FERST %	Inter-DICE %	Iso-DICE %
R	0.201	0.06	0.00	0.02	0.00
SER improvement	–	**70.00**	**100.00**	**90.00**	**100.00**

Table 4
Parameters of ISCAS'85 benchmarks.

Benchmark	Input	Output	Area
c432	36	7	2208
c499	41	32	3396
c880	60	26	5388
c1355	41	32	5236
c1908	33	25	9191
c2670	233	140	16601
c3540	50	22	25611
c5315	178	123	35682
c6288	32	32	46336
c7552	207	108	45466

Table 5
SER analysis results of various SEU-tolerant latch designs applied in ISCAS'85 benchmarks under TSMC 90 nm CMOS technology process.

R in ISCAS'85					
Benchmark	**convectional**	**FERST**	**DICE**	**Inter-DICE**	**Iso-DICE**
c432	8.01E−02	0.00	2.48E−02	1.10E−02	0.00
c499	8.56E−02	0.00	2.60E−02	1.15E−02	0.00
c880	6.96E−02	0.00	2.24E−02	9.90E−03	0.00
c1355	6.30E−02	0.00	2.08E−02	9.18E−03	0.00
c1908	3.31E−02	0.00	1.23E−02	5.39E−03	0.00
c2670	8.81E−02	0.00	2.65E−02	1.18E−02	0.00
c3540	1.59E−02	0.00	6.37E−03	2.78E−03	0.00
c5315	4.23E−02	0.00	1.51E−02	6.66E−03	0.00
c6288	8.07E−03	0.00	3.36E−03	1.46E−03	0.00
c7552	3.58E−02	0.00	1.32E−02	5.78E−03	0.00
avg.	**5.22E−02**	**0.00**	**1.71E−02**	**7.54E−03**	**0.00**

Table 6
The SER improvement of various SEU-tolerant latch designs in ISCAS'85 benchmarks under TSMC 90 nm CMOS technology process.

SER improvement in ISCAS'85				
Benchmark	**FERST (%)**	**DICE (%)**	**Inter-DICE (%)**	**Iso-DICE (%)**
c432	100.00	69.06	86.28	100.00
c499	100.00	69.65	86.53	100.00
c880	100.00	67.86	85.78	100.00
c1355	100.00	67.06	85.44	100.00
c1908	100.00	62.84	83.69	100.00
c2670	100.00	69.91	86.65	100.00
c3540	100.00	59.90	82.48	100.00
c5315	100.00	64.26	84.28	100.00
c6288	100.00	58.40	81.87	100.00
c7552	100.00	63.28	83.87	100.00
avg.	**100.00**	**65.22**	**84.69**	**100.00**

results for various latch circuits are performed by using the HSPICE simulator in TSMC 90 nm CMOS process, and predictive technology model (PTM) in the advanced CMOS technology processes for 32 nm and 22 nm CMOS process [33]. The power supply voltage is 1.2 V and the clock frequency is 500 MHz for the TSMC 90 nm CMOS process environment. The power supply voltage is 1 V and the clock frequency is 500 MHz under various PTM models. The performance comparison results for transistor count, power, delay, and power-delay product under TSMC 90 nm CMOS technology process and various PTM models are collected in Table 7.

As illustrated in Table 7, DICE has the fewest transistors while the transistor number of Iso-DICE latch is close to that of FERST latch due to construction of isolation mechanism. Both Iso-DICE and FERST overcame soft error interference by using isolation or mask mechanism to combat striking particle in architecture level; therefore, they can be implemented by choosing the transistors with nearly minimal size. Under TSMC 90 nm CMOS technology process, the power consumption of Iso-DICE and FERST latch design can be lower than that of a DICE latch. However, FERST latch consumes larger power than that of Iso-DICE latch. It is mainly because the FERST consumes a large amount of short circuit power in each output of C-element cell during its input signal transition. In contrast, there is no short circuit path existing in the Iso-DICE latch. Therefore, despite of using approximately equal transistor count, the proposed Iso-DICE consumes only around half power dissipation as compared with the FERST latch. There was no existing mechanism to resist soft errors in the DICE latch. As for the DICE latch, there is no isolation mechanism to cut or mask the soft-error propagation path to combat SEU interference. Hence, we must realize the DICE latch with larger transistor size to raise the critical charge of each internal node. But larger transistor size results in larger power dissipation, where the power consumption in the DICE design is nearly twice of a FERST latch.

As for the comparison of operating delay of latches, due to more complications in the isolation mechanism resulting in more cascaded MOS transistors on the critical transmission path, the delay time of Iso-DICE latch is about 1.55 times as compared with that of DICE latch. Because of more transmission stage between input and output terminal, the operating delay of the FERST design is longer about 10% as compared with that of Iso-DICE latch. To compare power consumption together with operating delay time, the proposed Iso-DICE latch can lower 59.74% PDP as compared with the DICE latch and lower 54.77% PDP as compared with the FERST latch design.

Under PTM models, the proposed Iso-DICE latch design also performs with the lowest PDP as compared with the DICE latch and the FERST latch design. It is noted that DICE latch design can provide larger driving capability than that of FERST and the proposed Iso-DICE design. Therefore, the difference between DICE design and the other two designs is closer. However, the power consumption difference between DICE design and the other two designs is larger. In respect of SEU-tolerance, the proposed Iso-DICE latch design can perform with competable soft-error tolerance as compared with the FERST latch design under single particle attack environment. Iso-DICE and FERST design can still both perform with more superior soft-error tolerance than that of DICE latch design. Although the critical charge of DICE latch lowers from 15.2fC to 10.9fC and 7.8fC respectively for the 22 nm and the 32 nm CMOS PTM model, the critical charge of conventional latch also lowers. Therefore, the SER improvement in the DICE latch can still be maintained as 74.00% and 69.88% respectively under 32 nm and 22 nm CMOS PTM model environment.

As compared with the DICE latch under 22 nm and 32 nm PTM model, PDP in the proposed Iso-DICE latch design can be lowered by 79.66% and 69.57% respectively while the proposed Iso-DICE latch design also performs with more superior SEU-tolerance. As compared with the FERST latch under 22 nm and 32 nm PTM model, PDP in the proposed Iso-DICE latch design can be saved by 10.99% and 19.21% respectively while the proposed Iso-DICE latch design can perform with competable SEU-tolerance.

Finally, we summarize the performance comparison in terms of power, delay, power-delay-product, SER improvement in latch

Table 7
The key performance comparison results for various SEU-tolerant latches.

Latch types	DICE	FERST	Proposed Iso-DICE
Number of MOS	18	28	26
Technology	TSMC 90 nm CMOS process		
Critical charge (fC)	15.2	$\gg 100$	$\gg 100$
SER improvement	70.00%	100%	100%
Multiple nodes SEU-tolerant ability	Partial (q0, q2 upset at the same time is not tolerable.)	Partial (N1, N2 or N3, N4 upset at the same time is not tolerable)	Complete
Power(uW)	35.82	18.60	9.30
Rising delay(pS)	73.69	149.24	124.02
Falling delay(pS)	78.18	111.61	111.24
Average delay(pS)	75.94	130.24	117.82
PDP(fS*J)	2.720	2.423	1.096
Power delay product (%)		89.08%	40.26%
Technology	32 nm CMOS PTM model		
Critical charge (fC)	10.9	$\gg 100$	$\gg 100$
SER improvement	74.00%	100%	100%
Power(uW)	2.385	0.631	0.596
Average delay(pS)	22.61	32.19	27.48
PDP(fS*J)	0.0539	0.0203	0.0164
Power delay product (%)		37.66%	30.43%
Technology	22 nm CMOS PTM model		
Critical charge (fC)	7.8	$\gg 100$	$\gg 100$
SER improvement	69.88%	100%	100%
Multiple nodes SEU-tolerant ability	Partial (q0, q2 upset at the same time is not tolerable.)	Partial (N1, N2 or N3, N4 upset at the same time is not tolerable)	Complete
Power(uW)	1.307	0.303	0.318
Average delay(pS)	21.80	31.25	26.49
PDP(fS*J)	0.0285	0.0095	0.0084
Power delay product (%)		33.19%	29.54%

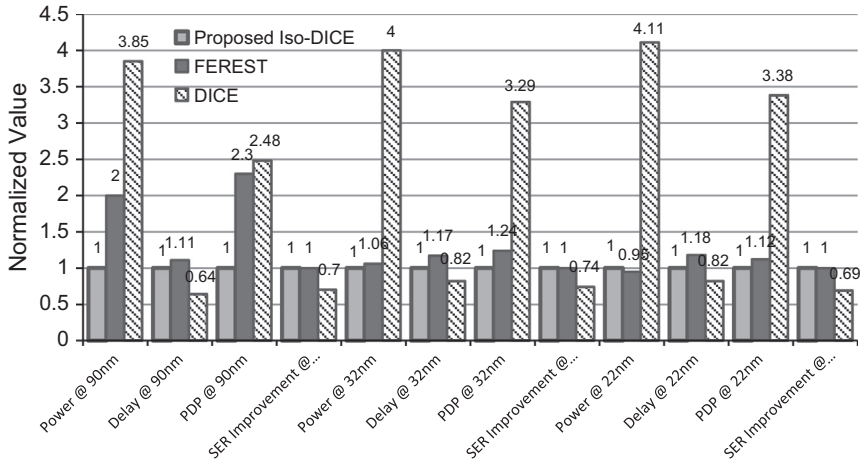

Fig. 12. Various performance indexes comparison results in different latch circuits.

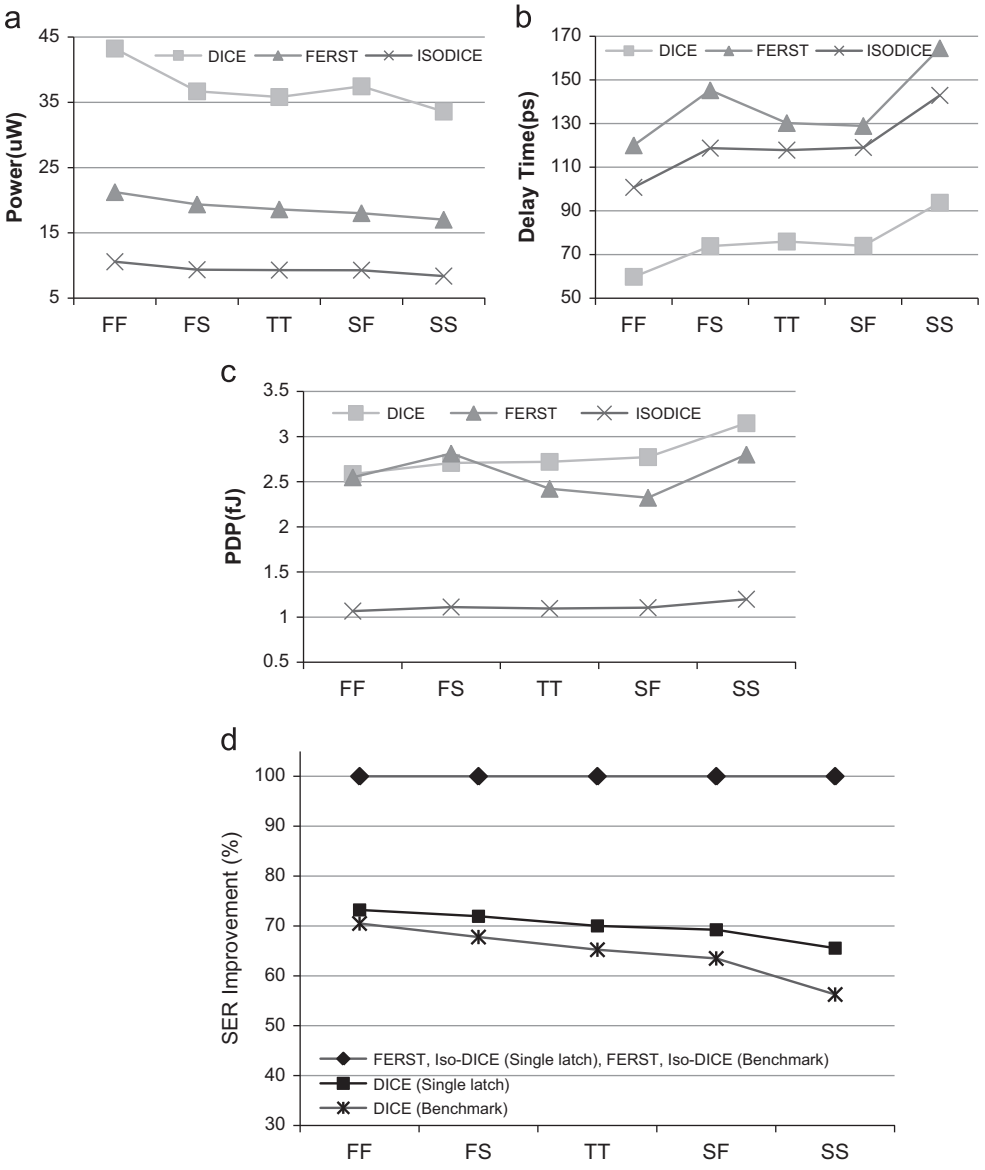

Fig. 13. Performance comparison results under various design corners. (a) power consumption, (b) operation delay, (c) power-delay-product, (d) SER improvement under various design corners under TSMC 90 nm CMOS technology process.

itself, and SER improvement as applying the latch circuits in the benchmark circuits in Fig. 12. As illustrated, the Iso-DICE latch we proposed in the paper not only performs with the same superior SEU-immunity against soft errors as FERST design, but also performs with lowest PDP, which behaves as a superior robust latch circuit candidate in the advanced VLSI designs. Moreover, our proposed Iso-DICE latch also demonstrates excellent SEU-tolerant ability in the benchmark circuits.

To further verify the process, voltage, temperature, and parameter variation effects, we demonstrate the performance comparison results under various design corners, which include typical–typical (TT), fast–fast (FF), slow–slow (SS), fast–slow (FS), and slow–fast (SF) corners. As illustrated in Fig. 13, the performance difference in terms of power, delay, and PDP are all within 25% drift limit. Pros and cons of various latch designs are still sorted in a consistent sequence as their typical–typical situation. As for the performance difference in terms of SER improvement, the FERST and the proposed Iso-DICE latch can still maintain their SER improvement as 100% while the SER improvement drift difference in the DICE latch is around 10%. It is because that the soft-error is isolated through transmission path interruption in architecture level in the FERST and the proposed Iso-DICE designs. The process and parameter variations would not affect the SER improvement performance in these two designs.

To evaluate how different soft-error occurring time impacts the SEU-tolerant ability of various latches, we inject the soft-error charge at any time of the whole clock duration period to evaluate their SER improvement respectively. Here a whole latching window is set as 1000ps. As illustrated in Fig. 14, the SER improvement is maintained unchanged in almost the entire clock cycle in the three latch designs. The SER improvement is maintained as 100% in both FERST and the proposed Iso-DICE latch designs in the whole latching window. Only when soft-error attacks the critical node of DICE latch circuit near the end of clock period that the charged particles do not have enough time to destroy the inter-latching mechanism, the SER improvement would increase in the DICE latch.

To evaluate the multi-node soft-error upsets effects in each latch design, a transistor level simulation method has been presented by Vanderbilt University [34]. It is to evaluate the charge required to be deposited on the most critical nodes and the secondary critical node in order to cause the storage cell to upset. We adopt the same approach to evaluate the multi-node soft-error upsets effects among DICE latch, FERST latch, and the proposed Iso-DICE latch. The maximum soft-error attack charge is simulated with 200fC. As illustrated in Fig. 15, the attacked particle energy with any combination of charge which lies below the curve will not cause a soft-error upset. The evaluation results show that the proposed Iso-DICE latch can resist multi-node soft-error upsets because of soft-error isolation mechanism. In most cases, FERST latch and DICE latch can also resist multi-node soft-error upsets because of c-element isolation mechanism and inter-latching mechanism. However, once soft-error attack both inputs of c-element at the same time, multi-node soft-error upsets will occur in the FERST latch. Once soft-error attack both nodes q0 and q2 of DICE latch at the same time, multi-node soft-error upsets will also occur in the DICE latch. Generally speaking, the critical charge curve for the FERST latch can still lies above that of the DICE latch design since C-element is a serial-connected architecture in both of its pull-up network and pull-down network while q0 and q2 are connected to the gate terminal of power/ground connected transistors. Consequently, the proposed Iso-DICE latch can provide a higher level of soft-error robustness as compared with the FERST latch and the FERST latch can provide the more superior soft-error robustness as compared with the DICE latch. As a conclusion, only the proposed Iso-DICE latch design can provide complete multiple nodes SEU-tolerant ability. Both FERST and DICE latches can provide partial multiple nodes SEU-tolerant ability, which can only tolerate a subset of multiple nodes upsets.

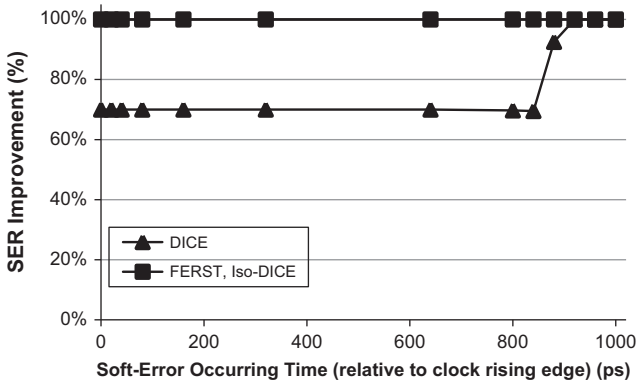

Fig. 14. SER improvement performance comparison results under various soft-error occurring time.

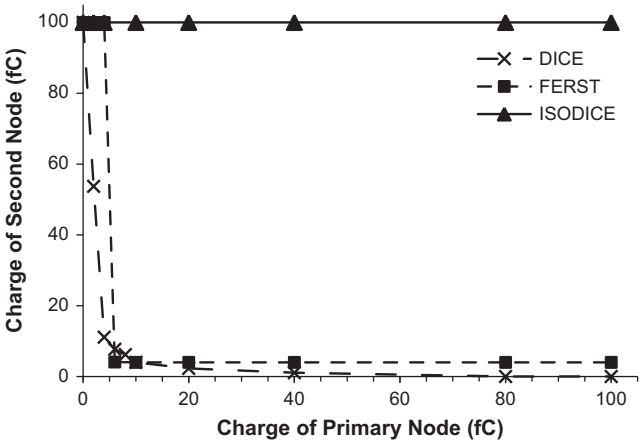

Fig. 15. Critical charge performance comparison results under soft-error attacking on multiple circuitry internal nodes.

5. Conclusion

In this paper, we proposed a robust SEU-tolerant latch design, which performs with lower PDP. Under TSMC 90 nm CMOS technology, experiment results show that both the Iso-DICE latch and the FERST latch have the capability of fully masking output faults caused by transient voltage in the internal nodes. However, the FERST latch consumes more energy and performs with larger PDP. Comparatively, the proposed Iso-DICE latch can perform with the same superior SEU-immunity against soft errors as FERST design, but performs with 55% lower PDP than FERST latch in TSMC 90 nm CMOS technology. Under 22 nm PTM model, the proposed Iso-DICE latch can also perform with 11% lower PDP. As a result, the proposed Iso-DICE latch can provide both characteristics of low PDP and high capability of masking SEUs. Moreover, the proposed Iso-DICE latch can tolerate multiple nodes soft-error upsets.

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References

[1] T. Calin, M. Nicolaids, R. Velazco, Upset hardened memory design for submicron CMOS technology, IEEE Transactions on Nuclear Science 43 (6) (1996) 2874–2878.

[2] M. Fazeli, S.G. Miremadi, A. Ejlali, A. Patooghy, Low energy single event upset/single event transient-tolerant latch for deep subMicron technologies, IET, Computers & Digital Techniques 3 (2009) 289–303.

[3] N. Miskov-Zivanov, and D. Marculescu, A systematic approach to modeling and analysis of transient faults in logic circuits, in: Proceedings of Quality of Electronic Design, pp. 408–413, 2009.

[4] S. Gangadhar, M. Skoufis, and S. Tragoudas, Propagation of transients along sensitizable paths, in: Proceedings of Fourteenth IEEE International On-Line Testing Symposium, pp. 129–134, 2008.

[5] P. Shivakumar, M. Kistler, S.W. Keckler, D. Burger, and L. Alvisi, Modeling the effect of technology trends on the soft error rate of combinational logic, in: Proceedings of the International Conference on Dependable Systems and Networks, pp. 389–398, 2002.

[6] R.C. Baumann, Radiation-induced soft-errors in advanced semiconductor technologies, IEEE Transactions on Device and Materials Reliability 5 (3) (2005) 305–316.

[7] P. Hazucha, C. Svensson, Impact of CMOS technology scaling on the atmospheric neutron soft error rate, IEEE Transactions on Nuclear Science 47 (2000) 2586–2594.

[8] E. Ibe, H. Taniguchi, Y. Yahagi, K. Shimbo, T. Toba, Impact of scaling on neutron-induced soft error in SRAMs from a 250 nm to a 22 nm design rule, IEEE Transactions on Electron Devices 57 (2010) 1527–1538.

[9] M. Omana, D. Rossi, C. Metra, Latch susceptibility to transient faults and new hardening approach, IEEE Transactions on Computers 56 (9) (2007) 1255–1268.

[10] S. Mitra, R. Iyer, K. Ravishankar, K. Trivedi, and J.W. Tschanz, Reliable system design: models, metrics and design techniques, in: Proceedings of IEEE/ACM International Conference on Computer-Aided Design, pp. xi, 2008.

[11] S. Lin, Y.B. Kim, and F. Lombardi, Soft-error hardening designs of nanoscale CMOS latches, in: IEEE VLSI Test Symposium, 2009. pp. 41–46, May. 2009.

[12] L. Wang, S. Yue, and Y. Zhao, Low-overhead SEU-tolerant latches, in: Microwave and Millimeter Wave Technology, International Conference on 18–21 pp.1–4, April. 2007.

[13] F.L. Kastensmidt, L. Sterpone, L. Carro and M.S. Reorda, On the optimal design of triple modular redundancy logic for SRAM-based FPGAs, in: Proceedings of. Design, Automation and Test in Europe, 2005. Vol. 2, pp. 1290–1295.

[14] M. Favalli, C. Metra, TMR voting in the presence of crosstalk faults at the voter inputs, IEEE Transactions on Reliability Vol. 53 (Sept. 2004) 342–348.

[15] L. Sterpone, M. Violante, Analysis of the robustness of the TMR architecture in SRAM-based FPGAs, IEEE Transactions Nuclear Science 52 (Oct. 2005) 1545–1549.

[16] P. Hazucha, T. Karnik, S. Walstra, B. Bloechell, J. Tschanzl, J. Maiz, K. Soumyanath, G. Demer, S. Narendra, V. De, S. Borkar, Measurements and analysis of SER tolerant latch in a 90-nm Dual-Vt CMOS process, in: IEEE Custom Integrated Circuits Conference, 2003, pp. 617–620.

[17] M. Omana, D. Rossi, C. Metra, Latch susceptibility to transient faults and new hardening approach, IEEE Transactions on Computer 56 (2007) 1255–1268. (Sept.).

[18] Y. Shao and S. Dey, Separate dual-transistor registers: a circuit solution for on-line testing of transient error in UDMC-IC, in: On-Line Testing Symposium, pp. 7–11, July. 2003.

[19] D.R. Blum, J.G. Delgado-Frias, Delay and energy analysis of SEU and SET-tolerant pipeline latches and flip-flops, IEEE Transactions Nuclear Science 56 (June. 2009) 1618–1628.

[20] D. Giot, P. Roche, G. Gasiot, R. Harboe-Sorensen, Multiple-bit upset analysis in 90 nm SRAMs: heavy ions testing and 3D simulations, IEEE Transactions Nuclear Science 54 (Aug. 2007) 904–911.

[21] R. Ramanarayanan, V. Degalahal, N. Vijaykrishnan, M.J. Irwin and D. Duarte, Analysis of soft error rate in flip-flops and scannable latches, SOC Conference, in: Proceedings of IEEE International SoC Conference, pp. 231–234, Sept. 2003.

[22] G.C. Messenger, Collection of charge on junction nodes from ion tracks, IEEE Transactions on Nuclear Science NS-29 (6) (1982) 2024–2031. (Dec.).

[23] M. Omana, D. Rossi, C. Metra, High-performance robust latches, IEEE Transactions on Computers 59 (11) (2010) 1455–1465.

[24] H. Cha and J.H. Patel, A logic-level model for α-particle hits in CMOS circuits, in: Proceedings of Twelfth IEEE International Conference Computer Design (ICCD'93), pp. 538–542, 1993.

[25] R. Garg, S.P. Khatri, Analysis and Design of Resilient VLSI Circuits Mitigating Soft Errors and Process Variations, Springer, USA, 2009.

[26] M. Singh, R. Rachala, I. Koren, Transient fault sensitivity analysis of analog-to-digital converters (ADC's), in: Proceedings of IEEE Annual Workshop on VLSI, April 2001, pp. 140–145.

[27] S.E. Skutnik, A scalable analytic model for single event upsets in radiation-hardened field programmable gate arrays in the PHENIX interaction region (Master's thesis), Iowa State University, Ames, IA, March 2005 [Online]. Available: ⟨http://shepody.physics.iastate.edu/skutnik/thesis.pdf⟩.

[28] K.M. Warren, A. Sternberg, R. Weller, L. Massengill, R. Reed, R. Schrimpf, M. Baze, Integrating circuit level simulation and Monte Carlo radiation transport code for single event upset analysis in SEU hardened circuitry, IEEE Transactions on Nuclear Science 55 (6) (2008) 2886–2894. (Dec.).

[29] Q. Zhou, M.R. Choudhury, and K. Mohanram, Tunable transient filters for soft error rate reduction in combinational circuits, in: Proceedings of Thirteenth European Test Symposium (ETS), pp. 179–184, 2008.

[30] P. Hazucha, C. Svensson, S.A. Wender, Cosmic-ray soft error rate characterization of a standard 0.6-μm CMOS process, IEEE Journal of Solid-State Circuits 35 (10) (2000) 1422–1429.

[31] N. Seifert, X. Zhu, D. Moyer, R. Mueller, R. Hokinson, N. Leland, M. Shade, and L. Massengill, Frequency dependence of soft error rates for sub-micron CMOS technologies, in: Proceedings of Technical Digest IEEE International Electron Devices Meeting, pp.14.4.1–14.4.4, 2001.

[32] N. Seifert, X. Zhu, L.W. Massengill, Impact of scaling on soft-error rates in commercial microprocessors, IEEE Transactions on Nuclear Science 49 (6) (2002) 3100–3106.

[33] ⟨http://ptm.asu.edu/⟩.

[34] D. Rennie, D. Li, M. Sachdev, B.L. Bhuva, S. Jagannathan, S.J. Wen, R. Wong, Performance, metastability, and soft-error robustness trade-offs for flip-flops in 40 nm CMOS, IEEE Transactions on Circuits and Systems-I 59 (8) (2012) 1626–1634. (Aug.).