Design of Schmitt Trigger Logic Gates Using DTMOS for Enhanced Electromagnetic Immunity of Subthreshold Circuits

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***Abstract*—This paper presents subthreshold digital circuit design and optimization method using Schmitt trigger logic gates for enhanced electromagnetic immunity. The proposed Schmitt trigger logic gates are based on a buffer design using dynamic threshold-voltage MOS for low-power operation. By expanding the Schmitt trigger to NAND/NOR gate, we can dramatically improve the noise immunity with much lower switching power consumption and significant area reduction compared with CMOS Schmitt triggers, at the expense of a slight increase in delay. Not only for the gate level, but also the circuit level immunity improvement is verified with ISCAS 85 benchmark. In addition, we propose a parameter to determine the optimal noise immunity considering the trade-off between immunity and performance. By using the proposed parameter, optimal hysteresis can be chosen for the reasonable performance deterioration.**

***Index Terms*—Digital circuits, electromagnetic interference (EMI), hysteresis, immunity, Schmitt trigger.**

I. Introduction

DUE to the growing demand for longer battery life in mobile devices, mobile integrated circuit (IC) designers have focused on reducing the power consumption of circuits, especially for supply voltage scaling. As a result, the supply voltage has been greatly reduced, and subthreshold circuits have been developed.

However, lowering the supply voltage simultaneously degrades the noise immunity of the circuit [1]–[2]. Since the threshold voltages have not scaled as aggressively as the supply voltage, the static noise margin of digital circuits has continuously decreased. Therefore, the signal itself is more vulnerable for the external noise and the immunity to electromagnetic interference (EMI) has become an important issue for IC designers, and several solutions have been proposed [3]–[12].

A Schmitt trigger is one such solution that can be appropriately used to enhance the noise immunity of a circuit at the expense of delay and power consumption [13]–[14]. Unlike comparator circuits, the switching threshold of the Schmitt trigger depends on the direction of input signal transition, a phenomenon known as *hysteresis*. In the presence of hysteresis, the threshold voltage of the Schmitt trigger is higher than that of comparators for positive transitions and lower for negative transitions. If the amplitude of the input signal variation is less than the switching threshold difference, the output of the Schmitt trigger will not respond directly to input. This makes the Schmitt trigger immune to undesired electromagnetically coupled noise.

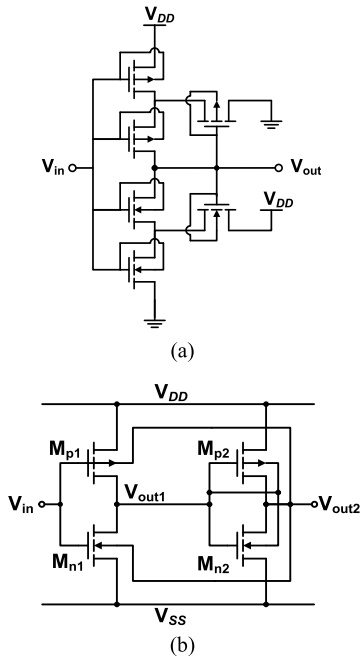

Fig. 1. (a) Traditional Schmitt trigger inverter. (b) VTCMOS Schmitt trigger inverter in [8].

Several approaches can be used to implement Schmitt trigger circuits suitable for low-power design [15]. Since traditional CMOS Schmitt trigger circuits require too many extra transistors for practical implementation, the dynamic threshold voltage MOS (DTMOS) design using a reduced number of transistors was introduced, as shown in Fig. 1 [8]. DTMOS design was applied to improve the EMI susceptibility in operational amplifier circuits [9]. However, previous researches on low-power Schmitt trigger circuits have focused only on extra buffer insertion between adjacent logic gates or threshold voltage control for improvement of noise immunity [16]–[17]. Although these methods do enhance noise immunity, they also require extra power consumption, which is not suitable for a low-power design [19].

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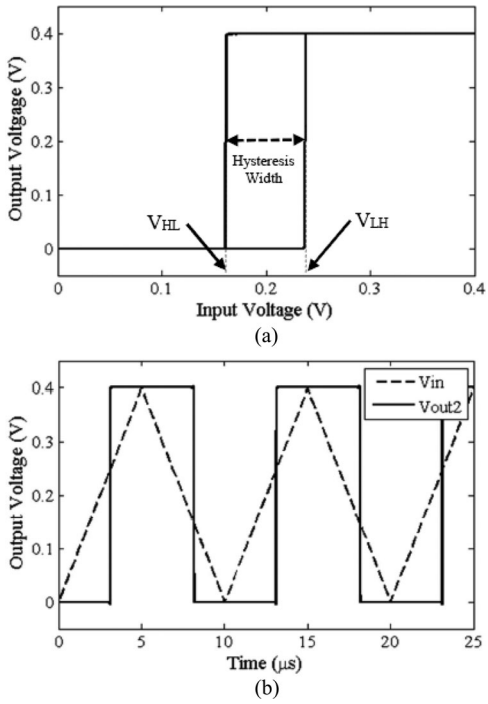

Fig. 2. (a) Voltage transfer characteristic of a Schmitt trigger buffer. (b) Input and output waveforms of a Schmitt trigger buffer.

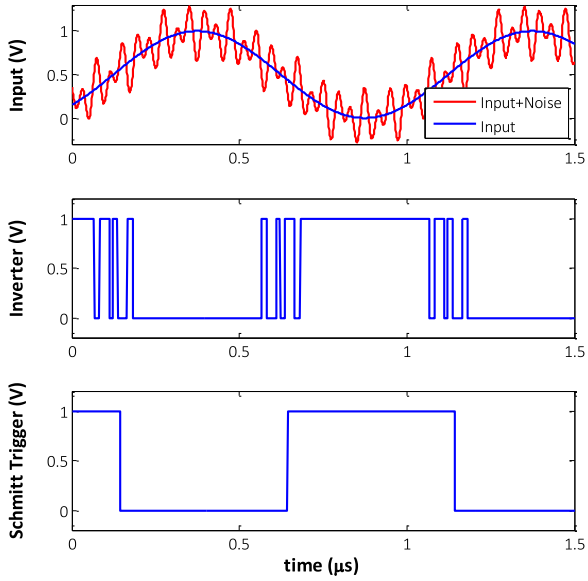

Fig. 3. Noise immunity enhancement achieved by using a Schmitt trigger.

In this study, we expanded the DTMOS buffer insertion method by merging the extra Schmitt trigger buffer with logic gates to improve the noise immunity for various types of low-power logic gate designs that use fewer transistors. The schematic designs of the Schmitt trigger logic gates are described in Section II, from basic buffer implication to multi-input logic gates with dc characteristics. Section III presents the performance and noise immunity simulation results of the proposed gate and the effectiveness of the proposed circuits with the noise immunity and performance of ISCAS benchmark circuits. The simulations are performed using Cadence Spectre circuit simulator using SAMSUNG 130 nm process information [23]. In Section IV, we discuss the limitation of the proposed DTMOS gates and present an optimization study of the noise immunity and performance with adjustable hysteresis. The conclusions are presented in Section VI.

II. Implementation of DTMOS Schmitt Trigger Gates

A. Noise Immunity Improvement Using a Schmitt Trigger

Schmitt trigger circuits are well known for their hysteresis and are utilized as an effective solution for noise immunity enhancement. Depending on the direction of a signal transition, the switching threshold voltage of the Schmitt trigger is separated into $V_{\rm LH}$ (for the low to high transition) and $V_{\rm HL}$(for the high to low transition), as shown in Fig. 2. Therefore, the actual output transition level deviates from $V_{\rm DD}/2$, allowing the Schmitt trigger to maintain its output when large-amplitude noise is injected into its input node, as shown in Fig. 3.

The traditional design schematic of the Schmitt trigger, shown in Fig. 1(a), can implement hysteresis by using an extra current path that resists the signal transition of the output node through the use of current feedback. In this case, extra power consumption is unavoidable when enhancing the noise immunity because the feedback circuit produces extra current in order to maintain the output in the presence of a noisy input signal. Therefore, the traditional design method for the Schmitt trigger is not suitable for low-power designs.

In contrast, the schematic of Fig. 1(b) shows the use of a voltage feedback path from the output of the second stage to the substrate of the first-stage inverter for hysteresis implementation. In this way, there is no extra current requirement to secure the stability of the output, which is more appropriate for low-power design. In addition, the inverter output $V_{\rm out1}$ and the buffer output $V_{\rm out2}$ can be merged into one logic gate.

According to [5], the threshold voltage of the DTMOS must be lowered below the supply voltage to ensure the operation of the transistor in the saturation region because the supply voltage is near the normal threshold voltage value ($\cong 0.4\,\rm V$). To lower the threshold voltage, the gate and substrate are tied together to generate a forward body bias condition at the body-to-source junction. Utilizing the body effect with negative source-to-body bias condition, this method can decrease the threshold voltage.

However, the substrate bias of the first-stage inverter, shown in Fig. 1(b), is connected to $V_{\rm OUT2}$ and is independent of its input node. Therefore, the threshold voltage of the first stage varies according to the value of $V_{\rm OUT2}$; this design is called variable threshold voltage CMOS (VTCMOS). Since each transistor in the first stage is set to a zero-body bias condition for the output transition, the turn-on voltage of each transistor is higher for the case shown in Fig. 1(b) than it is for normal DTMOS. According to [8], the switching threshold voltage can be described with the following equations:

$$V_{\rm LH} = \frac{V_{\rm DD} - |V_{{\rm th},p}| + \zeta \times V_{{\rm th0},n}}{\zeta + 1} \tag{1}$$

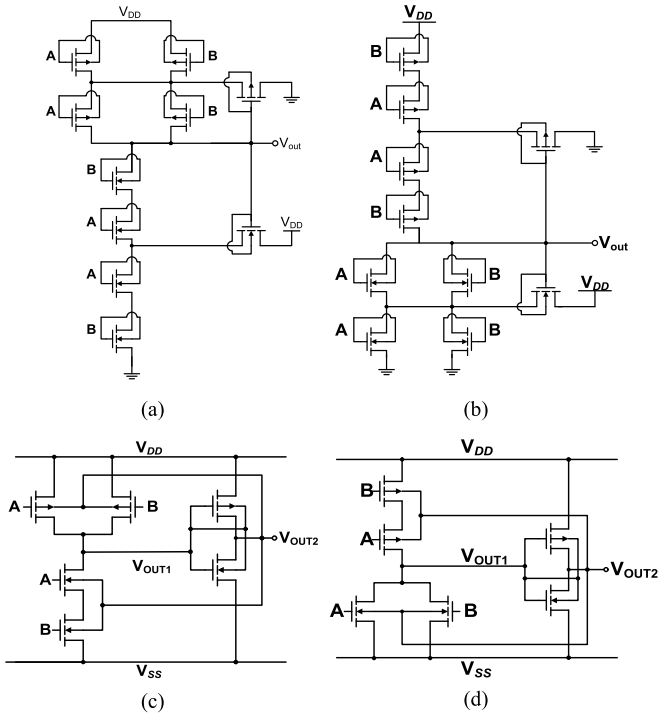

Fig. 4. (a) Traditional Schmitt trigger AND gate. (b) Traditional Schmitt trigger OR gate. (c) Proposed Schmitt trigger AND gate. (d) Proposed Schmitt trigger OR gate.

$$V_{\mathrm{HL}} = \frac{V_{\mathrm{DD}} + \zeta \times V_{\mathrm{th},n} - |V_{\mathrm{th0},p}|}{\zeta + 1} \tag{2}$$

where $V_{\mathrm{th},p(n)}$ is the threshold voltage of the PMOS (NMOS) for the forward bias condition; $V_{\mathrm{th0},p(n)}$ is the threshold voltage of the zero-bias condition, $\zeta = \sqrt{(\beta_n/\beta_p)}$; and β_n and $\beta_p$are the transconductance parameters of NMOS and PMOS, respectively.

B. AND and OR Gate Construction

Expanding the scheme shown in Fig. 1(b), we can modify the AND gate and OR gate to operate as Schmitt triggers, as shown in Fig. 4. Similar to the buffer case, V_{out1}, shown in Fig. 4(c) and (d), can be utilized as the inverted outputs NAND and NOR, respectively. As shown in–Fig. 4, the proposed design scheme uses four fewer transistors for inverting logic compared to the traditional scheme. Since the proposed Schmitt trigger logic gates also use the voltage feedback from V_{OUT2}, they require less switching current consumption.

The basic operation of these AND and OR gates is similar to that in the buffer case. However, the value of *R* in (1) and (2) must be adjusted as appropriate. If the output is changed by only one input transition, the situation is the same as in the buffer case. However, when both input transitions experience a changed output value, the two PMOS transistors and the two NMOS transistors in the first stage are turned on and off at the same time, as if they were one large transistor. Therefore, the two transistors in series can be modeled as a single transistor with a doubled channel length, and two parallel transistors can be replaced by a transistor with a doubled channel width. Therefore, we can derive the effective value of ζ in (1) and (2) for the case of a Schmitt trigger AND gate with $\beta_p' = 2\beta_p$ and $\beta_n' = \beta_n/2$ as

$$\zeta' = \sqrt{\beta_p'/\beta_n'} = 2\zeta.$$

We can also derive the effective value of R for the case of a Schmitt trigger OR gate with width $\beta_p'' = \beta_p/2$ and $\beta_n'' = 2\beta_n$ from the following equation:

$$\zeta' = \sqrt{\beta_p''/\beta_n''} = \zeta/2. \tag{3}$$

III. Noise Immunity Improvement of DTMOS Schmitt Trigger Gates

A. Simulation Setup

For the schematic implementation, we designed a unit DTMOS inverter with $w_p = 0.7$ μm and $w_n = 1$ μm. Based on this geometric information, we designed the proposed logic gates and traditional Schmitt triggers. For the immunity analysis, we defined the failure condition for the output of the logic gate as a variation of more than 40 mV (10% of V_{DD}) under the noise injection condition. The simulations are performed using Cadence Spectre circuit simulator using SAMSUNG 130 nm process information [23].

B. Gate-Level Immunity Enhancement

1) Schmitt Trigger Buffer (Inverter): Fig. 5 shows the dc transfer characteristic comparison results of a buffer for different process corners. To guarantee logical equivalence, we connected the traditional Schmitt trigger inverter with the normal DTMOS inverter to construct a buffer scheme. Therefore, the traditional Schmitt trigger requires an additional inverter to construct a buffer, requiring eight transistors in total. By employing the VTCMOS scheme, however, the number of transistors needed to construct a buffer was halved, as shown in the Table I. In addition, due to the higher V_{TH} for the zero substrate bias condition, the VTCMOS scheme reduced switching current from 1.277 mA to 310.92 μA (about 75% reduction) at the expense of a slight increase in delay compared to that of the traditional Schmitt trigger. The high current consumption of the traditional scheme is due to the additional current injection path through its feedback loop in the first stage.

As shown in Fig. 5, the hysteresis width of the VTCMOS scheme is greater than that of the traditional Schmitt trigger except for the fast corner simulation. Although the difference in hysteresis width is small, it improves the noise immunity of the Schmitt trigger buffer, as shown in Fig. 6.

2) Schmitt Trigger AND (NAND) Gate/OR (NOR) Gate: Figs. 7 and 9 show the dc characteristics of the Schmitt trigger AND and OR gates implemented using the proposed VTCMOS scheme. Similar to the buffer scheme, we added a DTMOS inverter to the traditional Schmitt trigger for logical equivalence with the VTCMOS scheme. Detailed performance comparison parameters are shown in Tables II and III. Using the proposed scheme, we reduced more than 50% of the switching

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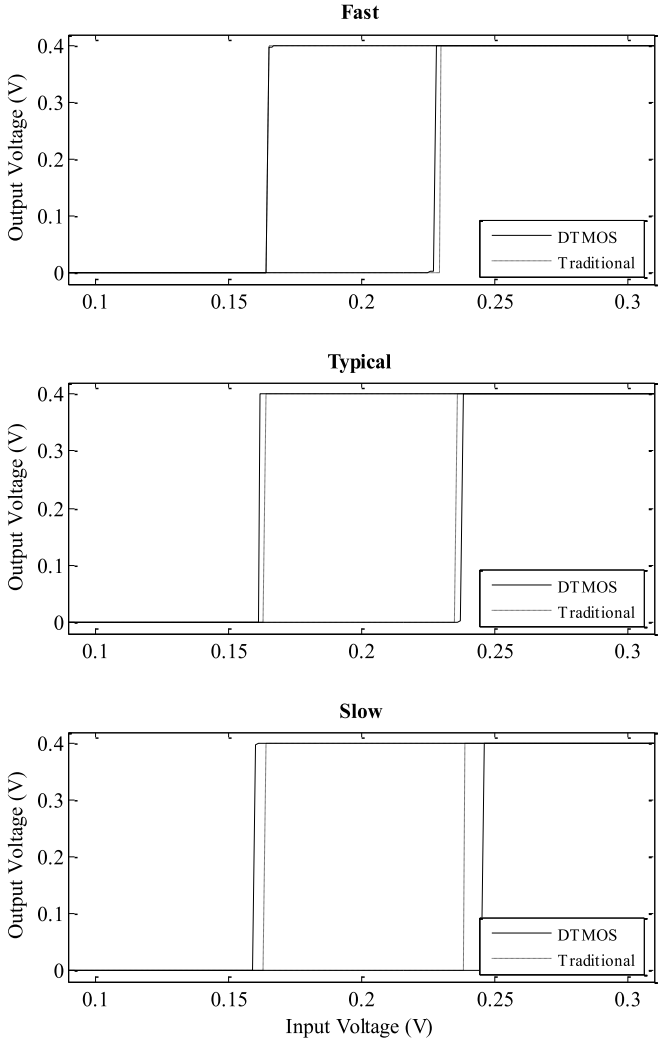

Fig. 5. Hysteresis plot for a buffer scheme using VTCMOS buffer and a traditional Schmitt trigger inverter with a DTMOS inverter.

TABLE I
CHARACTERISTICS OF A TWO SCHMITT TRIGGER BUFFER (FOR TYPICAL CORNER CONDITION)

Characteristic	Value	
	VTCMOS	Traditional
Number of Transistor	4	8 (6 + 2)
V_{LH}	237.5 mV	235.5 mV
V_{HL}	161.5 mV	163.5 mV
Hysteresis Width	76 mV	72 mV
Switching Current	310.92 μA	1.277 mA
Delay	2.88 ns	1.73 ns

current consumption (1.106 mA to 357.42 μA for AND gate, 248.24 to 123.71 μA for OR gate) using half areas for both gates.

Figs. 8 and 10 show the input noise immunity for different implementation methods. For the entire frequency range, the proposed Schmitt trigger circuits with the VTCMOS method

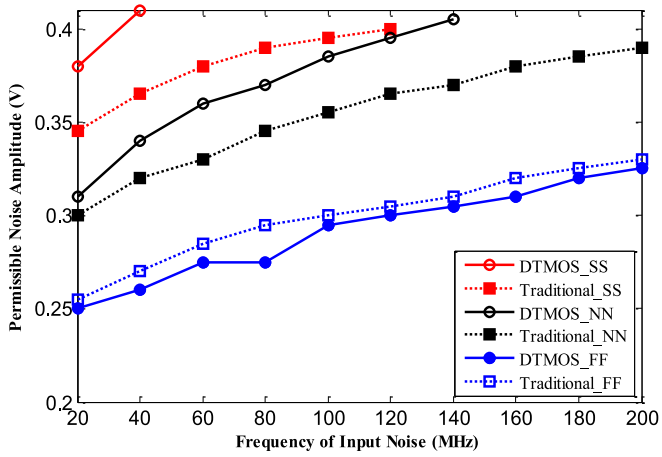

Fig. 6. Permissible noise amplitude comparison of Schmitt trigger buffer.

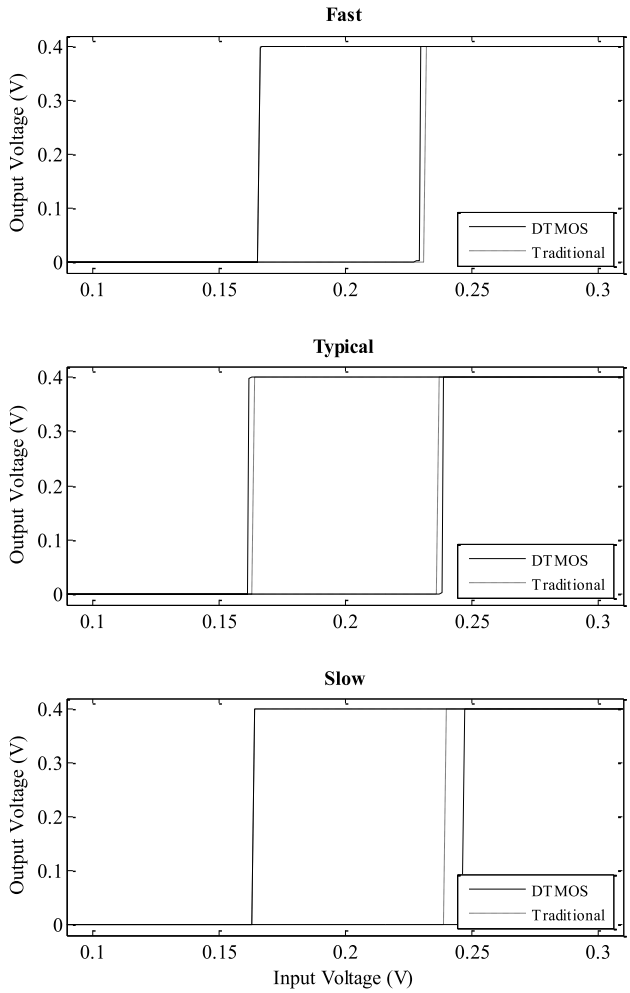

Fig. 7. Hysteresis plot of a Schmitt trigger AND gate according to the process corner.

show higher noise immunity for low-power operation compared to the traditional DTMOS Schmitt trigger, except for the fast corner case. For both AND and OR gate, slower corner condition makes noise immunity higher with widened hysteresis width.

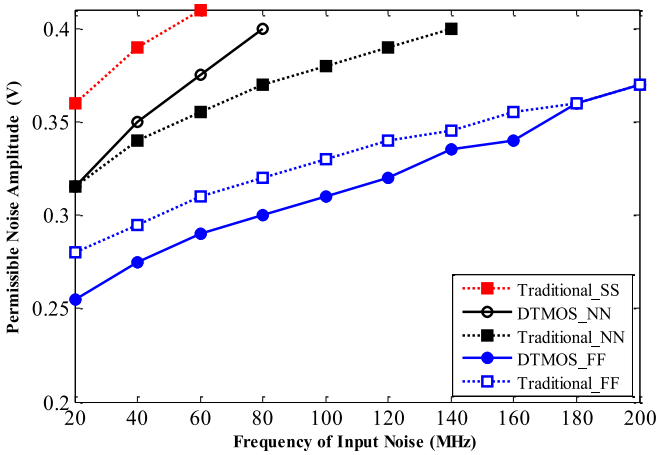

Fig. 8. Permissible noise amplitude comparison of a Schmitt trigger AND gate (Note: No failure occurred for DTMOS_SS).

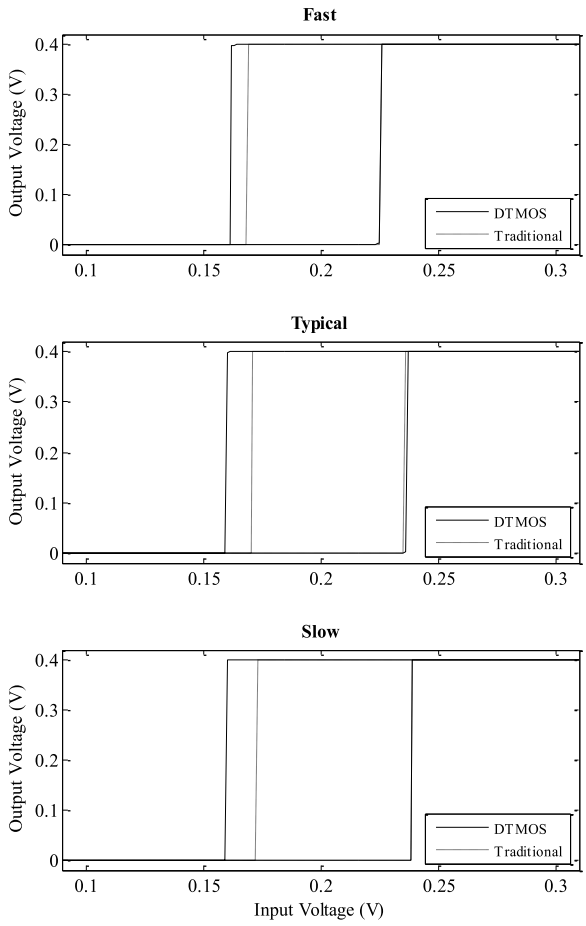

Fig. 9. Hysteresis plot of an OR gate.

C. Circuit-Level Immunity Improvement

We have explained above that the proposed Schmitt trigger can be used to improve gate-level noise immunity by requiring lower power consumption and less area than the traditional Schmitt trigger. To validate this approach in a larger digital circuit design, we applied the schematics shown in Figs. 1 and 4 to ISCAS '85 benchmark circuits [20]. Since ISCAS '85 benchmark circuits consist of several combinational circuits, we chose C432 (interrupt controller), C1908 (16-bit error decoder/corrector), and C6288 (16-bit multiplier) for the immunity simulation target.

Fig. 11 shows circuit-level noise immunity improvement with proposed logic gate for the ISCAS'85 benchmark circuits. The immunity of the C432 circuit was improved by 21.7% by using the proposed scheme. The noise immunities of the C1908 and C6288 circuits were improved by 17.8% and 19.3%, respectively. When the noise was injected at other input nodes, the proposed scheme was able to improve noise immunity by 19.73% on average, as shown in Fig. 12.

TABLE II
CHARACTERISTICS OF A TWO-SCHMITT TRIGGER AND GATE (FOR TYPICAL CORNER CONDITION)

Characteristic	Value	
	VTCMOS (Proposed)	Traditional
Number of Transistor	6	12 (10 + 2)
V_{LH}	238.5 mV	236.5 mV
V_{HL}	164.45 mV	164.45 mV
Hysteresis Width	75.29 mV	72.96 mV
Switching Current	357.42 μA	1.106 mA
Delay	4.426 ns	2.564 ns

TABLE III
CHARACTERISTICS OF A TWO-SCHMITT TRIGGER OR GATE

Characteristic	Value	
	VTCMOS	Traditional
Number of Transistor	6	12 (10 + 2)
V_{LH}	237.5 mV	237.5 mV
V_{HL}	157.51 mV	162.5 mV
Hysteresis Width	79.99 mV	75 mV
Switching Current	123.71 μA	248.24 μA
Delay	5.576 ns	3.804 ns

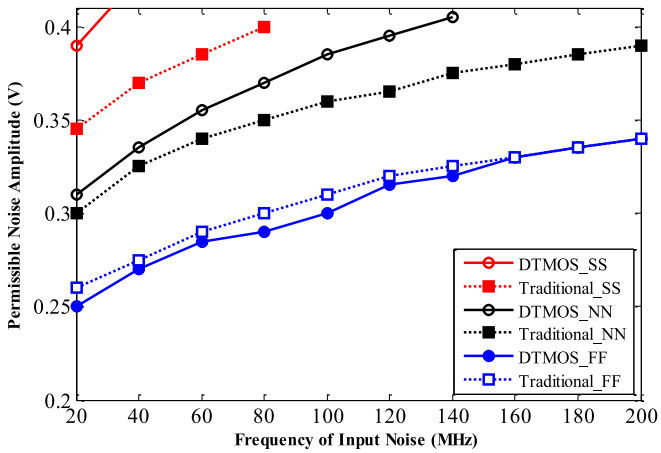

Fig. 10. Permissible noise amplitude comparison of Schmitt trigger OR gates.

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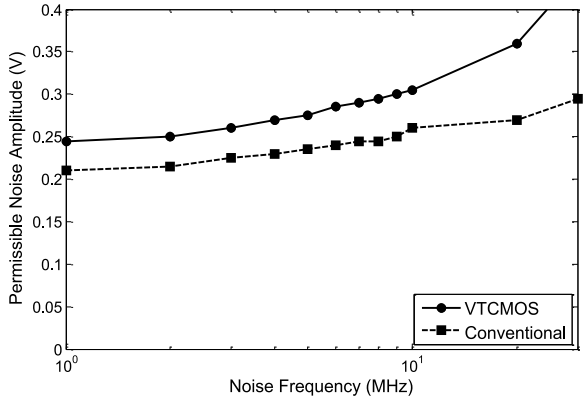
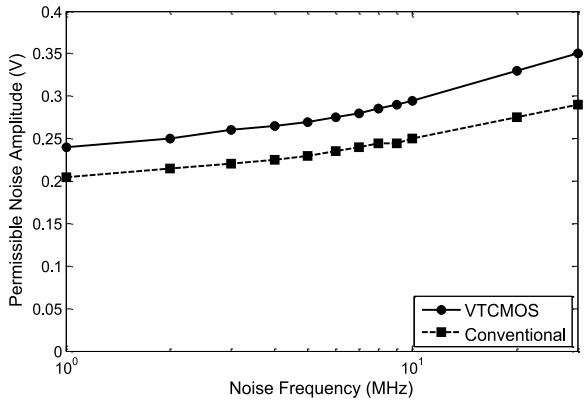
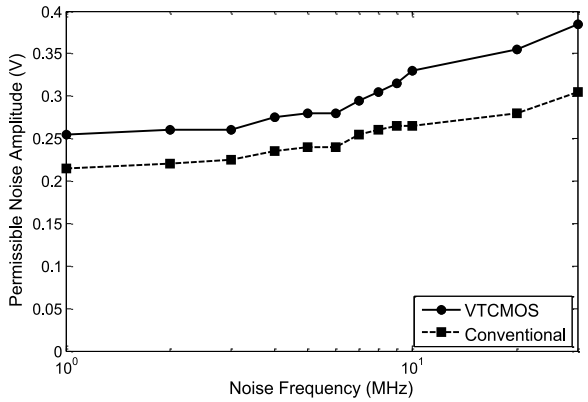


(a)



(b)



(c)

Fig. 11. Circuit-level noise immunity improvement with proposed logic gate for the ISCAS' 85 benchmark. (a) C432 (noise injected at input N1). (b) C1908 (noise injected at input N99). (c) C6288 (noise injected at input N273).

Because we greatly reduced the power consumption and area required at the gate level, these advantages are also provided at the circuit level. Therefore, the proposed scheme is a useful solution not only for nose immunity enhancement, but also for reducing power consumption and improving integration.

IV. Schmitt Trigger With Fully Adjustable Hysteresis

A. Limitations of the Proposed Scheme

As discussed in the previous section, the proposed DTMOS Schmitt trigger with VTCMOS is a better solution for noise immunity enhancement, requiring fewer transistors and lower power consumption compared with the conventional scheme. However, the proposed Schmitt trigger has the structural limitation of expanded hysteresis width.

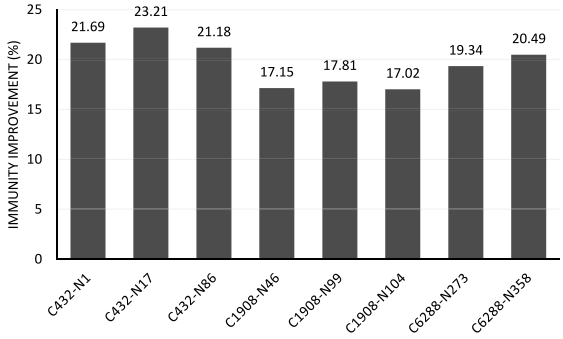


Fig. 12. Overall noise immunity improvement of ISCAS' 85 benchmark.

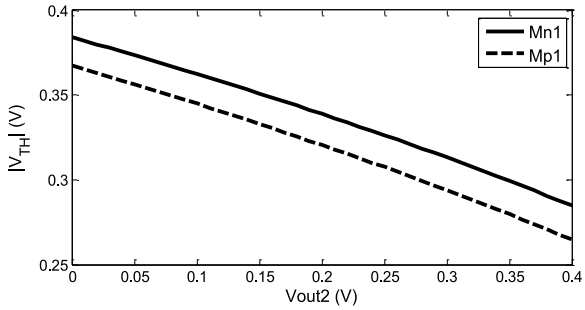


Fig. 13. Threshold voltage variation of Mn1 and Mp1 in Fig. 1(b) with respect to feedback body bias (V_{OUT2}).

The hysteresis width can be calculated from (1) and (2) in the following equation:

$$\begin{aligned}\text{Hysteresis Width} &= V_{\mathrm{LH}} - V_{\mathrm{HL}} \\ &= \frac{|V_{\mathrm{th0},p}| - |V_{\mathrm{th},p}| + \zeta \times (V_{\mathrm{th0},n} - V_{\mathrm{th},n})}{\zeta + 1}.\end{aligned} \tag{4}$$

However, as shown in Fig. 13, the threshold voltage variation of the NMOS $\Delta V_{\mathrm{th},n} = V_{\mathrm{th0},n} - V_{\mathrm{th},n}$ is nearly equal to that of the PMOS $\Delta V_{\mathrm{th},p} = |V_{\mathrm{th0},p}| - |V_{\mathrm{th},p}|$. Therefore, (4) can be approximated as follows:

$$\begin{aligned}\text{Hysteresis Width} &= \frac{\Delta V_{\mathrm{th},p} + \zeta \times V_{\mathrm{th},n}}{\zeta + 1} \cong \Delta V_{\mathrm{th}(n,p)} \\ &= \gamma \left(\sqrt{|2\Phi_F|} - \sqrt{|2\Phi_F - V_{\mathrm{BS}}|} \right)\end{aligned} \tag{5}$$

where Φ_{F} is the Fermi potential of the transistor, $\varepsilon_{\mathrm{si}}$ is the permittivity of silicon $\gamma = \sqrt{2q\varepsilon_{\mathrm{si}}^{'} N_{\mathrm{sub}}}/C_{\mathrm{ox}}$, and N_{sub} is the doping concentration of the substrate.

Hysteresis width is dependent on the value of γ, which means that it is independent of $\zeta \left(= \sqrt{(\beta_N / \beta_P)} \right)$. Since the value of γ is process-dependent, the hysteresis width cannot be controlled at the circuit level. As shown in Fig. 14, varying the sizes of the

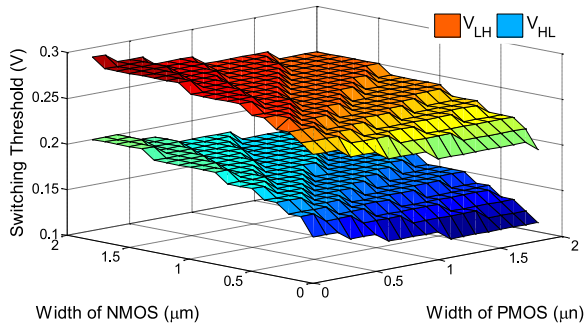


Fig. 14. Switching threshold voltage variation with varying widths of PMOS and NMOS for a 130-nm channel length.

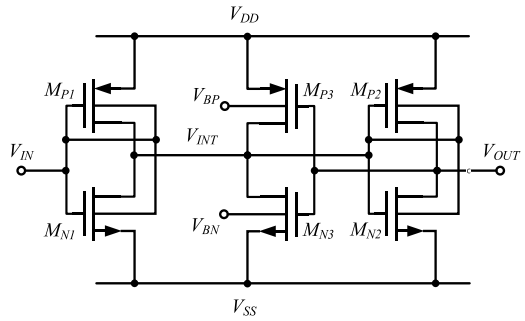


Fig. 15. DTMOS Schmitt trigger buffer with fully adjustable hysteresis.

PMOS and the NMOS cannot change the difference between $V_{\rm LH}$ and $V_{\rm HL}$, which is equal to the hysteresis width. Therefore, a different Schmitt trigger logic scheme is needed to vary the hysteresis width and thereby further enhance noise immunity.

B. Schmitt Trigger with Fully Adjustable Hysteresis

Based on the concept of a feedback network from [21] and [22], Singhanath *et al*. proposed the DTMOS Schmitt trigger with fully adjustable hysteresis [18]. Fig. 15 shows the schematic of the proposed scheme. As shown in the figure, the output node voltage is fed back to the gates of M_{P3} and M_{N3}. Therefore, M_{P3} or M_{N3} holds the value of the $V_{\rm INT}$ node, making this node unchangeable. In other words, the hysteresis width is increased by this feedback network, and the noise immunity of the circuit is simultaneously improved.

It is also possible to extend the hysteresis width by controlling the substrate potential of M_{P3} and M_{N3}. According to [15], $V_{\rm LH}$ and $V_{\rm HL}$ can be calculated using the following respective equations:

$$\mathrm{V_{LH}} = m\left\{K_1 + \sqrt{K_1^2 + m\left[K_2 + n\left(V_{\rm DD} - |V_{\rm TH,P3}|\right)^2\right]}\right\} \tag{6}$$

$$\mathrm{V_{HL}} = p\left\{K_1 + \sqrt{K_1^2 + p\left[K_3 - q\left(V_{\rm DD} - V_{\rm TH,N3}\right)^2\right]}\right\} \tag{7}$$

where $m = \beta_{N1}/(\beta_{N1} - \beta_{P1})$, $n = \beta_{P3}/\beta_{N1}$, $p = \beta_{P1}/(\beta_{P1} - \beta_{N1})$, $q = \beta_{N3}/\beta_{P1}$, $K_1 = -V_{\rm TH0,N1} - (\beta_{P1}/\beta_{N1})(V_{\rm TH0,P1} - V_{\rm DD})$, $K_2 = (\beta_{P1}/\beta_{N1})\left(V_{\rm TH0,P1} - V_{\rm DD}\right)^2 - \left(V_{\rm TH0,N1}\right)^2$, and $K_3 = \left(V_{\rm TH0,P1} - V_{\rm DD}\right)^2 + [\beta_{P1}/(\beta_{P1} - \beta_{N1})]\left(V_{\rm TH0,N1}\right)^2$. The key idea of [15] is to control $V_{{\rm TH},P3}$ by adjusting $V_{\rm BP}$ and $V_{{\rm TH},N3}$ through $V_{\rm BN}$ based on the following relations:

$$V_{{\rm TH},P3} = V_{{\rm TH0},P3} + \gamma\left(\sqrt{(|2\Phi_F| + V_{\rm DD} - V_{\rm BP})} - \sqrt{|2\Phi_F|}\right) \tag{8}$$

$$V_{{\rm TH},N3} = V_{{\rm TH0},N3} + \gamma\left(\sqrt{(|2\Phi_F| - V_{\rm BN})} - \sqrt{|2\Phi_F|}\right). \tag{9}$$

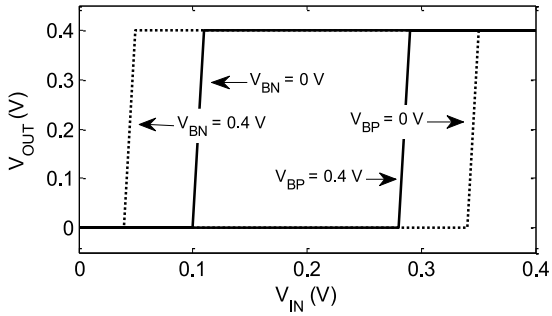


Fig. 16. Voltage transfer characteristic of the system in Fig. 15.

According to (6)–(9), $V_{\rm LH}$ depends on $V_{\rm BP}$, and $V_{\rm HL}$ depends on $V_{\rm BN}$. As a result, it is possible to control hysteresis width under conditions of low-power supply voltage, such as 0.4 V, as shown in Fig. 16.

Although adopting the hysteresis-adjustable DTMOS Schmitt trigger requires extra power consumption by the feedback network, the DTMOS scheme provides a significantly larger power margin than does the conventional Schmitt trigger [15].

V. Optimization of DTMOS Schmitt Trigger Gates

A. Simulation Setup

Although the hysteresis width of the hysteresis-adjustable DTMOS Schmitt trigger logic proposed in the previous section can be increased, it needs to be controlled at a proper value because both power consumption and delay increase for larger hysteresis widths.

To determine the optimal hysteresis width, we designed a buffer chain using ten identical Schmitt trigger buffers based on the one shown in Fig. 15. We injected a periodic clock pulse with noise to the input node and monitored the output waveform. For each Schmitt trigger, the hysteresis width was controlled by varying the amount of forward body bias voltage $V_{\rm BS}$ ($V_{\rm BS} = V_{\rm BN} = V_{\rm DD} - V_{\rm BP}$).

The power consumption and delay were measured for each Schmitt trigger buffer. To obtain highly reliable results, we divided all the simulation results by 10 to convert total power consumption or delay into the average of each Schmitt trigger.

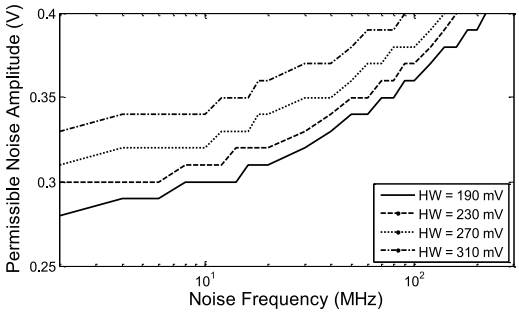


Fig. 17. Noise immunity for different hysteresis widths.

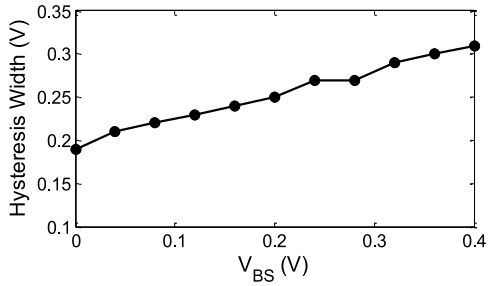


Fig. 18. Hysteresis width variation with respect to forward body bias.

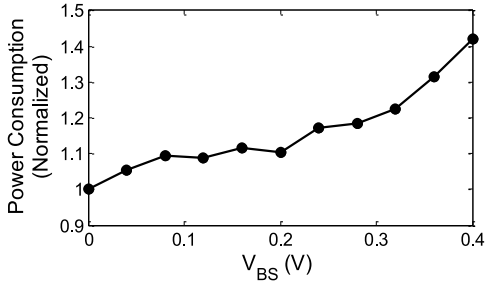


Fig. 19. Normalized power consumption variation.

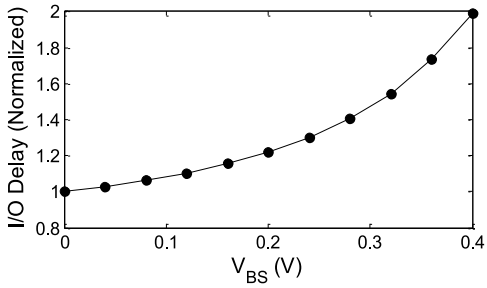


Fig. 20. Normalized I/O delay.

The simulation results are based on a Cadence Spectre simulation using SAMSUNG 130 nm process information [23].

B. Noise Immunity (Hysteresis Width)

Fig. 17 shows the relationship between permissible noise amplitude and its frequency for different hysteresis widths. In all cases, the noise immunity increased for higher frequencies and for greater hysteresis width. Therefore, it is reasonable to use hysteresis width as a representative of noise immunity. Fig. 18 shows the hysteresis width variation with respect to $V_{\rm BS}$: The hysteresis width of each Schmitt trigger buffer increased as the forward body bias voltage increased.

This can be explained using (8) and (9). As $V_{\rm BS}$ increases, both $|V_{{\rm TH},P3}|$ and $V_{{\rm TH},N3}$ decrease. Therefore, more current flows through $V_{\rm DD}$ or $V_{\rm SS}$ to the $V_{\rm INT}$ node, which prevents transition of the output. As a result, $V_{\rm LH}$ from (6) increases, $V_{\rm HL}$ from (7) decreases, and finally, hysteresis width increases.

C. Power Consumption

Fig. 19 shows the simulation results of the power consumption of a ten Schmitt trigger buffer chain, normalized with respect to the initial power consumption when $V_{\rm BS} = 0$V. Normalized power consumption can be calculated as follows:

$$P/P_0 = (1/P_0T)\int_0^T V_{\rm DD}\cdot i_{\rm sw}(t)\,dt \tag{10}$$

where P is power consumption, T is the period of the input signal, $i_{\rm sw}$ is the switching current of each buffer, and P_0 is the power consumption for the zero body bias condition, which is 13.85 nW for $(W/L) = (0.8\mu{\rm m}/0.13\mu{\rm m})$.

As described earlier, the Schmitt trigger consumes more switching current as $V_{\rm BS}$ increases. Therefore, we verified that increasing the hysteresis width to enhance noise immunity requires more power consumption.

D. I/O Delay

The simulated normalized I/O delay, which is the average delay of a single buffer of the buffer chain, is shown in Fig. 20. For the condition $(W/L) = (0.8\ \mu{\rm m}/0.13\ \mu{\rm m})$, the variation in I/O delay is doubled for $V_{\rm BS} = 0.4$ V compared to the zero body bias condition value τ_{d0}= 1.8 ns.

E. Optimal Hysteresis Width Extraction

We propose the immunity-power-delay ratio (IPDR) to represent the relationship between hysteresis width, power consumption, and delay. IPDR is expressed as follows:

$$\text{IPDR} = \text{HW}_{\rm norm}/(P_{\rm norm}\times\tau_{\rm norm}) \tag{11}$$

where $\text{HW}_{\rm norm}$ is the normalized hysteresis width, $\text{P}_{\rm norm}$ is the normalized power consumption, and $\tau_{\rm norm}$ is the normalized I/O delay. The IPDR of the hysteresis-adjustable DTMOS Schmitt trigger buffer is shown in Fig. 21. The optimal hysteresis width that maximizes IPDR can be determined from Figs. 18 and 21. Increasing $V_{\rm BS}$ more than 80 mV produces an IPDR of less than 1. At higher values of $V_{\rm BS}$, we expect improved noise immunity at the expense of increases in power consumption and delay. Therefore, except for a specific case that requires very high noise immunity, it is desirable to set $V_{\rm BS}$ to less than 80 mV for the transistor technology used in this study. Using the designs shown in Figs. 15 and 22, it is possible to expand the noise immunity at the large digital circuit level.

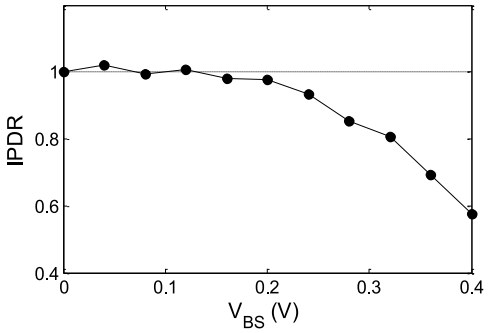


Fig. 21. IPDR of a Schmitt trigger buffer with fully adjustable hysteresis.

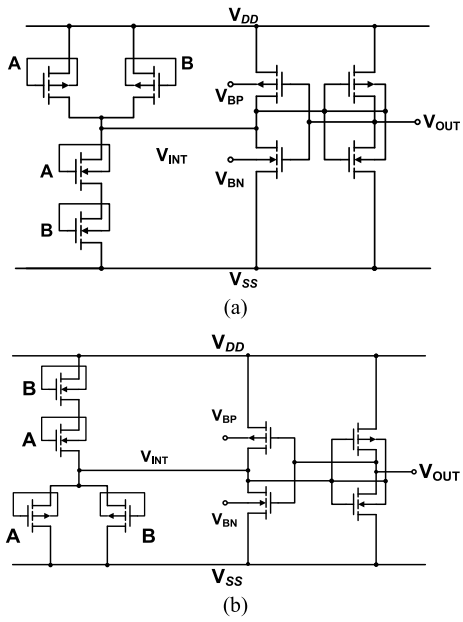


Fig. 22. Schmitt trigger AND/OR gate with fully adjustable hysteresis based on Fig. 15. (a) AND gate. (b) OR gate.

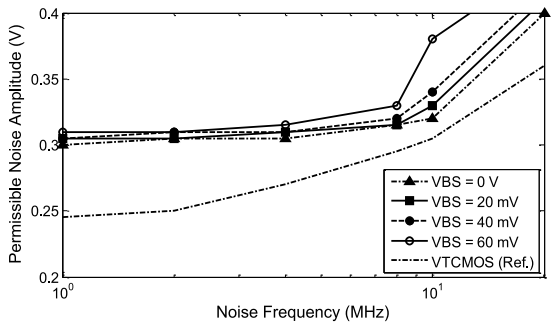


Fig. 23. Noise immunity enhancement by adopting adjustable hysteresis.

F. Application of IPDR in Benchmark Circuits

Fig. 22 shows the extension of the hysteresis-adjustable Schmitt trigger buffer shown in Fig. 15 to AND and OR gates.

Fig. 23 shows the simulation results of applying a Schmitt trigger logic gate with adjustable hysteresis to C432 of the ISCAS '85 benchmark. Compared to the Schmitt trigger logic implementation of C432 using nonadjustable hysteresis (VTCMOS), the immunity of the circuit based on adjustable hysteresis using $V_{\rm BS}$ increased dramatically. However, as the forward body bias ($V_{\rm BS}$) is increased from 0 V to 60 mV, the difference among hysteresis-adjustable Schmitt trigger case became less noticeable, especially for low-frequency noise.

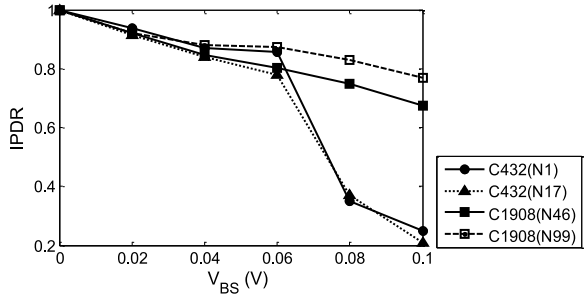


Fig. 24. IPDR of several circuits in the ISCAS' 85 benchmark.

Fig. 24 shows the IPDR values of several circuits in the ISCAS '85 benchmark, including C432. Every value decreased to less than 1 as the forward body bias $V_{\rm BS}$ increased because the noise immunity of the benchmark circuit was not much improved much by adjusting $V_{\rm BS}$, as shown in Fig. 23. However, the IPDR decreased sharply as $V_{\rm BS}$ exceeded 80 mV. This phenomenon occurs because power consumption and delay increase dramatically at values above this threshold. Therefore, it is reasonable to set a maximum $V_{\rm BS}$ to maximize noise immunity in order to achieve a reasonable performance tradeoff for this technology.

VI. Conclusion

As the supply voltage of a circuit decreases, noise immunity becomes more important to guarantee signal integrity. This paper presents a method of improving noise immunity applicable to subthreshold circuits.

The traditional method for immunity enhancement is to use a Schmitt trigger, which requires an additional current path to adjust the switching threshold voltage and a large area. However, by utilizing the proposed VTMOS scheme, which adjusts the threshold voltage of the MOS transistor to implement the hysteresis of the transfer characteristics, both area and switching power consumption can be significantly reduced while simultaneously providing improved noise immunity, at the expense of a slight increase in delay. Therefore, the proposed VTCMOS-based digital logic design can enable noise-immune low-power IC design.

To determine the optimum tradeoff point between noise immunity and performance, we investigated the DMOS Schmitt trigger with fully adjustable hysteresis. This method allows independent control of the two switching threshold voltages, so the hysteresis width can be increased. However, the power consumption and I/O delay also increase with greater hysteresis width.

We propose the IPDR, the ratio between immunity, power consumption, and I/O delay, as an index to determine the trade-off between noise immunity and performance, which enables the determination of the optimal hysteresis width. Based on the gate-level and transistor-level simulation results, the maximum forward body bias point of 80 mV was derived using SAMSUNG 130 nm technology. This approach can be applied to other technologies in order to derive the design guidelines to balance noise immunity and performance. The proposed optimization parameter IPDR provides a reasonable method to determine noise immunity under certain performance specifications when combined with NAND/NOR circuits.

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