5-6 GHz CMOS Low-Noise Direct Conversion Receiver Using a Differential RF VGA with a Differential Inductor Load

Wei-Ling Chang, Chinchun Meng, and Chih-Kai Chang
Department of Electrical Engineering
National Chiao Tung University
Hsinchu, Taiwan
ccmeng@mail.nctu.edu.tw

Guo-Wei Huang
High Frequency Technology Division
National Nano Device Laboratories
Hsinchu, Taiwan
gwhuang@ndl.narl.org.tw

***Abstract*— A low-noise low-power direct conversion receiver with a differential RF VGA is demonstrated using 0.18um CMOS technology. A topology that uses a differential inductor load for a differential RF VGA is employed for the single-to-differential conversion. Since the common-mode rejection ratio of a differential variable gain amplifier is increased by the mutual magnetic coupling in a differential inductor load, this work achieves noise floor less than 5 dB covering the 5-6 GHz band. Moreover, the conversion gain is around 50 dB and the total current consumption is 4.75 mA at 1.8 V supply voltage.**

Keywords—low-noise, low-power, LNA, CMOS, direct-conversion receiver, differential inductor, VGA.

I. INTRODUCTION

Wireless local area networks (WLAN) has been developed for many years and still gained attractions because of the increasing usage of the mobile devices. Recently, the IEEE 802.11 ac targets a wideband and high data-rate performance with each channel up to 80 MHz at the 5-6 GHz band. The direct conversion using CMOS technology has been a widely used topology among various receiver architectures because of the properties of high integration level and the absence of image signals [1], [2].

In this paper, a low-noise low-power I/Q DCR using a differential RF variable gain amplifier (VGA) with a differential inductor load to achieve a single-to-differential conversion is demonstrated. There are two remarkable properties by carefully designing a differential inductor with magnetic coupling at the load of a differential VGA. First of all, this design merges two inductors into one differentially excited symmetric inductor to save the die area through magnetic coupling and increase the quality factor [3]. Secondly, a differential inductor has a good common-mode rejection ratio (CMRR) because it functions differently for a differential-mode signal and a common-mode signal. More detailed discussions are reported in Section II, and Section III shows the measurement results. Finally, conclusions are given in Section IV.

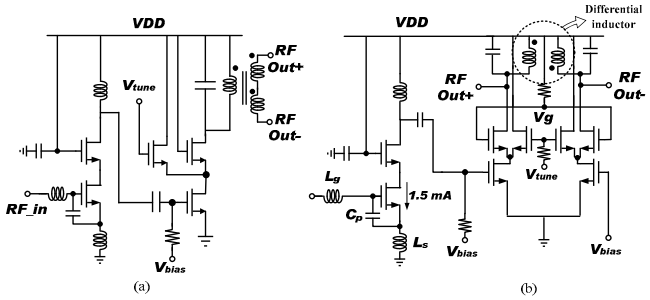

Fig. 1. Two VGA topologies for an LNA with the subsequent RF VGA, (a) a single-ended VGA with a single-to-differential transformer load (b) a differential VGA with a differential inductor load.

II. CIRCUIT DESIGN

Fig. 1 shows two topologies of an LNA with the subsequent RF VGA. A single-ended RF VGA with a transformer load for the single-to-differential conversion at output is shown in Fig. 1(a) [4]. An alternative topology that uses a differential RF VGA with a differential load to achieve the differential out is shown in Fig. 1(b). A cascode LNA is employed with a source-degenerated inductor L_s, a gate inductance L_g and the parallel gate-source capacitor C_p to achieve input match and noise match at the same time under the current consumption constraint of 1.5 mA. The subsequent RF VGA has the gain control achieved by adjusting the voltage of V_{tune} for current-steering in the cascode device. The differential output is achieved differently for both topologies. The magnetic coupling in the transformer of Fig. 1(a) performs the single-to-differential conversion while the self-inductance is in resonance with the load capacitor. On the contrary, the mutual coupling between half-coils of a differential inductor in Fig. 1(b) enhances the inductance seen by the load capacitor to result in a differential inductor with a small area. Thus, the topology in Fig. 1(b) is adopted in this paper. However, a good common-mode rejection ratio is needed for a single-to-differential conversion in Fig. 1(b) because the differential RF VGA is fed with a single-ended input signal.

Fig. 2(a) shows the layout and equivalent circuit of a differential inductor. The magnetic coupling between the half-coils enhances the inductance value and the quality factor is

978-1-5090-1235-0/16/$31.00 ©2016 IEEE

high for a differential excitation. Thus, the area of a differential inductor in Fig. 1(a) is strongly reduced when compared to that of a single-to-differential transformer in Fig. 1(b). Fig. 2(b) indicates the equivalent circuit with the dot convention of a differential inductor. The T-model equivalent circuit with the self-inductance L and the mutual inductance M is shown in Fig. 2(c). The mutual inductance is negative in Fig. 2(c) because the magnetic flux is subtracted when the ports are excited with currents flowing in as shown by the dot convention in Fig. 2(b). It is noticeable that the common/differential modes experience different loads. The differential load sees an $L+M$ load while a common mode sees an L-M load. As a result, after a careful design of the differential inductor with the coupling k factor close to one, the CMRR approaches infinite because the common-mode has a short-circuit load while the differential-mode sees an open load caused by the parallel resonance of the load capacitor and 2 L load.

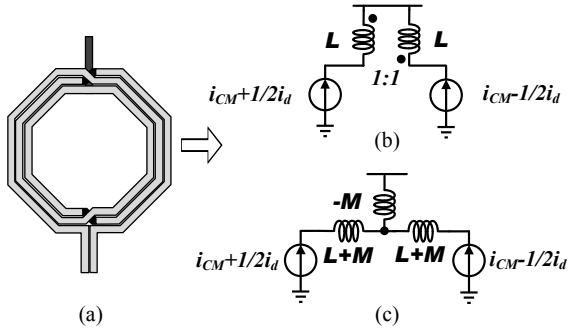

Fig. 2. (a) Conceptual layout of a differential inductor. (b) Simplified equivalent circuit (c) T model with self and mutual inductances of a differential inductor.

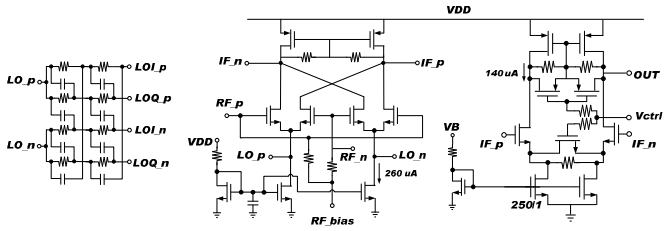

Fig. 3. The schematic of a double-balanced I/Q active mixers with IF VGA and the LO poly-phase filter.

In this work, the proposed I/Q DCR consists of a one-stage low noise amplifier (LNA) followed by a differential RF VGA with a differential inductor load, two double-balanced Gilbert mixers pumped by a poly-phase filter for LO I/Q generation, two output IF VGAs. The double-balanced active mixer mixes the RF signal with the I/Q LO signals from the poly-phase filter. A two-stage RC-CR poly-phase filter, as shown in Fig. 3, is employed at the differential LO ports to generate the accurate differential quadrature LO signals. The active mixer can not only provide conversion gain but also great port-to-port isolation in a low current consumption. It consumes only 260 µA in one path as shown in Fig. 3 [2]. Last but not least, Fig. 3 also shows an IF VGA with a wide gain tuning range using R-r attenuation method [5] behind the mixer. By tuning voltage V_{ctrl}, the IF tuning range is more than 25 dB with 140 µA current consumption for one IF VGA.

III. Measurement Results

Fig. 4 shows the die photo of a 5-6 GHz low-noise low-power I/Q DRC in 0.18µm CMOS technology, and the die-size is 1.5 x 1 mm^2 including the DC/RF pads. By on-wafer measurement, the total current consumption is 4.75mA at the supply voltage of 1.8 V. Fig. 5 indicates the conversion gain and the input return loss with respect to RF frequency. The peak gain is 50 dB at 5.4 GHz and the 3-dB bandwidth is from 5.1 GHz to 5.9 GHz. Also, the return loss is better than 10 dB for the whole operating frequency range. By properly biasing the mixer core, the LO pumping power is about 6 dBm to achieve fully current commutation as shown in Fig. 6. Fig. 7 shows the noise performance of this work. At the measurement frequency point of 5.2/5.5/5.8 GHz, the flicker noise corner is around 1 MHZ as expected for the active MOS mixer [1] and the noise floor can be less than 6/5/5 dB, respectively. The flicker noise corner of a CMOS active mixer can be reduced by many means such as dynamic injection, static injection, passive mixer and BJT mixer cores as discussed in the literature [1], [3] and thus is not a focus of this paper. The DRC has a wide gain tuning range of 35 dB while V_{ctrl} is tuned from 0 to 0.8 V. Due to the double-balance topology, the isolations of LO-to-RF and LO-to-IF are better than 60 dB as shown in Fig. 9. Fig. 10 demonstrates the amplitude imbalance < 1 dB and the phase difference < 2 degrees of the output I/Q signals. Finally, the I/Q output signal waveforms are shown in Fig. 11.

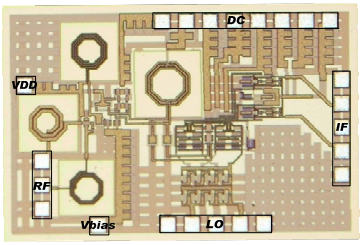

Fig. 4. Die photo of a 0.18µm CMOS 5-6 GHz I/Q DRC.

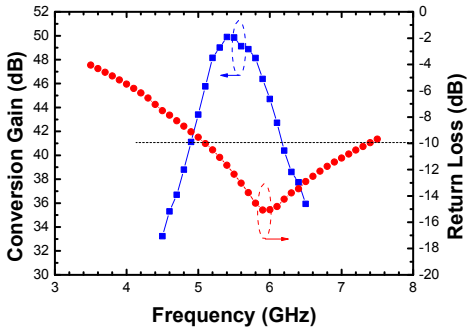

Fig. 5. Conversion gain and input return loss with respect to RF frequency of a 0.18µm CMOS 5-6 GHz DRC receiver.

IV. Conclusions

This paper demonstrates a 5-6 GHz I/Q DRC receiver with the differential RF VGA in a 0.18µm CMOS process. The noise floor is around 4.8-6 dB covers the range from 5 to 6 GHz. Moreover, the conversion gain is up to 50 dB at a low current consumption of 4.75 mA.

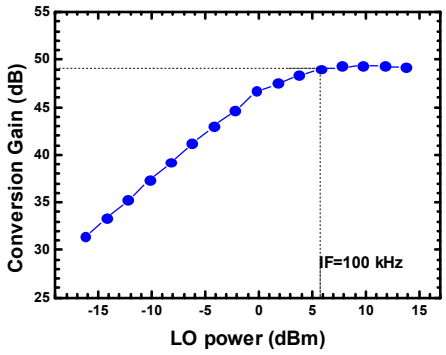

Fig. 6. Conversion gain with respect to LO power of a 0.18µm CMOS 5-6 GHz DRC receiver.

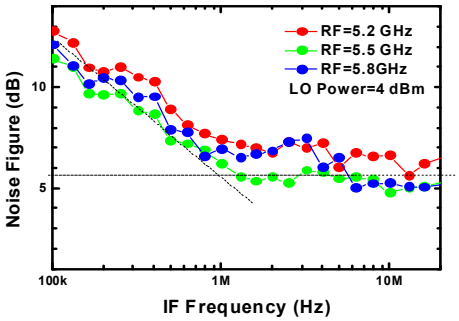

Fig. 7. Noise performance of a 0.18µm CMOS 5-6 GHz I/Q DRC.

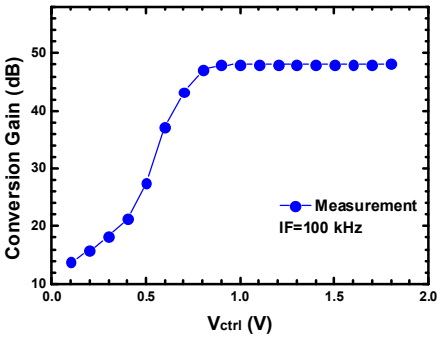

Fig. 8. Conversion gain with respect to V_{ctrl} of an IF VGA for a 0.18µm CMOS 5-6 GHz DRC receiver.

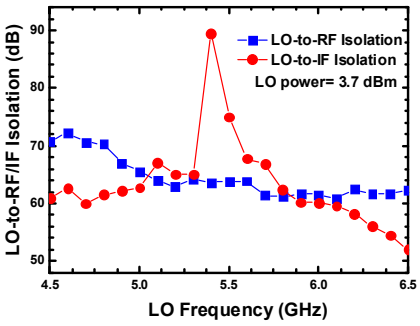

Fig. 9. Isolation performance between LO, RF and IF of a 0.18µm CMOS 5-6 GHz DRC receiver.

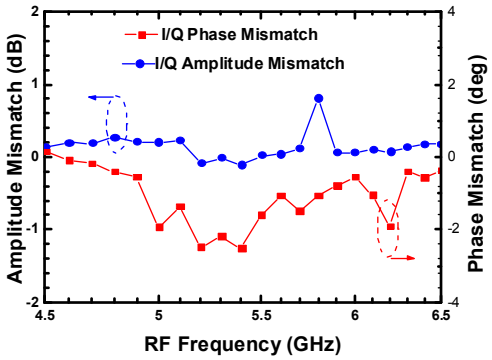

Fig. 10. Amplitude mismatch and phase difference of a 0.18µm CMOS 5-6 GHz DRC receiver.

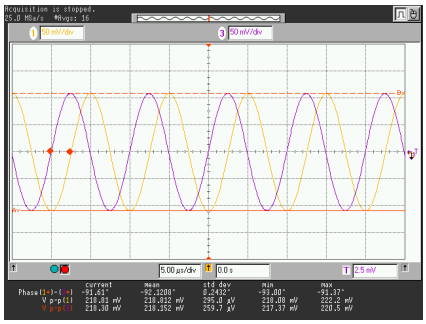

Fig. 11. I/Q waveforms of a 0.18µm CMOS 5-6 GHz DRC receiver.

ACKNOWLEDGMENT

This work is supported by National Science Council of Taiwan, Republic of China under contract numbers NSC 104-2221-E-009 -061 and by MoE ATU program under contract number 95W803. The authors would like to thank National Chip Implementation Center (CIC) for technical support.

REFERENCES

[1] H. Darabi and A. A. Abidi, "Noise in RF-CMOS mixers: A simple physical model," IEEE J. Solid-State Circuits, vol. 35, pp. 15 - 25, Jan. 2000.

[2] J. Park, C.-H. Lee, B.-S. Kim and Joy Lasker, "Design and Analysis of Low Flicker-Noise CMOS Mixers for Direct-Conversion Receivers" IEEE Trans. Microw. Theory Tech., vol. 54, no. 12, pp. 4372 - 4380, Dec. 2006.

[3] D. J. Cassan and John. R. Long, "A 1-V Transformer-Feedback Low-Noise Amplifier for 5-GHz Wireless LAN in 0.18-µm CMOS," IEEE J. Solid-State Circuits, vol. 38, pp. 427 - 435, Mar. 2003.

[4] J. S. Syu, C. C. Meng, and C. L. Wang, "2.4-GHz Low-Noise Direct-Conversion Receiver With Deep N-Well Vertical-NPN BJT Operating Near Cutoff Frequency" IEEE Trans. Microw. Theory Tech., vol. 59, no. 12, pp. 3195 - 3205, Dec. 2011.

[5] Y.-S. Youn, C.-S. Kim, N.-S. Kim, and H.-K. Yu, "A 1 GHz-band low distortion up-converter with a linear in dB control VGA for digital TV tuner," in IEEE Radio Freq. Integrated Circuits Symp. Dig., pp. 257-260, May 2001.