Investigating the Behavior of Physical Defects in pn-Junction Based Reconfigurable Graphene Devices

Sandeep Miryala, Andrea Calimera,
Enrico Macii, Massimo Poncino
Politecnico di Torino,
10129, Torino, Italy

Letícia Bolzani Poehls
Catholic University of Rio Grande do Sul,
90619-900, Porto Alegre, Brazil

***Abstract*—Graphene, one of the viable candidates to replace Silicon in the next generation electronic devices, is pushing the research community to find new technological solutions that can exploit its special characteristics. Among the proposed approaches, the electrostatic doping represents a key option. It allows the implementation of equivalent pn-junctions through which is possible to build a new class of reconfigurable logic gates, the devices analyzed in this work. Recent works presented a quantitative analysis of such gates in terms of area, delay and power consumptions, confirming their superiority w.r.t. CMOS technologies below the 22nm.**

This work explores another dimension, that is testability, and proposes a study of possible physical defects that might alter the functionality of the graphene logic gates. The electrical behavior of faulty devices, obtained through the emulation of physical failures at the SPICE-level, has been analyzed and mapped at a higher level of abstraction using proper fault models. Most of such models belong to the CMOS domain, but for some specific class of defects, new fault definitions are needed.

I. Introduction

Due to its unique electro-mechanical properties, graphene [1] has been indicated as a viable candidate to replace Silicon in the next generation of electronic circuits and micro-systems. Nevertheless, the carrier dynamics that govern its electrical behavior substantially differs from that of conventional semiconductor technologies. The main difference lies in the fact that the energy band structure of graphene is gapless, namely, conduction and valence bands touch each other at zero-energy where the Fermi Energy (E_F) passes. This prevents the material to implement the OFF state, and hence, to achieve a high ON/OFF current ratio. This makes the implementation of digital graphene devices a true challenge.

To overcome this issue, many device structures and fabrication processes have been proposed in the last years. Most of them, fruit of research investments by world-class industries, like IBM [2] and Samsung [3], differ in the way graphene is isolated, patterned, controlled and interconnected. At this preliminary stage it is hard to predict which of these solutions will prevail in the electronics market, and in how much time; instead, what is of paramount importance is to understand the main features that distinguish each option, assess their limits and the design opportunities they give.

Moving toward this direction, this papers proposes a study of the fault models that can cover possible physical defects in a new class of reconfigurable graphene logic device. First introduced in [4] and here referred as *RG-device*, such device have an interesting characteristic that places them at the head of the race: differently from devices that require the pattering of graphene (e.g., nanoribbon FETs [5]), the RG-devices make use of a pristine sheet of graphene, thereby keeping unchanged the intrinsic properties of the material.

A RG-device consists of a graphene sheet with co-planar back-gates that implement an electrostatic doping [6]. When a positive (or negative) voltage is fed to back gate, the E_F of the graphene region on top of that gate shifts up (down) in the conduction (valence) band leading to n-type (p-type) doping; opposite bias voltages on adjacent gates are used to create equivalent pn-junctions [7]. Through a pn-junction is possible to implement a dynamic tuning of the electron transmission probability across the graphene sheet. This allows to electronically reconfigure the resistive paths between inputs and output ports of the device (the metal-to-graphene contacts placed on the front side of the graphene sheet). From a functional point of view, a RG-device implements a reconfigurable multiplexer [8]; proper signal assignments at the inputs allows to perform all basic Boolean logic functions [9]. Promising results have been published in [4] and [10] which indicate that the RG-devices can outperform CMOS technologies below the 22nm node in terms of both delay and power consumption.

The contribution of this work is twofold. On the one hand it proposes an analysis of the electrical misbehaviors induced by physical defects; since the RG-device is built on a pristine sheet of graphene, only the physical defects at the metal pints of the device have been considered. On the other hand, it helps to understand whether the fault models typically adopted in standard CMOS technologies can also cover physical failures at the logic level and, if not, present alternative models. Two types of defects are taken into account: *Open* defects, i.e., floating metal contacts, and *Short* defects, i.e., short between metal contacts that are placed physically close. The analysis is validated through the SPICE simulation of a Verilog-A model of the RG-device in which physical failures have been injected manually; different configurations implementing basic Boolean logic functions, i.e., INV, AND, OR, and MUX. The obtained matching between defects and faulty behavior is finally used to identify suitable fault models.

978-1-4799-0597-3/13/$31.00

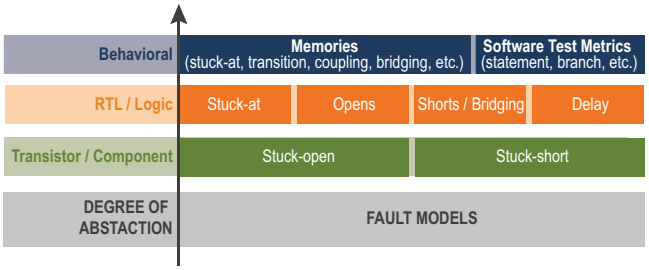

Fig. 1. Fault models taxonomy

II. Fault Models for Digital Circuits

The aggressive scaling of device geometries significantly increased the occurrence of physical defects during the manufacturing process of integrated circuits. The adoption of appropriated models that can abstract physical failures at higher layers is mandatory for a proper handling of designing the testing procedures.

Fault modeling is the translation of physical defects to mathematical constructs that can be managed by software simulators with the aim of providing a metric for quality assessment [11]. In this context, a *fault* is the representation of a defect at higher levels of abstraction [12]. Modeling at different levels of abstraction corresponds to different tradeoff between the fault model accuracy, i.e., its capability to represent the defect, and the speed of its simulation [13]. Figure 1 summarizes the most adopted fault models for CMOS technologies [12]. The integration of multiple fault models typically allows the coverage of the entire set of physical defects.

At the Behavioral Level few implementation details of the circuit are available, therefore, models at this level play a more important role in simulation-based verification rather than in testing.

At the Register-Transfer Level (RTL) and Logic Level, circuits are represented by functional blocks and logic gates netlist. The most common fault model for digital design relates to *stuck-at* faults affecting the interconnection between gates [12]. Although intuitive and easy to manage, the stuck-at model cannot cover all the possible faulty behaviors that might appear [14]. In order to bridge this gap, a model at the logic level that consists of *Open* and *Short* faults has been devised. For further details on fault model implementations, out of the scope of this work, readers can refer to literature on the subject (e.g., [12], [14]).

At the Transistor or Component level, the granularity of the models is the single transistor or component, therefore, fault models like *stuck-open* and *stuck-short*, do apply to individual transistors rather than single gates. Stuck-open faults produce a floating state of a given transistor contact, whereas stuck-short faults produce a conducting path between power supply and ground [12].

III. Reconfigurable Graphene Device

A. Graphene PN-Junction

Figure 2 shows the basic structure of a voltage controlled graphene pn-junction. The two metal back-gates are used to implement the electrostatic doping [7], whereas the front metal contacts represent the conceptual source (left) and the probe (right) that are emitting and receiving the carriers.

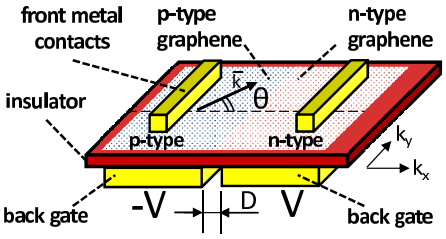

Fig. 2. Graphene-based pn junction.

When a back-gate is fed with a negative voltage, the Fermi energy level E_F is shifted down in the valence band leading to p-type doping in the graphene region on top of the gate itself. On the contrary, a positive voltage shifts E_F up in the conductance band leading to n-type doping. In case a symmetric control voltage is simultaneously applied at two adjacent split gates ($\pm V$ in Figure 2), the device implements the pn-junction.

As demonstrated in [15], carriers injected in the p-region through the left front contact cross the potential barrier at the pn-junction with a transmission probability $T(\theta)$ that depends on (i) the angle θ between the electron's wave vector $\bar{\mathbf{k}}$ and the normal of the junction, and (ii) the width D of the pn transition region. Equation 1 gives the analytical expression of $T(\theta)$:

$$T(\theta) = cos^2(\theta)e^{-\pi \mathbf{k} D \sin^2 \theta} \quad (1)$$

The transmission probability $T(\theta)$ is 1 for those carriers that travel orthogonally toward the junction (i.e., $\theta = 0$) regardless of D and exponentially decreases for higher values of θ ($T(\theta) = 0$ for $\theta = \pi/2$). As shown in the next subsection, the RG-device exploits the transmission properties of the pn-junction to implement a voltage controlled switch.

B. RG-device Structure and Functionality

Figure 3 shows 3D, back and front views of the RG-device as introduced in [4]. It consists of two back-faced pn-junctions: $j1$, on the left, controlled by back-gate pair S-$\bar{U}$; $j2$, on the right, controlled by back-gate pair S-U.

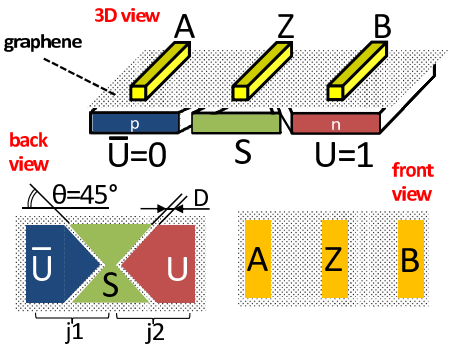

Fig. 3. RG-device structure.

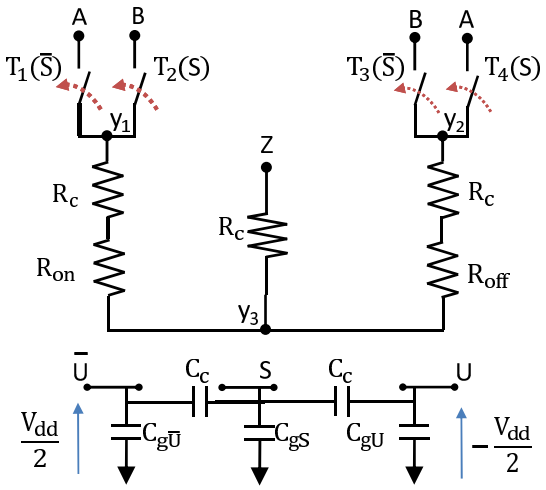

Fig. 4. Electrical schematic of the reconfigurable device.

The back-gates $\bar{U}$ and U are driven with a fixed and symmetric voltage, i.e., $\bar{U} = -Vdd/2$ and $U = +Vdd/2$. This forces the lateral regions of the graphene sheet to be p-type (on the left) and n-type (on the right). Notice that in this implementation, $+Vdd/2$ and $-Vdd/2$ correspond to logic "1" and logic "0" respectively.

The shared back-gate S in the center serves as logic input. When S='0', the central graphene becomes p-type. This forms a pp-junction on the left, i.e., a zero barrier potential through which carriers are totally transmitted, and a pn-junction on the right, i.e., a barrier potential through which carriers are transmitted with the transmission probability $T(\theta)$ presented in the previous subsection. It is worth noticing that θ is physically imposed as 45^o by construction (see the back-view in Figure 3). The resulting p-p-n doping profile of the graphene sheet creates a low-resistive path (R_{low}) between the front contacts *A*-*Z* and a high-resistive path (R_{high}) between the front contacts *B*-*Z*. This forces the output Z following the input signal associated with the lowest resistance, i.e., $Z = A$. A dual behavior is observed when S ="1". In this case the central graphene region is n-doped, leading to p-n-n graphene doping; a low-resistive path between the contacts *B*-*Z* makes the output to follow B, i.e., Z=B.

From a functional point of view, the RG-device serves as a multiplexer, that is, Z=A when S ='1', while Z=A when S ='0'. As shown later in the text, different input configurations allows to build several basic Boolean functions.

C. Equivalent Electrical Model

Figure 4 shows the equivalent electrical model of the RG-device implemented using the Verilog-A modeling language [9]. The four switches T_1, T_2, T_3, T_4, are controlled by the input voltage S. When $V(S) = -V_{dd}/2$ (S ="0"), T_1 and T_3 are closed, while T_2 and T_4 open; hence, A is connected to y_3, hence to Z, through the low resistance R_{low} (left branch), while B is isolated from y_3 due to the high resistance R_{off} (right branch). When $V(S) = V_{dd}/2$ (S ="1"), T_2 and T_4 are closed, while T_1 and T_3 open; hence, B is connected to y_3 through R_{low}, and A is isolated from y_3 due to R_{high}.

The analytical expressions of R_{low} and R_{high} have been derived from [4]. R_{low} is simply defined by the geometrical width W of the graphene sheet, as shown in the following equation:

$$R_{nn} = R_o/N_{ch} = \frac{h\pi}{4q^2 W k_F} \tag{2}$$

where $R_o = h/4q^2$ is the quantum resistance per mode in the graphene sheet, and $N_{ch} = Wk_F/\pi$ represents the number of excited modes [16].

The value R_{high}, instead, is function of the transmission probability $T(\theta)$ (Equation1) with θ=45° as imposed by the geometries of the device:

$$R_{pn} = \frac{R_o}{T(\theta)N_{Ch}} = \frac{h\pi}{4q^2 W K_F T(45°)} \tag{3}$$

It is worth noticing that R_{high}/R_{low} is in the order of 10^6.

Resistive and capacitive parasitics are integrated in the model. The resistors R_c (assumed to be 10Ω [4]) model the contact resistance at the three front metal-to-graphene contacts. The lumped capacitances C_g consists of the oxide capacitance C_{ox} in series with the quantum capacitance C_q from the graphene sheet. Finally C_c models the capacitive coupling among the three back-gates. Since in this work we deal with DC-analysis we omit the detailed description of C_g and C_c; interested readers can refer to [4] for additional details.

IV. Understanding and Modeling Physical Defects in RG-devices

In order to characterize the electrical behavior of faulty RG-devices and map physical failures to fault models, a basic scheme composed of three main stages has been followed:

1) *Specification of physical defects*, during which a subset of potential physical failures that can occur in the RG-devices has been identified.
2) *Defect modeling and simulation*, where the effects of the physical failures have been modeled by means of equivalent electrical circuits for SPICE simulations.
3) *Mapping physical failures to fault models*, in which the faulty behavior of the RG-device has been analyzed and, when possible, mapped to some fault models (borrowed from the CMOS domain).

A. Specification of physical defects

As introduced in Section III, a RG-device consists of a pristine sheet of graphene that in this work is considered as fault-free. More attention, instead, is given to defects on the metal back-gates and the metal-to-graphene front contacts, whose fabrication is similar to manufacturing processes used in today's VLSI technologies. Hence, this paper considers failure mechanisms that typically occur in CMOS circuits [17], namely, *metal shorts* (*Shorts* hereafter), i.e., short-circuits between two (or more) contacts that are physically close, and *metal opens* (*Opens* hereafter), i.e., open-circuit of metal contacts.

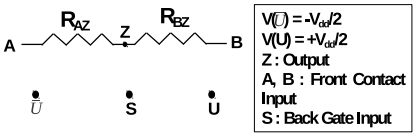

Fig. 5. Fault free electrical model of the RG-device in the DC-domain

It is worth noticing that, given the physical geometries of the RG-device, shorts are more likely to appear at the back-gates, whereas front-contacts are more immune to these kind of defects. TableI summarizes the defects we analyzed.

TABLE I
PHYSICAL FAILURES INJECTED IN THE RG-DEVICE

Shorts	*Opens*
between U and S	front contact A
between S and U	front contact B
between U, S and U	front contact Z

B. Defect modeling and simulation

The electrical model described in Section III is used as basis for emulating the physical failures in the RG-device. Figure 5 shows a simplified version of such model in the DC-domain. The two back-gates $\bar{U}$ and U are connected to the power supply rails, -$V_{dd}/2$ and +$V_{dd}/2$ respectively. The resistor between the front contacts A and Z is labeled as R_{AZ}, whereas that between B and Z is R_{BZ}; their value ranges from R_{low} to R_{high} depending on the potential applied at the central back-gate S (the control voltage of the four switches of the original model Figure 4). Notice that in the schematic R_{AZ} and R_{BZ} lump the resistive parasitic R_c at the front-contacts.

Modeling shorts and opens defects using the fault-free model of Figure 5 is straightforward. Figure 6 shows the resulting faulty netlists.

1) Electrical models under short defects: since the back-gates $\bar{U}$ and U are connected to the power rails, their voltage is stronger than that of S, which is supposed to be driven by a RG-device in the fan-in.

In case of a Short between $\bar{U}$ and S (Figure 6-a), the voltage at $\bar{U}$, i.e., -$V_{dd}/2$, dominates on S; recalling the effect of electrostatic doping, this corresponds to the formation of a pp-junction between A and Z, which implies $R_{AZ} = R_{low}$, and a pn-junction between B and Z, namely, $R_{BZ} = R_{high}$. On the contrary, in case of a Short between S and U (Figure 6-b) the voltage at U, i.e., +$V_{dd}/2$, dominates on S, leading to a pn-junction between A and Z, which implies $R_{AZ} = R_{high}$, and a nn-junction between B and Z, namely, $R_{BZ} = R_{high}$. The picture is less intuitive in the presence of a concurrent Short between $\bar{U}$, S and U (Figure 6-c), which corresponds to a short between the power-rails +$V_{dd}/2$ and -$V_{dd}/2$. In this case, the entire supply voltage V_{dd} drops across the low-resistive path formed by the short of the three back-gates, which, due to a high current density, may burn up. Although is correct to believe that this condition may induce a severe failure of the entire device, in this theoretical study this condition is mapped as the case of missing doping across the entire graphene sheet. Under this condition, a pure semi-metallic resistive behavior of graphene is considered, i.e.,

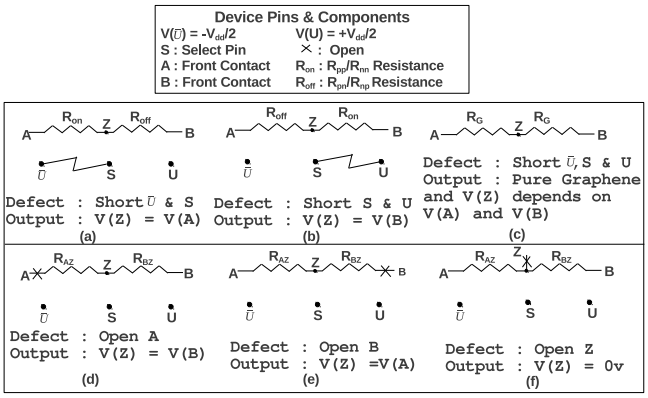

Fig. 6. Equivalent circuits for the RG-device under Open and Short defects

both inputs A and B connected to Z through the intrinsic resistance of the graphene sheet, i.e., R_{AZ}=R_{BZ}=R_G, with $R_{low} < R_G < R_{high}$.

2) Electrical models under open defects: an Open defect on a front metal contact prevents the current flowing through the contact itself. In the case of an Open defect at at A (Figure 6-d), the output port Z is driven by the signal B (due to high impedance on contact A), while, in case of an Open defect at B (Figure 6-e), Z is driven by A (due to high impedance on contact B). When an open defect occurs at the output contact Z (Figure 6-f), the output voltage settles at 0V.

C. Mapping physical failures to fault models

Appropriate input logic signals can be fed to the RG-device in order to build several basic Boolean logic functions. Depending on the input configuration pattern, the same physical defect may thereby perturb the logic functionality of the RG-gate in different ways. This motivates the choice of a cell-based analysis. A complete description of all the possible logic configurations can be found in [9]. Figure 7 only shows the implementation of the logic functions used as benchmarks in this work: INVerter, AND, OR and MUltipleXer[1].

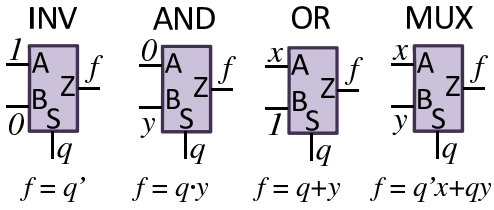

Fig. 7. Logic gates architectures using the RG-device as primitive

For each logic function, the corresponding input configuration pattern is applied at each of the six equivalent faulty netlists presented in the previous section (Figure 6). The results obtained through SPICE simulations have been summarized in the Tables II, III, IV.

The three tables show the behavior of primary inputs and outputs (column *PI* & *PO*) under different defects (column *defect*) as collected from SPICE simulations; the search for possible faults models is done at two levels, the logic level

[1]Recall that a logic "1" corresponds to +$V_{dd}/2$, logic "0" to -$V_{dd}/2$.

(column *Logic Fault Model*) and the component level (column *Component Fault Model*).

At a glance, one can observe that most of the defects can be mapped using standard stuck-at fault models at the logic level. However there are cases where no suitable logic models can be applied, indicated as '*' in the tables, and for which a component level fault model is needed, the st-at-0V. Such a model identifies the condition under which a given terminal is frozen at an intermediate voltage value, i.e., 0V, mid value of input voltage swing.

1) INV fault models (Table II): referring to Figure 6), in case of Short between $\bar{U}\&S$ ($S\&U$) the output Z follows the signal at A (B), which, for the INV logic (Figure 7) is fixed at "1" ("0"). This behavior is intrinsically imposed by the structure of the RG-device, which always forces the output Z following the input associated to the lowest resistance (R_{low}). Less significant, but still possible, is to map Short-$\bar{U}\&S$ (Short-$S\&U$) as a st-at-0 (st-at-1) on the input S.

A similar logic behavior has been observed for Open defects on A (B), for which the output Z is forced to follow B (A), resulting in a st-at-0 (st-at-1) on Z. In this case the high impedance at A (B) is due to floating input contacts rather than a change of the doping profile (Figure 6). Differently, for Short-$\bar{U}\&S$ and Short-$S\&U$ is not possible to identify any fault at the input S.

Substantially different is the defect Short $\bar{U}\&S\&\bar{U}$, For this specific case, is the difference between the values applied at the inputs A and B that comes into play. As shown in Figure 6, both A and B are connected to Z with the same resistance R_G; when the logic values at A and B are concordant (i.e., both at "1" or "0"), Z settles to that value (i.e., "1" or "0"), when discordant, Z settles to 0V, i.e., st-at-0V. However, since in the INV implementation A and B are fixed to opposite values by construction, Z is stuck at 0V.

2) AND and OR fault models (Table III): In the AND configuration both namely back-gate S and the front-contact B act as logic inputs, whereas the front contact A is fixed at logic "0" (Figure7). The electrical analysis done for the single-variable function INV still hold here, but, due to a different input pattern configuration, the resulting fault models slightly differ.

The Short $\bar{U}\&S$ forces Z to follow A causing a st-at-0 fault at the output Z; the Short $S\&U$, instead, makes Z to follow B, which now represents a logic input of the AND, i.e., st-at-B. This kind of behavior are known as stuck-at logical effect in CMOS technologies.

For the same reason, defects Open A and Open B can be mapped as st-at-B and st-at-0 on Z respectively.

In contrast with the analysis done for the INV gate, the Short $\bar{U}\&S\&\bar{U}$ induces a different behavior. For the AND, in fact, only the front contact A is driven by a steady "0", while B is driven by a "free" signal. Therefore, a dual behavior can be observed: B="0" implies a st-at-0 on Z (A and B concordant); B="1" implies a st-at-0V on Z (A and B discordant). In other words, there is not an unique fault model one can use, instead contrasting behaviors appear depending on the logic input. This might represent a critical issue during test pattern generation.

The effect produced by the Open Z defect is the same as that of the INV, and hence, the same model does apply, namely, st-at-0V.

Concerning the OR logic gate, it is important to highlight that its implementation can be seen as the complement of the AND (Figure7): A represents the logic input and B is fixed at "1". Therefore the defect mapping can be easily inferred from that of the AND gate. More specifically, those defects that are mapped with a st-at-0 in the AND result in a st-at-A; defects that are mapped to st-at-B in the AND result in st-at-1 in the OR; Short $\bar{U}\&S\&\bar{U}$ and Open Z are equivalent in both AND and OR. The result table for the OR gate has been omitted for the sake of space.

3) MUX fault models (Table IV): In the implementation of the MUX gate both A and B are logic inputs that can assume any of the two logic values, and hence, st-at-0 and st-at-1 faults never occur.

The Short $\bar{U}\&S$ forces Z to follow A, i.e., st-at-A on Z, while, the Short $S\&U$ forces Z to follow B, i.e., st-at-B.

An Open A obviously forces Z to follow B, i.e., st-at-B on Z, while an Open B forces Z to follow A, i.e., st-at-A.

Finally, as for the INV, AND and OR gates, the Short $\bar{U}\&S\&\bar{U}$ and the Open Z are modeled at component level as stuck-at-0V on Z.

V. Conclusions and Final Remarks

This paper proposes a study on the effects of physical failures in a new class of graphene based reconfigurable logic gates. Apart from introducing the equivalent electrical models of the faulty devices, it also proposes possible defect-to-fault mapping using proper fault models.

The obtained results demonstrate that, as for the CMOS technologies, faults models at different levels of abstraction are needed for the full coverage of the physical defects. As transistor-level models in the CMOS technologies helped to cover specific failures whose effect was not observable at the logic value, so does the suck-at-0V for the RG-devices. The suck-at-0V model is reminiscent of the stuck-short model used in CMOS circuits to cover the *Vdd*-to-*Gnd* shorts that cause the outputs of logic gates to reach intermediate values. Differently from CMOS, however, the actual output value is not determined by the impedance ratios between pull-up/down networks or the the associated faults, indeed, it is stuck at a precise voltage. This is manly due to the symmetric structure of the graphene device.

Going on through the comparison with CMOS technologies, a right and proper consideration relies on the fact that while in CMOS technologies the implementation of a given Boolean logic function requires multiple transistors, using the RG-devices even complex functions, like the MUX, require a single component. This may have positive impact on testing as the cardinality of possible defects per logic gate drastically reduces. The downside is that physical defects do not necessarily produce the same faulty behavior, namely, the same defect

TABLE II
MAPPING DEFECTS FOR INV FUNCTION, PI-PRIMARY INPUT AND PO-PRIMARY OUTPUT

Function: INV	**PI & PO**		**Logic Fault Model**		**Component Fault Model**	
Defect	*S*	*Z*	*S*	*Z*	*S*	*Z*
Short $\overline{U}$ & S	0	Z=notS=1	st-at-0	st-at-1	*	*
Short S & U	1	Z=notS=0	st-at-1	st-at-0	*	*
Short $\overline{U}$ & S & U	0V	Z=0V	*	*	st-at-0V	st-at-0V
Open A	0 / 1	Z=B=0	*	st-at-0	*	*
Open B	0 / 1	Z=A=1	*	st-at-1	*	*
Open Z	0 / 1	Z=0V	*	*	*	st-at-0V

TABLE III
MAPPING DEFECTS FOR AND FUNCTION, PI-PRIMARY INPUT AND PO-PRIMARY OUTPUT

Function: AND	**PI & PO**		**Logic Fault Model**		**Component Fault Model**	
Defect	*S*	*Z*	*S*	*Z*	*S*	*Z*
Short $\overline{U}$ & S	0	Z=A=0	st-at-0	st-at-0	*	*
Short S & U	1	Z=B	st-at-1	st-at-B	*	*
Short $\overline{U}$ & S & U	0V	Z=0, B=0 Z=0V, B=1	* *	* *	st-at-0V	* *
Open A	0 / 1	Z=B	*	st-at-B	*	*
Open B	0 / 1	Z=A=0	*	st-at-0	*	*
Open Z	0 / 1	Z=0V	*	*	*	st-at-0V

TABLE IV
MAPPING DEFECTS FOR MUX FUNCTION, PI-PRIMARY OUTPUT AND PO-PRIMARY OUTPUT

Function: MUX	**PI & PO**		**Logic Fault Model**		**Component Fault Model**	
Defect	*S*	*Z*	*S*	*Z*	*S*	*Z*
Short $\overline{U}$ & S	0	Z=A	st-at-0	st-at-A	*	*
Short S & U	1	Z=B	st-at-1	st-at-B	*	*
Short-$\overline{U}$ & S & U	0V	Z=A=B=0 Z=A=B=1 Z=0V, A≠B	* * *	* * *	st-at-0V	* * *
Open A	0 / 1	Z=B	*	st-at-B	*	*
Open B	0 / 1	Z=A	*	st-at-A	*	*
Open Z	0 / 1	Z=0V	*	*	*	st-at-0V

on the same RG-device, generates different faults depending on the logic configuration of the device itself.

These and other issues are currently object of study, and they will probably demand for new testing methods and tools. For instance, it is planned to investigate the effects of open defects at the back-gates and proper algorithm for test patterns generation.

REFERENCES

[1] K. S. Novoselov, D. Jiang, F. Schedin, T. Booth, V. Khotkevich, S. Morozov, and A. K. Geim, "Two-dimensional atomic crystals," in *Proceedings of the National Academy of Sciences of The United States of America*, 2005, pp. 10 451–10 453.

[2] Y.-M. Lin, C. Dimitrakopoulos, K. A. Jenkins, D. B. Farmer, H.-Y. Chiu, A. Grill, and P. Avouris, "100-ghz transistors from wafer-scale epitaxial graphene," *Science*, vol. 327, no. 5966, p. 662, 2010.

[3] H. Yang, J. Heo, S. Park, H. J. Song, D. H. Seo, K.-E. Byun, P. Kim, I. Yoo, H.-J. Chung, and K. Kim, "Graphene barristor, a triode device with a gate-controlled schottky barrier," *Science*, vol. 336, no. 6085, pp. 1140–1143, 2012.

[4] S. Tanachutiwat, J. U. Lee, W. Wang, and C. Y. Sung, "Reconfigurable multi-function logic based on graphene p-n junctions," in *DAC'10: ACM/IEEE Design Automation Conference*, june 2010, pp. 883 –888.

[5] M. Lemme, T. Echtermeyer, M. Baus, and H. Kurz, "A graphene field-effect device," *IEEE Electron Device Letters*, vol. 28, no. 4, pp. 282–284, apr 2007.

[6] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, and A. A. Firsov, "Electric field effect in atomically thin carbon films," *Science*, vol. 306, no. 5696, pp. 666–669, 2004.

[7] B. Huard, J. Sulpizio, N. Stander, K. Todd, B. Yang, and D. Goldhaber-Gordon, "Transport measurements across a tunable potential barrier in graphene," *Physical review letters*, vol. 98, no. 23, p. 236803, 2007.

[8] S. Miryala, A. Calimera, E. Macii, and M. Poncino, "Delay model for reconfigurable logic gates based on graphene pn-junctions," in *GLSVLSI'13: ACM , Great Lakes Symposium on VLSI*, may 2013, pp. 1–6.

[9] S. Miryala, M. Montazeri, A. Calimera, E. Macii, and M. Poncino, "A verilog-a model for reconfigurable logic gates based on graphene pn-junctions," in *DATE'13: ACM/IEEE Design, Automation and Test in Europe*, mar 2013, pp. 1–4.

[10] P. Chenyun and A. Naeemi, "Device- and system-level performance modeling for graphene p-n junction logic," in *ISQED'12: IEEE International Symposium on Quality Electronic Design*, march 2012, pp. 262 –269.

[11] A. Crouch, *Design-for-test for Digital IC's and Embedded Core Systems: CD ROM*, ser. Design-for-test for Digital IC's and Embedded Core Systems. Prentice Hall PTR, 1999. [Online]. Available: http://books.google.it/books?id=eJMHYgEACAAJ

[12] V. D. Agrawal, 1943, and I. ebrary, *Essentials of electronic testing for digital, memory, and mixed signal VLSI circuits*, ser. Frontiers in electronic testing ;. New York :: Kluwer Academic,, c2002. [Online]. Available: http://site.ebrary.com/lib/wmulib/Doc?id=10053265

[13] M. Sachdev, "Defect oriented testing for CMOS analog and digital circuits," 1998.

[14] L.-T. Wang, C.-W. Wu, and X. Wen, *VLSI Test Principles and Architectures: Design for Testability (Systems on Silicon)*. San Francisco, CA, USA: Morgan Kaufmann Publishers Inc., 2006.

[15] V. V. Cheianov and V. I. Fal'ko, "Selective transmission of dirac electrons and ballistic magnetoresistance of *n-p* junctions in graphene," *Phys. Rev. B*, vol. 74, p. 041403, Jul 2006.

[16] V. V. Cheianov, V. Fal'ko, and B. L. Altshuler, "The focusing of electron flow and a veselago lens in graphene p-n junctions," *Science*, vol. 315, no. 5816, pp. 1252–1255, 2007.

[17] S. Al-Arian and D. Agrawal, "Physical failures and fault models of cmos circuits," *Circuits and Systems, IEEE Transactions on*, vol. 34, no. 3, pp. 269 – 279, mar 1987.