Power Modeling and Characterization of Graphene-Based Logic Gates

Sandeep Miryala, Andrea Calimera, Enrico Macii, Massimo Poncino

Dipartimento di Automatica e Informatica, Politecnico di Torino, Torino, Italy
Email: {sandeep.miryala, andrea.calimera, enrico.macii, massimo.poncino}@polito.it

***Abstract*—As a result of CMOS technology approaching its physical limits and of the semiconductor market has started asking for materials that are able to implement new smarter devices, Graphene and composites are emerging as potential replacements for Silicon.**
Unlike true semiconductors, however, Graphene shows a zero-gap energy band structure that could potentially limit its use in digital applications. Nevertheless, recent works have proven the possibility of implementing electrostatically controlled pn-junctions which serve as a basic primitive for a new class of digital logic gates. These gates naturally behave as a 2-to-1 multiplexer in which the polarity of the input select line can be dynamically reconfigured: the Reconfigurable Graphene MUltipleXer (RG-MUX). Interconnection of multiple RG-MUXs with proper assignments of the inputs signals allow to implement all the basic Boolean logic functions.
In this work we investigate the electrical properties of RG-MUXs. More specifically, we introduce a power consumption model that could be used in future design and optimization tools for digital circuits. Characterization data obtained through SPICE-level simulations of a RG-MUX are collected and used to validate the model.

I. Introduction

In the near future electronic circuits can benefit from the unique properties of Graphene [1] to implement a new generation of electronic systems with enhanced mechanical features, like stretchability, flexibility and transparency.
However, due to its two-dimensional (2D) atomic structure, Graphene shows electrical characteristics that substantially differ from semiconductors used in today's Field Effect Transistors (FETs). The most relevant one is the lack of an energy gap between conduction and valence bands, which, indeed, touch each other at the Fermi Energy (E_F). This prevents the material to implement the OFF state and complicates the fabrication of digital devices with reasonable ON/OFF current ratio.
Different solutions have been proposed in the recent years to overcome this drawback. Most of them, e.g., [2] and [3], face the problem with a radical approach: the cut of Graphene sheets into narrow stripes (called as Graphene Nanoribbons, i.e., GNRs). Those GNRs show an energy band gap proportional to their width and can be used as a regular semiconductor to implement Graphene-FETs [4]. Although effective, these approaches suffer from a severe limitation, namely, the injection of physical defects that alter the level of disorder of the material [5].
Only few other works, instead, propose a less aggressive strategy based on *electrostatic doping*. The latter is used to implement an equivalent graphene pn-junction [6] that serves as basic switch for a more complex logic gate [7], the target of this work. Such a gate consists of a graphene sheet with co-planar split gates placed on the back side (through which is possible to implement the electrostatic doping) and three metal-to-graphene contacts on the front side (which serve as in/out-put pins); as will be shown later in the text, it conceptually implements a reconfigurable 2-to-1 multiplexer, the *RG-MUX*. It is worth noticing that, since electrostatic doping does not require any graphene patterning, the RG-MUX preserves the intrinsic properties of the material.
The electrical/functional characteristics of the RG-MUX are making it quite attractive in the CAD community. The works described in [8] and [7], for instance, provide an electrical model of the device and show how proper interconnections of multiple RG-MUXs allow to implement a full library of logic gates; results published in [7] and [9] also state the superior of logic gates implemented with the RG-MUX w.r.t. the CMOS counterparts. More abstract delay and fault models are finally proposed in [10] and [11], while [12] discusses possible implementation style of designs that use RG-MUXs.
In this work we take a step forward and we propose an analytical model for the dynamic power consumption of the RG-MUX. Following the same methodology introduced in [10], the in-to-out transition paths across the device are organized in two main categories, i.e., *back-to-out* (containing those patterns that involve the back-gates of the RG-MUX) and *front-to-out* (containing those patterns that involve the front contacts of the RG-MUX); each of them is then associated with the proper power model. SPICE-level characterization data obtained by simulating a verilog-A model of the RG-MUX have been used to validate the proposed models.

II. Graphene Based Logic Gates

A. Graphene RG-MUX

Figure 1 shows the structure of the RG-MUX [7], including 3D, back and front views. The device consists of a graphene sheet and six metal pins: three metal gates on the back side, $\bar{U}$, S and U, that are isolated from the graphene by a thick layer of oxide, and three metal-to-graphene contacts on front side, A, B (as inputs) and Z (as output). Pins $\bar{U}$ and U are the *configuration pins* and are always driven by complemented voltages; the pin S works as *selective pin* of the MUX, whose polarity is controlled through $\bar{U}$ and U.
The voltages applied at the back-gates $\bar{U}$, S and U, implement the electrostatic doping [13] through which the doping profile

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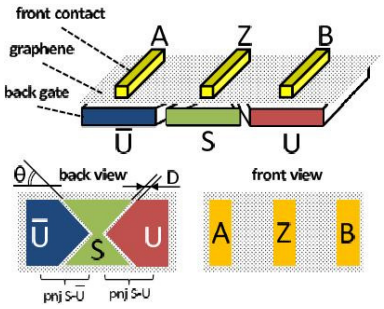


Fig. 1. RG-MUX design views.

of the two resulting back-faced pn-junctions (*pnj S-$\bar{U}$* on the left and *pnj S-U* on the right) can be dynamically controlled. When U='1' ($\bar{U}$='0'), the graphene region above the U gate results as n-doped (the Fermi energy E_F moves up in the conduction band due to positive control voltage), while that above the $\bar{U}$ gate as p-doped (the Fermi energy E_F moves down in valence band due to a negative control voltage). Notice that the '1'-logic value is $+V_{dd}/2$ and the '0'-logic value is $-V_{dd}/2$. Under such configuration, when S='0', the central graphene becomes p-type forming a pp-junction on the left and a pn-junction on the right; the pp-junction shows a low resistance (R_{pp}), whereas the pn-junction a high resistance (R_{pn}). The output Z, which follows the input signal associated with the smallest resistive path, is therefore connected to input A. On the contrary, when S ='1', the central graphene becomes n-type forming a low resistive nn-junction on the right (R_{nn}); this forces the output Z to follow B.
A dual behavior is observed when U='0' ($\bar{U}$='1'), namely, *Z=B* when *S=0* and *Z=A* when *S=1*; from a functional viewpoint this corresponds to changing the polarity of selective pin of the multiplexer.

B. Electrical Model

Figure 2 shows the electrical model of the RG-MUX. The two resistors R_{AZ} and R_{BZ} model the resistive graphene path from the input pins A and B to the output Z respectively. Their value ranges from $R_{nn} = 300\Omega$ ($= R_{pp}$), when the back-gates are polarized with same voltages (the ON state), to $R_{pn} = 10^7\Omega$ ($= R_{np}$), when the back-gates are polarized with opposite voltages (the OFF state).
The value of R_{nn} is given by:

$$R_{nn} = R_0/N_{ch} \tag{1}$$

where $R_0 = \frac{h}{4q^2}$ is the quantum resistance per mode and N_{ch} is the number of excited modes in the graphene sheet [1].
The resistance R_{pn} can be estimated including the transmission probability T_θ of the carriers across the pn-junction:

$$R_{pn} = \frac{R_o}{N_{ch}T(\theta)} \tag{2}$$

$T(\theta)$ depends on (i) the angle θ between the electron's wave vector (K_F) and the normal of the junction and (ii) the distance

[1]A detailed discussion of the electrical model is out of the scope of this work; interested readers can refer to prior works [7], [10] for additional details.

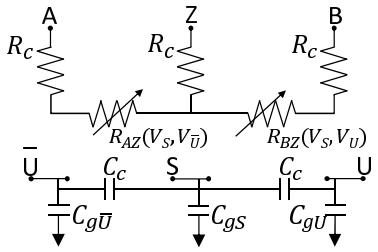


Fig. 2. RG-MUX electrical model.

D of the transition regions (please refer to back view in Figure 1). Equation 3 gives the expression for $T(\theta)$.

$$T(\theta) = \begin{cases} \cos^2(\theta)e^{-\pi D \cdot min\{K_{F,S}, K_{F,\bar{U}}\}\sin^2\theta} & \text{for } R_{AZ} \\ \cos^2(\theta)e^{-\pi D \cdot min\{K_{F,S}, K_{F,U}\}\sin^2\theta} & \text{for } R_{BZ} \end{cases} \tag{3}$$

where θ is 45^o by construction (please refer to Figure 1), while $K_{F,\bar{U}}$, $K_{F,S}$, $K_{F,U}$ are the Fermi wave vectors on the graphene regions above the back-gates $\bar{U}$, S and U respectively; all of them depend on the Fermi energy E_F whose level is function of the back-gates voltage[1].
The electrical model also includes parasitics of the metal contacts. The resistors R_c at the front pins A, B and Z, model the resistance of the metal-to-graphene contacts [7]. The lumped capacitance C_g at the back-gates (i.e., $C_{g\bar{U}}$ at $\bar{U}$, C_{gS} at S, C_{gU} at U) consists of the series of the oxide capacitance C_{ox} and the quantum capacitance of the graphene sheet C_q, i.e., $C_g = 1/(C_{ox}^{-1} + C_q^{-1})$[1].

C. MUX-based Logic Gate Library

Appropriate input configuration patterns can be fed to the RG-MUX in order to build several basic Boolean logic functions. A complete description of all the possible logic configurations can be found in [8]; for example, Figure 3 shows the configuration of four basic logic gates: INVerter, AND, OR and MUltipleXer.

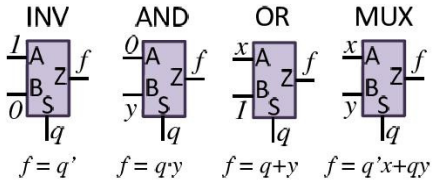


Fig. 3. Logic gates architectures using the RG-MUX as primitive.

III. Dynamic Power Model

Figure 4 shows the four different transition paths through the RG-MUX gate (depicted with its symbolic view): *S-to-Z* (from the select pin S to the output Z); *U-to-Z* (from the reconfiguration pin U to the output pin Z); *A-to-Z* and *B-to-Z* (from input pins A and B to output pin Z). Notice that, thanks to the symmetric structure of the device, (i) both low-to-high and high-to-low output transitions induce the same power consumptions, (ii) the paths *A-to-Z* and *B-to-Z* are electrically equivalent, (iii) also the paths *U-to-Z* and $\overline{U}$*-to-Z* are electrically equivalent.
Since the electrical behavior of the device is mainly defined by the type of terminals involved in the switching, we can

group the paths in two main categories [10]: *back-to-out* paths, i.e., those involving the back-gates (*S-to-Z* and *U-to-Z*), and *front-to-out* paths, i.e., those involving the front metal contacts (*A-to-Z* and *B-to-Z*). In the next subsections we describe the power models for the two categories.

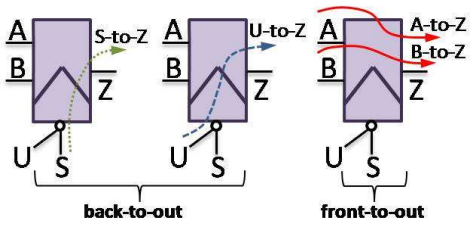


Fig. 4. In-to-out RG-MUX logic paths.

A. Power model for back-to-out transitions

During back-to-out transitions, the front contacts are driven by signals stuck at a constant logic value, whether it is '0' or '1', whereas the back-gate (U when considering the path *U-to-Z*, or S when considering the path *S-to-Z*), are fed with a rising, or falling, input signal.

Under this configuration the equivalent junction resistance between inputs (A, B) and output (Z), i.e., R_{AZ} and R_{BZ} (please refer to Section-II), can be seen as voltage-controlled resistor whose value depends on the voltage applied at the back-gates. Therefore, the input signals at A and B charge the output node Z through a variable resistor.

For the sake of clarity, and with no loss of generality, we consider a high-to-low output transition through the path *S-to-Z* for a simple inverter gate (INV configuration in the Figure 3) for which $U =$ '1' ($\bar{U} =$ '0'). As soon as S starts rising up, the graphene region on top of the back-gate S shifts from p-type to n-type changing the value of R_{AZ} from R_{pp} to R_{pn} (and that of R_{BZ} from R_{pn} to R_{nn}). Figure 5 plots R_{AZ} and R_{BZ} as function of the voltage at gate S; the plot is obtained using the Verilog-A model discussed in Section II. That pushes the output Z to switch from input A (stuck-at-'1') to input B (stuck-at-'0'), resulting in a high-to-low output transition.

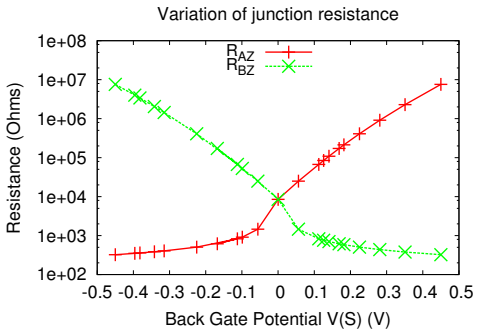


Fig. 5. R_{AZ} and R_{BZ} vs. voltage at the select pin S

This configuration is similar to that of CMOS gates in which the pull-up and pull-down networks show an equivalent resistance that dynamically changes with the signal voltage fed at the gate input. Hence, the energy consumed can be analytically modeled as typically done for standard CMOS circuits:

$$E_{back-to-out} = \frac{1}{2} \cdot C_l \cdot V_{dd}^2 \tag{4}$$

with C_l as the load capacitance at the output pin Z. Differentiating E over the output transition time T, we obtain the power dissipated for a single output transition:

$$P_{back-to-out} = \frac{1}{2} \frac{C_l \cdot V_{dd}^2}{T} \tag{5}$$

It is worth emphasizing that, thanks to the symmetric structure of the device, this model still holds for both low-to-high and high-to-low transitions, and for the logic paths *U-to-Z* and $\bar{U}$-*to-Z* also.

B. Power model for front-to-out transitions

During front-to-out transitions, the back-gates are driven by signals stuck at a constant logic value, whether it is '0' or '1', whereas the front contacts (A when considering the path *A-to-Z*, or B when considering the path *B-to-Z*), are fed with a rising, or falling, input signal.

Differently from back-to-out transitions, the equivalent junction resistances R_{AZ} and R_{BZ} keep a constant value for the entire switching period, i.e., R_{pn} or R_{nn} - depending on the voltages applied at U and S, while the output Z follows the switching dynamic of the inputs (A or B) associated with the lowest resistive path.

Let us consider a low-to-high output transition through the path *B-to-Z* for the AND gate (AND configuration in the Figure 3), with U='1' ($\bar{U}$='0') and S='1'. In this configuration $R_{AZ} = R_{pn}$, while $R_{BZ} = R_{nn}$; hence, Z follows the input signal B. As soon as B keeps rising, the load capacitance at Z charges up due to the current passing through R_{BZ} till it reaches a stable logic value.

As a matter of fact, the circuit simply reduces to a capacitor charged through a constant resistance with ramp input. The total average power consumption can be thereby expressed as:

$$P_{front-to-out} = \frac{1}{T} \int_0^T R_{nn} i_{C_l}^2(t) dt = \frac{R_{nn}}{T^2} C_l^2 V_{dd}^2 \tag{6}$$

IV. Characterization Results

The analytical models have been validated through the simulation of a standard SPICE netlist where the RG-MUX is instantiated by means of a macro containing the Verilog-A model presented in Section II. The RG-MUX is driven by piece-wise linear voltage sources that emulate ramp signals with parameterized rise/fall transition time t_{in}; the load is a parameterized capacitance C_l. The simulations cover a wide range of possible operating conditions: $t_{in} \in \{1ps : 200ps\}$ (20 steps), $C_l \in \{10fF : 32fF\}$[2] (20 steps). The supply voltage V_{dd} is fixed ad 0.9V, which implies '0'-logic$= -0.45V$ and '1'-logic$= 0.45V$.

Figures 6, 7 and 8 show the comparison between the power dissipation obtained with SPICE (lines) and that calculated with models (markers); the plots include the results for back-to-out paths, i.e., *S-to-Z* and *U-to-Z*, and the front-to-out path, i.e., *A-to-Z*. Notice that, as already introduced in Section III, due to the symmetric structure of the device, the paths $\bar{U}$-*to-Z* and *B-to-Z* are electrically equivalent to *U-to-Z* and *A-to-Z*

[2]In terms of fanout (FO) the load capacitance ranges from FO-2 to FO-8.

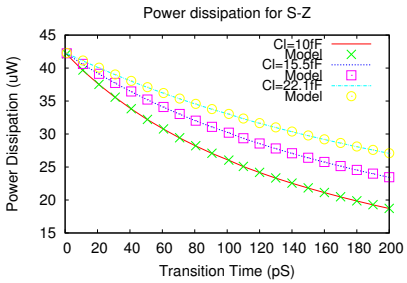


Fig. 6. S-to-Z power dissipation

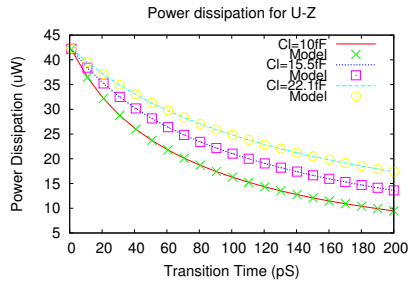


Fig. 7. U-to-Z power dissipation

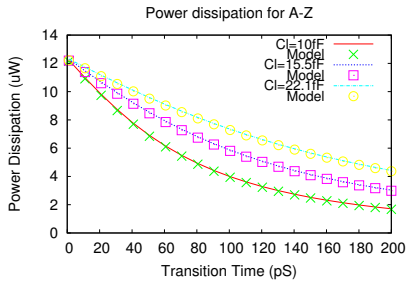
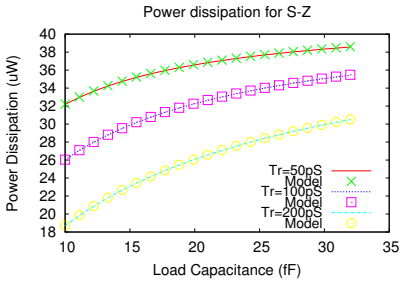
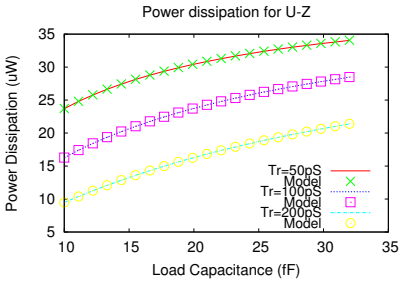
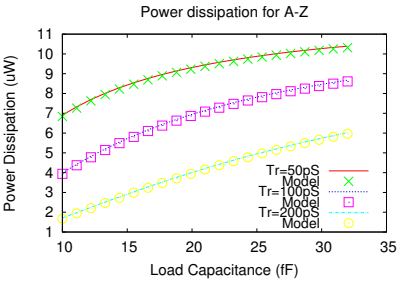


Fig. 8. A-to-Z power dissipation







respectively; hence, theirs plots have been omitted; for the same symmetry reasons, there is no difference between low-to-high and high-to-low output transitions.

As one can easily observe, the proposed models are in close agreement with SPICE simulations; this suggests their use in future logic-level analysis tools, with no need of pre-characterized look-up-tables (as done in modern CMOS CAD flows).

Concerning the dependence from the load capacitance (bottom plots), power dissipation increases as C_l gets larger; that's the classical behavior also shown by CMOS gates.

A less intuitive, yet more interesting analysis concerns the dependence from t_in. While for CMOS gates slower input signals (i.e., with longer t_in) may induce larger power consumption due to higher short-circuit currents, the same does not apply for the RG-MUX. In case of RG-MUX, as t_{in} gets larger, the output charging time (T in Equation 5) decreases proportionally, making the device less power hungry. This opens new optimization scenarios, where the amount of power consumption can be tuned by means of slower input signals, that is the basic principle behind adiabatic logic circuits.

V. Conclusions

Graphene devices based on electrostatically-controlled pn-junctions represent a potential alternative to CMOS logic gates. While this technology is still in the early days, the CAD community started investigating the design opportunity it might give.

Moving toward this direction, this paper introduced a first analytical models for the power consumption of a reconfigurable graphene multiplexer (RG-MUX), a multi-function gate that can be used as new primitive for digital logic circuits.

For each of the two types of transition paths, i.e., *back-to-out* and *front-to-out*, we provided an intuitive, yet effective model that well fits with simulation results obtained through SPICE. The proposed can be used for accurate power characterization of future graphene-based cells libraries.

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