Reconfigurable Multi-Function Logic Based on Graphene P-N Junctions

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ABSTRACT

In this paper, we introduce a novel reconfigurable graphene logic based on graphene p-n junctions. In this logic device, switching is accomplished by using co-planar split gates that modulate the properties that are unique to graphene, including ambipolar conduction, electrostatic doping, and angular dependent carrier reflection. In addition, the use of these control gates can dynamically change the operation of the device, leading to reconfigurable multi-functional logic. A device model is derived from carrier transmission probability across the p-n junction for allowing quantitative comparison to CMOS logic. Based on this model, we show that the proposed graphene logic has significant advantages over CMOS gate in terms of delay-power product and signal restoration, while maintaining a similar footprint. Furthermore, the device utilizes a large graphene sheet with minimal patterning, allowing feasible integration with CMOS circuits, for potential CMOS-graphene hybrid circuits.

Categories and Subject Descriptors

B.6.1 [**Logic Design**]: Design Styles – *combinational logic, logic arrays.* B.7.1 [**Integrated Circuits**]: Types and Design Styles – *advanced technologies, VLSI (very large scale integration).*

General Terms

Performance, Design.

Keywords

Graphene, Device, p-n Junction, Reconfigurable Logic, Logic Gate.

1. INTRODUCTION

Graphene, a mono-layer sheet of carbon atoms, exhibits many remarkable electronic properties. Graphene is characterized by long electron mean free path, ballistic transport, and high current density [1-6]. Its Fermi level can be tuned with a gate electrode to dope it with electrons or holes [7]. These features of graphene offer new opportunities for establishing novel carbon-based nanoelectronic systems that are functionally different from conventional CMOS devices. Several graphene nanoribbon FETs have been reported [8, 9] and these ribbons are expected to *open* a sufficiently large band-gap to be used as the FET channel material. However, one major challenge of using graphene ribbon is the edge scattering of the narrow ribbon, leading to relatively low mobility. Even the bandgap is not well defined in these structures due to edge disorder. Therefore, it is not clear that these devices can out-perform conventional Si-based FET devices. Instead, the graphene p-n junction device we propose is based on large graphene sheets and preserve the intrinsic chiral property of carriers. Therefore, it shows a significant improvement over the nanoribbon devices by utilizing intrinsic electronic properties of large graphene sheets, and can be used to establish novel reconfigurable logic gates with high performance.

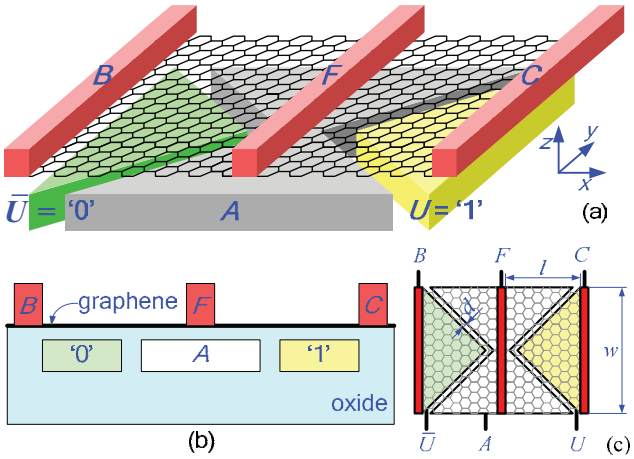

Figure 1. Proposed reconfigurable graphene logic gate: (a) 3D illustration, (b) cross section view, (c) top view.

Our device relies on electrostatic doping to form graded p-n junctions. The p-n junction is formed using co-planar split gates beneath a graphene sheet. The graphene sheet is laid on a very smooth surface to reduce electron scattering. By applying opposite biases (negative and positive bias voltages) to the split gates, the Fermi level of the two regions of the graphene sheet will be lowered and raised above the Dirac point, leading to p-type and n-type doping, respectively. Electrostatic doping has been used to demonstrate graphene p-n junctions [2] to validate theoretical estimates of conductance across the p-n interface [5].

Assuming a limited scattering effect, electrons can exhibit an optics-like behavior on a graphene sheet. Similar to optical lenses and prisms to manipulate light beam, graphene p-n interfaces can be used to manipulate carrier trajectory. This analogy has been extended in reference [3] to show that electrons injected from a point source on one side of the junction can be expected to refocus to a point on the other side of an abrupt p-n junction as the carriers scatter at the interface. A different analogy is that of a mirror to reflect electrons for a graded p-n interface. For the latter case, the

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electron transmission probability across the interface is strongly angle-dependent due to wavefunction mismatch and inter-band tunneling and is given as [5]:

$$T(\theta) = \cos^2(\theta) e^{-\pi k_F d \sin^2(\theta)} , \quad (1)$$

where k_F is the Fermi wave vector, θ is the incident angle between the electron's wave-vector and interface, and d is the gap of the p-n interface. Depending on θ and d, a fraction of electrons will be transmitted through the interface and the rest will be reflected [4]. For example, given reasonable values of d and k_F, the critical angle for the total internal reflection is 45°, yielding on/off ratio such as 10^3-10^5. Therefore, the device can be tuned from the on state to the off state by switching the n-n interface to the angle-dependant p-n interface.

Here, the strong dependence of transmission on angle is used to construct our multi-functional graphene device. For a large incident angle, the transport through a p-n junction can be highly resistive as most of the carriers will be reflected from the junction. The same junction, however, when doped as either an n-n or p-p interfaces will exhibit a low resistive state as carriers will be transported at the high Fermi velocity. This property will enable us to develop graphene logic based on p-n junctions.

In this paper, we develop a reconfigurable graphene logic circuit using back-to-back p-i-n junctions (here after called p-n junction for simplicity) formed from three split gates with three top contacts made to a single sheet of graphene (see Fig. 1). By modifying the voltages on the split gates, the ON/OFF state of the two junctions are switched, establishing different logic functions. Therefore, the proposed graphene logic provides multifunction gates that can be dynamically reconfigured, leading to innovative graphene circuit implementations.

2. GRAPHENE RECONFIGURABLE LOGIC

2.1 MUX-Based Logic

As shown in Fig. 1, the structure of the proposed graphene reconfigurable logic device consists of three split gates, three electrodes, and a single monolayer graphene sheet. To make the p-n junctions, bipolar voltages are required in the circuit. Here, we define logic '0' to be the negative voltage ($-½V_{DD}$) and logic '1' to be the positive voltage ($+½V_{DD}$).

The middle back gate is defined as input A. The triangular gates on either side of gate A are connected to $\overline{U}$ = '0' and U = '1' making the graphene regions above the gates p-type (green color) and n-type (yellow color), respectively, as shown in Fig. 1. These electrostatic gates are buried underneath the graphene sheet separated by a thin layer of oxide material (Fig. 1b). These two side gates are used to dynamically reconfigure the circuit.

The three electrodes on the top of and beneath the graphene are connected as follows. The middle electrode (F) is the output terminal while the left (B) and right (C) electrodes are used as input terminals.

Configuring the voltages of these electrodes, the circuit implements a multiplexer (MUX) function. Its operation is as follow. As shown in Fig. 2a, when input A is '1', the middle graphene region becomes n-type. The output electrode F connects to the right terminal C, i.e. $F = C$. For the other p-n junctions between electrodes B and F, however, the total internal reflection creates a high resistive state so that the current flow between these electrodes is turned off. Alternatively, as shown in Fig. 2b, when input A is '0', the middle graphene region becomes p-type and the output electrode F connects to the left terminal B, i.e. $F = B$. Similarly as before, a p-n junction is formed between F and C electrodes so the current flow between electrodes C and F is turned off. Therefore, the circuit performs the MUX function $F = AC + \overline{A}B$.

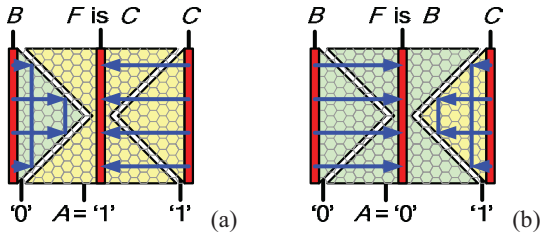
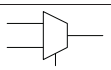
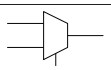
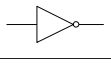
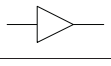
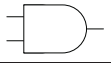
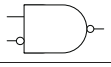
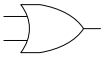
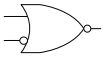


Figure 2. Operations of the device if configured as a 2:1 multiplexer: (a) The input A is '1', the output $F = C$, (b) when input A is '0', the output $F = B$.

Table 1. Multi-function and reconfigurability

		$U = 1$		$U = 0$	
V_B	V_C	Function	Output	Function	Output
B	C		$AC + \overline{A}B$		$\overline{A}C + AB$
1	0		$\overline{A}$		A
0	C		AC		$\overline{A\overline{C}}$
B	1		$A + B$		$\overline{A + \overline{B}}$

In Fig. 2, in order to get total reflection of the incident electron, the incident angle for each of the p-n interfaces is chosen to be $\theta = 45°$, although other angles are possible depending on the Fermi energy and the gate spacing d. Each angle, however, will lead to different transmission and reflection rates and make impact to the area, delay and power performance of the device.

2.2 Multi-Function and Reconfiguration

We now examine other functions that can be accomplished with this device. By modifying one or both of the top input terminals B and C, the graphene device can provide multiple functions as shown in Table 1 in addition to the MUX function described in the previous section.

When the terminals B/C are set to '1'/'0', respectively, an inverter function $F = \overline{A}$ is achieved. When input A is '0', the output F becomes '1'. When the input A is '1', the output F becomes '0'. Similarly, when the terminal B is set to '0' and the terminal C remains an input, the AND function $F = AC$ is obtained. When the terminal B remains as an input and the terminal C is set to '1', the OR function $F = A+B$ is achieved.

Note that a CMOS multiplexer can also provide similar multiple functions, which requires at least four transistors. However, such a MUX has weak output voltages and small fan-out, which cannot provide high-performance inverter, AND and OR gate functions. On the other hand, the proposed graphene MUX requires one integrated device structure with a similar area of four transistors, which can utilize the superior properties of

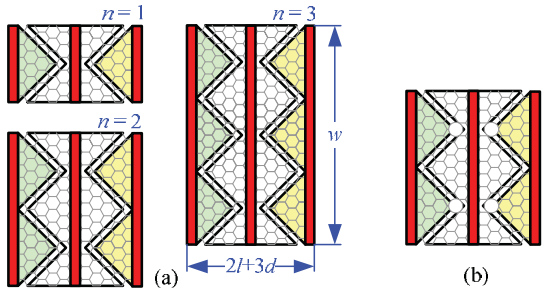


Figure 3. (a) Device scaling of the proposed device from n = 1, 2, and 3. (b) The Klein tunneling current can be reduced by introducing holes on the graphene sheet.

graphene to achieve high performance multi-function gates without voltage and fan-out degradation.

In addition, the proposed graphene multi-function device has an added reconfigurable capability by switching the two bottom control gate voltages as shown in Table 1. The above four functions are based on the bottom control gate $U = 1$. When $U = 0$ and $\bar{U} = 1$ are used, the output function will be changed as the input signal A is inverted, i.e. $F_0(A,B,C) = F_1(\bar{A},B,C)$. Therefore, the existing MUX function $F_0 = AC + \bar{A}B$ is programmed to become $F_1 = \bar{A}C + AB$. The inverter $F = \bar{A}$ will become a buffer $F = A$, while the AND and OR gates are also changed as seen in Table 1. Therefore, the proposed graphene device can be considered as a MUX-XOR gate:

$$F = \overline{(A \oplus U)}B + (A \oplus U)C \quad , \tag{2}$$

where the U terminals serve as control/configuration terminals. Note that the CMOS implementation of this function requires at least 8 transistors. Thus, the proposed graphene device can be half the size of the corresponding CMOS implementation.

3. DEVICE ANALYSIS

In order to evaluate the performance of the proposed device, we first estimate the resistance and capacitance values of the graphene p-n junction. Then, we carry out area, delay, and power performance analyses.

3.1 Capacitance and Resistance

For the proposed graphene device, the middle gate capacitance C_g is used to estimate the device RC delay and power consumption. It is a serial capacitance of the electrostatic capacitance C_{OX} and gate quantum capacitance C_Q, i.e. $C_g^{-1} = C_Q^{-1} + C_{OX}^{-1}$. Similar to the conventional parallel plate capacitor, C_{OX} depends on the oxide material and geometric dimension. The C_{OX} per unit area is $C_{OX,\square} = \varepsilon / EOT$, where ε is the oxide constant, and EOT is the effective oxide thickness. For the typical oxide material and thickness corresponding to 45nm and below technology nodes, $C_{OX,\square}$ is in the order of μF/cm^2.

The quantum capacitance depends on the Fermi energy of the graphene sheet. This Fermi energy E_F is derived from the gate voltage V_g and the oxide properties of the proposed device [7] as:

$$E_F = \frac{1}{\gamma EOT}\left(\sqrt{\varepsilon^2 + 2\gamma\varepsilon q V_g EOT} - \varepsilon\right) \quad , \tag{3}$$

where $\gamma = (4\pi q^2)/(h^2 v_F^2)$ is a constant depending on graphene properties, q is the elementary charge, v_F is the Fermi velocity, and h is the Plank's constant. Then, the quantum capacitance per unit area is $C_{Q,\square} = \gamma E_F$. For the proposed graphene device, $C_{q,\square}$ value is comparable to that of $C_{OX,\square}$, which is also in the order of μF/cm^2. Thus, $C_{g,\square}^{-1} = C_{OX,\square}^{-1} + C_{q,\square}^{-1}$. Note that when the middle gate voltage changes, E_F will change, leading to different $C_{q,\square}$ and $C_{g,\square}$ values.

The OFF and ON resistance values of the proposed graphene device depend on the electron transmission across the p-n and n-n interface, respectively. Due to the workfunction difference of the metal electrode and graphene sheet, the electrons coming out of the electrode can be modulated to have a narrow range of the direction variation [12]. Therefore, the electrons can travel to the p-n interface in a parallel trajectory on the graphene sheet. The incident angle of the electron transmission at the p-n interface is consistently 45°. Hence, the OFF resistance R_{pn} can be estimated by incorporating the transmission probability $T(\theta)$ from (1) into the quantum resistance, i.e. $R_{pn} = R_0 / (N_{ch} T(\theta))$, where $R_0 = h/(4q^2)$ is the quantum resistance per mode and $N_{ch} = wk_F/\pi$ [4] is the number of modes. Hence, the resistance of the p-n interface is:

$$R_{pn} = \frac{\pi h}{4q^2 w k_F T(\theta)} \quad , \tag{4}$$

where h, q, k_F and $T(\theta)$ are given above, while the device width w is illustrated in Fig. 1.

For an n-n interface, the carriers can easily cross the interface. The transmission is defined by the device geometry without the $T(\theta)$ part. The resistance across the n-n interface, R_{nn}, can be estimated by:

$$R_{nn} = \frac{\pi h}{4q^2 w k_F} \quad . \tag{5}$$

In addition to R_{pn} and R_{nn} values, a typical value for the contact resistance R_c between graphene and metal electrode is assumed to be in the order of 10Ω.

3.2 Area, Delay, and Power

By using the above RC values and the dimension parameters, the area, delay and power performance of the proposed device are evaluated. Considering the gap distance d, width of the device w and the narrowest length of the middle gate $2d$ (as illustrated in Fig. 1a), we calculate the distance of signal path as $l = \left(\sqrt{2} + \frac{1}{2}\right)d + \frac{1}{2}w$. Then, the device area is $A = (2l + d) \times w = 2wd\left(\sqrt{2} + 1\right) + w^2$. The area of the middle gate is $A_g = \frac{1}{2}w^2 + 2wd$, and that of the triangular gates is $A_{g2} = \frac{1}{4}w^2$.

Note that due to the 45° angle requirement of the split gates, the width w is correlated to the device length l for the structure shown in Fig. 1c, which adds unnecessary capacitance. In order to reduce the capacitance and increase the scalability of the device, the junction can be segmented into n regions as shown in Fig. 3a. Therefore, if w is fixed and n is increasing, the length $2l$ can be

Table 2. Performance comparison at 45nm technology

	CMOS	Graphene $n = 1$	Improvement
Device Area (μm^2)	0.405	0.382	6%
Switching Delay (ps)	2.46	0.451	82%
Switching Energy (fJ)	0.137	0.137	-
Total Power at 10GHz (μW)	5.78	5.59	3%
Delay-Power Product (ps-μW)	14.22	2.52	82%

Table 3. Performance comparison at 22nm technology

	CMOS	Graphene $n = 3$	Improvement
Device Area (μm^2)	0.0968	0.105	-8%
Switching Delay (ps)	1.27	0.177	86%
Switching Energy (fJ)	0.0286	0.0286	-
Total Power at 10GHz (μW)	1.23	3.15	-156%
Delay-Power Product (ps-μW)	1.56	0.557	64%

scaled down to $2l = 2\left(\sqrt{2}+\frac{1}{2}\right)d + \frac{1}{n}w$. By using this scaling scheme, the device area is $A = 2wd\left(\sqrt{2}+1\right) + \frac{1}{n}w^2$. The area of the middle gate is reduced to $A_g = \frac{1}{2n}w^2 + 2wd$, and that of the split gate is reduced to $A_{g2} = \frac{1}{4n}w^2$.

The logic delay evaluation is generally based on switching delay required to charge the output capacitance of the next stage. Here, we consider a load capacitance of 4 middle gates (fan-out of 4) for the next stage. Thus, the delay is estimated by using Elmore RC delay such that $\tau_{sw} = \left(R_{nn} + 2R_c\right)4C_g$, where gate capacitance is $C_g = C_{g,\square}A_g$.

The power performance analysis consists of three parts, i.e. leakage power of p-n junctions, oxide leakage power, and dynamic power. The p-n leakage power is based on the leakage current of the graphene p-n region. The power consumption due to the effective p-n resistance R_{pn} and two contact resistances $2R_c$ is estimated as $P_{leak} = V_{DD}^2 / \left(R_{pn} + 2R_c\right)$. The oxide leakage power is due to the vertical tunneling current through the gate oxide. The typical values of gate leakage current density (J_g) depending on *EOT* are obtained from ITRS [11]. For example, the gate leakage current is J_g = 1.88μA/μm^2 for *EOT* = 12Ang and it will increase with the thinner *EOT*. Thus, the oxide leakage power is $P_{g,leak} = \frac{1}{2}J_g\left(A_g + 2A_{g2}\right)V_{DD}$. The dynamic power analysis of the proposed device is based on the switching energy of one device driving the middle spilt gate of another device. The switching energy is $E_{sw} = \frac{1}{2}C_gV_{DD}^2$ and the dynamic power is $P_{dyn} = \alpha C_gV_{DD}^2 f$, where α = 0.5 is the activity factor and f is the clock frequency. Based on the three power consumption estimations, the overall power of the device can be obtained as $P_{total} = P_{dyn} + P_{leak} + P_{g,leak}$.

The above power analysis does not consider the Klein tunneling [10] of the graphene sheet location corresponding to the corner of the split gate. For carriers incident at angle θ = 0, the chiral nature of carriers precludes back scattering and leads to a large transmission (T = 1). To reduce such leakage currents, we propose to pattern small voids at these p-n interface corners as shown in Fig. 3b to reduce this leakage path, which might solve this leakage problem.

4. COMPARISON WITH CMOS

In order to demonstrate the efficiency of the proposed graphene reconfigurable device, we compare the performance of the proposed graphene device with the corresponding CMOS device based on both 45nm and 22nm technology nodes [11, 13].

The proposed graphene device provides a reconfigurable multi-function logic. A single device can be used as a MUX/INV/AND/OR gate as described in Fig. 2 and Table 1. For these functions, the corresponding CMOS gates will require 4/2/6/6 transistors. For a fair comparison, we compare the proposed graphene device with a typical 4-transistor CMOS gate (NAND). We consider a standard load of 4 input of the same gate (fan-out of 4) with interconnect resistances and capacitances. Since the switching energy depends on the gate capacitance C_g, we choose w and *EOT* of the graphene device such that C_g's are the same for both CMOS and grapheme gates.

Based on 45nm technology [11, 13], the performances of the CMOS gate in terms of area, delay, switching energy and total power are obtained from ITRS roadmap parameters: C_g = 302aF and V_{DD} = 0.95V.

For the corresponding grapheme device, the following design parameters need to be determined: n, w, *EOT*, d, and V_{DD}. Since the minimum feature of the 45nm technology node is 18nm, the value of d = 18nm and V_{DD} = 0.95V are used here [11]. Based on these values and n = 1, we choose the other parameters to enable the middle gate capacitance of the graphene device to be C_g. Using *EOT* = 17Ang, we have C_{OX} = 2.02μF/cm^2 for a given E_F = 0.18eV. Furthermore, w = 187nm is used here to get C_g = 302aF. The resistances of the p-n and n-n interfaces are R_{pn} = 10MΩ and R_{nn} = 318Ω. Therefore, the R_{OFF}/R_{ON} ratio is 3.15×10^5. Then, the area, delay and power data of the proposed graphene device are obtained and shown in Table 2. Note that the distance between adjacent devices of 2w is included in the graphene device area estimation, and resistance/capacitance of interconnects are also included.

The results in Table 2 demonstrate that for the 45nm technology node, the graphene device shows 6% area reduction compared with four CMOS transistors to implement the same function. It is 82% faster than the CMOS gate. Its total power including the gate oxide and p-n leakage is 3% smaller than the corresponding CMOS. Furthermore, the delay-power product of the delay is 82% better than the CMOS. Here, the graphene device is based on n = 1, without segments. If the segmented p-n junctions with n > 1 are used in a graphene device, an even more significant improvement over the 45nm CMOS gate is expected.

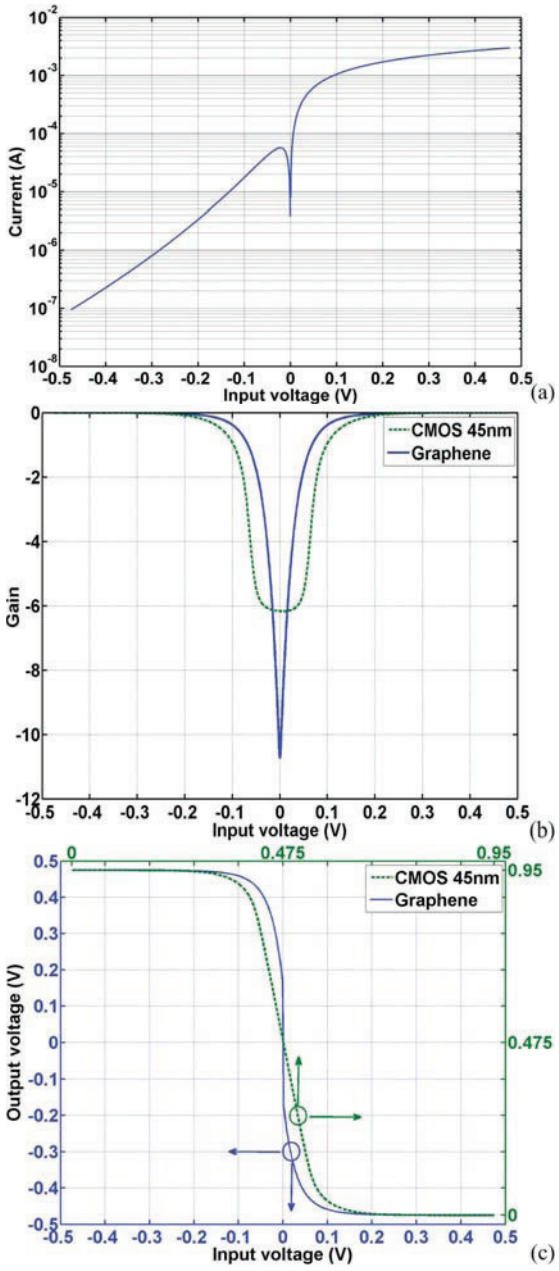


Figure 4. (a) I-V characteristics between terminals *A* and *C* of the proposed graphene device, (b) Inverter gain demonstrate signal restoration, (c) Transfer function characteristics of the proposed graphene inverter and 45nm CMOS inverter.

Based on the 22nm technology node, the CMOS performance is also derived using the parameters from the ITRS roadmap [11]. Here, the d = 9nm, C_g = 89aF, and V_{DD} = 0.8V are used. Whereas, the proposed graphene device characteristics are as follows: E_F = 0.22eV, w = 110nm, n = 3, EOT = 7Ang, and V_{DD} = 0.8V. In this way, the middle gate capacitance of the graphene device is also C_g = 89aF that is the same as the CMOS gate. Using these parameters, we have R_{pn} = 324kΩ and R_{nn} = 440Ω. R_{OFF}/R_{ON} is 735, which is much smaller than the 45nm case. This leads to a higher leakage power. As seen in Table 3, the graphene device is 86% faster than the CMOS device, while requiring 8% larger area. In addition, for the same switching energy, the total power of the graphene gate including the leakage power is much worse than the CMOS power consumption. Note that E_F value is increased by 1.22X to reduce the p-n leakage current. The delay-power product is the major indicator of the device performance. By trading-off high speed to get low energy and low power, the performance of the device is still better than the CMOS gate for 22nm technology node, leading to 64% improvement in terms of delay-power product.

This comparison study demonstrates that the proposed graphene device is a high-speed device, while providing complex logic function different from a single transistor device. However, the leakage power due to the p-n junction tunneling degrades the power performance. With aggressive scaling beyond the dimensions discussed above, a larger leakage current is expected, leading to an increase of the stand-by power. Our estimation suggests that the total power of the scaled graphene device will be similar to that of the corresponding CMOS device with modest performance improvement. In order to reduce the leakage current, a high Fermi level E_F is required, which might reduce the oxide thickness and lead to oxide tunneling and fabrication challenges. Therefore, new way to increase E_F is required to improve the performance of the proposed graphene device for below 22nm technologies.

Another advantage of our graphene device is the reconfigurable nature due to the use of the two control/configuration terminals (i.e. terminals $+U$ and $-U$ in Fig. 1). The voltages of these control terminals can be modified on-the-fly, which will tailor the MUX gate to other gate functions for different real-time computation tasks. Since these terminals are not in the signal paths, reconfiguration of the graphene device will not affect the operations of the other parts of the circuit, providing an efficient dynamical reconfigurable scheme. It is noteworthy that the CMOS MUX-XOR circuit (Eqn. 2) can also perform the same reconfigurable scheme. However, the CMOS implementation would suffer from the large footprint, two-stage operation delay, and large power consumption, which is not as efficient as the proposed graphene structure.

In addition to the aforementioned performance advantages and reconfigurable capabilities, the proposed graphene logic device might be easily fabricated and integrated with CMOS circuits. The proposed structure does not require the patterning of the graphene sheet. Instead, the split gates are patterned to different shapes to control the operation of the graphene sheet. The advanced CMOS lithography techniques can be used efficiently for the control gate patterning. Thus, the proposed device structure might be more efficient than most of the existing graphene structures that require graphene patterning. Even though the method to use the graphene into the foundry is still challenging, the proposed method can open new ways to establish an efficient integration of graphene devices with CMOS devices. Thus, this study might lead to the future technology breakthrough of establishing CMOS-graphene hybrid circuits.

5. CASE STUDY SIMULATION

Based on the above RC equations and performance data, we simulate the proposed graphene inverter driving other 4 graphene inverters (INV-FO4) as a case study to illustrate the performance advantage of our device. We use the graphene device parameters based on 45nm technology: d = 18nm, w = 187nm, n = 1, V_{DD} = 0.95V and EOT = 17Ang. For the purpose of comparison, we also

simulate the same INV-FO4 CMOS circuit based on 45nm technology. The HSPICE models for CMOS devices are obtained from [13].

The current-voltage (I-V) characteristics, voltage gain curve, and inverter transfer characteristics of the proposed inverter are shown in Fig. 4. The I-V characteristics between Terminals *A* and *C* of the proposed device are shown in Fig. 4a. The I-V characteristics demonstrate a diode-like behavior.

When terminal *C* is fixed to a positive voltage of '1', and the negative input voltage is applied to the terminal *A*, an asymmetric p-n junction is formed between the two terminals. This p-n junction will be more and more resistive when the input voltage becomes more negative. On the other hand, if the positive input voltage is applied to the terminal *A*, this junction will become n-n junction. In this case, the resistance of the n-n junction increases according to the decrease of the positive input voltage.

It is noted that, for a small positive and negative voltages, the resistance of the p-n and n-n junctions increases (see Fig. 4a around the input voltage of 0V). This is due to the fact that the density of states of the graphene sheet is too low to contribute to the conductance. Thus, the conductance is limited by the number of carriers rather than the p-n/n-n interfaces.

The inverter gain defined by $\partial V_{out}/\partial V_{in}$ of the proposed graphene p-n junction device shown in Fig. 4b is around -11, which demonstrates that the proposed inverter can provide strong signal restorations even with an input signal of only 30% of the voltage swing. Compared with the corresponding CMOS inverter with around -6 gains, the proposed graphene p-n junction device offers almost 2X gain improvement. The large gain of the proposed graphene inverter can enable the device to exhibit an excellent transfer behavior when the top terminals *B* and *C* connect to constant $\pm$½ V_{DD} values.

However, if the graphene device implements the MUX, AND, and OR functions, the transfer behavior is then different from the inverter case. All these three functions are based on the top electrode *B* or *C* connecting to an input signal. Thus, the voltages of the *B* and *C* terminals are not constant but depend on the input voltages from the previous stage. Thus, these voltages will be degraded due to the contact resistance and the channel resistance R_{nn}. This is similar to the voltage drop of the CMOS MUX. Therefore, an inverter or a buffer will be required to restore the signal after several stages of signal propagation in these cases.

The graphene inverter transfer characteristics are shown in Fig. 4c. The noise margin property of the device can be obtained from the transfer characteristics. The two unity gain points which determined the noise margin of the device are marked. The value of the characteristic voltages defined by the unity gain points are V_{IH} = 77.9mV = $-V_{IL}$ and V_{OH} = 436mV = $-V_{OL}$. Then, the noise margin values of the proposed graphene p-n junction inverter are $NM_L = NM_H$ = 358mV or 37.7% of the V_{DD} swing. Compared with the CMOS inverter which has $NM_H = NM_L$ = 336mV, the proposed graphene p-n junction device offers 6.5% noise margin improvement.

6. CONCLUSION

In this paper, we describe a novel graphene reconfigurable logic device based on the control of p-n doping configurations using split gates. By using split gates to change the graphene properties, multi-function logic gate can be obtained and can be dynamically reconfigured.

The physical model of the graphene logic is derived to examine the device performance. Compared to CMOS devices, the proposed graphene device shows significant speed advantages. For various technology nodes, the delay-power product of the proposed graphene device can be much better than those of the corresponding CMOS gates, which can be used to tradeoff speed to get efficient energy/power saving. We also demonstrate that the power dissipation of the graphene device in the below 22nm device can be similar to that of CMOS due to leakage currents, with only modest performance improvement. Further leakage reduction will require the use of the new doping techniques or oxide materials.

In addition to the performance comparison, the I-V simulation of the proposed graphene inverters is carried out. The results demonstrate that the graphene logic gate can provide excellent transfer behaviors with large voltage gain and noise margin. The scaling approach, device fabrication, and its integration with CMOS are also discussed in this paper. Due to these superior properties, this proposed graphene reconfigurable logic is expected to establish a novel computing paradigm for the post-CMOS era.

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